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Details

E·XF

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, I ² S, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	144KB (48K x 24)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f6012-30i-pf

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC30F6011/6012/6013/6014

Pin Diagrams (Continued)



Note: For descriptions of individual pins, see Section 1.0 "Device Overview".

NOTES:

Table 1-1 provides a brief description of device I/O pinouts and the functions that may be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE 1-1:	PINOUT I/O	DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN15	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVDD	Р	Р	Positive supply for analog module.
AVss	Р	Р	Ground reference for analog module.
CLKI CLKO	і О	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC
CN0-CN23	I	ST	function. Input change notification inputs. Can be software programmed for internal weak pull-ups on all
			inputs.
COFS CSCK CSDI CSDO	I/O I/O I O	ST ST ST —	Data Converter Interface frame synchronization pin. Data Converter Interface serial clock input/output pin. Data Converter Interface serial data input pin. Data Converter Interface serial data output pin.
C1RX C1TX C2PX	 0 	ST — ST	CAN1 bus receive pin. CAN1 bus transmit pin. CAN2 bus receive pin.
C2TX	0		CAN2 bus receive pin. CAN2 bus transmit pin
EMUD EMUC EMUD1	I/O I/O I/O	ST ST ST	ICD Primary Communication Channel data input/output pin. ICD Primary Communication Channel clock input/output pin. ICD Secondary Communication Channel data
EMUC1 EMUD2 EMUC2 EMUD3	I/O I/O I/O I/O	ST ST ST ST	input/output pin. ICD Secondary Communication Channel clock input/output pin. ICD Tertiary Communication Channel data input/output pin. ICD Tertiary Communication Channel clock input/output pin. ICD Quaternary Communication Channel data
EMUC3	I/O	ST	input/output pin. ICD Quaternary Communication Channel clock input/output pin.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INT0 INT1 INT2 INT3 INT4		ST ST ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2. External interrupt 3. External interrupt 4.
LVDIN	I	Analog	Low-Voltage Detect Reference Voltage input pin.
MCLR	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OCFA OCFB OC1-OC8	 0	ST ST —	Compare Fault A input (for Compare channels 1, 2, 3 and 4). Compare Fault B input (for Compare channels 5, 6, 7 and 8). Compare outputs 1 through 8.
Legend: CMOS = CMOS c ST = Schmitt I = Input	compatible Trigger inp	input or output out with CMOS le	Analog = Analog input evels O = Output P = Power

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TABLE 3-2:EFFECT OF INVALID
MEMORY ACCESSES

Attempted Operation	Data Returned
EA = an unimplemented address	0x0000
W8 or W9 used to access Y data space in a MAC instruction	0x0000
W10 or W11 used to access X data space in a MAC instruction	0x0000

All effective addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes or 32K words.

3.2.3 DATA SPACE WIDTH

The core data width is 16 bits. All internal registers are organized as 16-bit wide words. Data space memory is organized in byte addressable, 16-bit wide blocks.

3.2.4 DATA ALIGNMENT

To help maintain backward compatibility with PIC® MCU devices and improve data space memory usage efficiency, the dsPIC30F instruction set supports both word and byte operations. Data is aligned in data memory and registers as words, but all data space EAs resolve to bytes. Data byte reads will read the complete word which contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the X data path (no byte accesses are possible from the Y data path as the MAC class of instruction can only fetch words). That is, data memory and registers are organized as two parallel byte wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

As a consequence of this byte accessibility, all effective address calculations (including those generated by the DSP operations which are restricted to word sized data) are internally scaled to step through word aligned memory. For example, the core would recognize that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. Should a misaligned read or write be attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed, whereas if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap will then be executed, allowing the system and/or user to examine the machine state prior to execution of the address fault.

FIGURE 3-10: DATA ALIGNMENT

	15 MSB	8 7 LSB ()
0001	Byte1	Byte 0	0000
0003	Byte3	Byte 2	0002
0005	Byte5	Byte 4	0004
			-

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A sign-extend (SE) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions, including the DSP instructions, operate only on words.

3.2.5 NEAR DATA SPACE

An 8-Kbyte 'near' data space is reserved in X address memory space between 0x0000 and 0x1FFF, which is directly addressable via a 13-bit absolute address field within all memory direct instructions. The remaining X address space and all of the Y address space is addressable indirectly. Additionally, the whole of X data space is addressable using MOV instructions, which support memory direct addressing with a 16-bit address field.

3.2.6 SOFTWARE STACK

The dsPIC DSC devices contain a software stack. W15 is used as the Stack Pointer.

The Stack Pointer always points to the first available free word and grows from lower addresses towards higher addresses. It pre-decrements for stack pops and post-increments for stack pushes as shown in Figure 3-11. Note that for a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

Note:	A PC push during exception processing
	will concatenate the SRL register to the
	MSB of the PC prior to the push.

There is a Stack Pointer Limit register (SPLIM) associated with the Stack Pointer. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word aligned. Whenever an Effective Address (EA) is generated using W15 as a source or destination pointer, the address thus generated is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value, 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800, thus preventing the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 3-11: CALL STACK FRAME



TABLE 3-3: CORE REGISTER MAP

SFR Name	Address (Home)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
W0	0000								W0 / WR	EG								0000 0000 0000 0000
W1	0002								W1									0000 0000 0000 0000
W2	0004		W2											0000 0000 0000 0000				
W3	0006		W3											0000 0000 0000 0000				
W4	8000		W4											0000 0000 0000 0000				
W5	000A		W5											0000 0000 0000 0000				
W6	000C								W6									0000 0000 0000 0000
W7	000E								W7									0000 0000 0000 0000
W8	0010								W8									0000 0000 0000 0000
W9	0012								W9									0000 0000 0000 0000
W10	0014								W10									0000 0000 0000 0000
W11	0016								W11									0000 0000 0000 0000
W12	0018								W12									0000 0000 0000 0000
W13	001A								W13									0000 0000 0000 0000
W14	001C								W14									0000 0000 0000 0000
W15	001E								W15									0000 1000 0000 0000
SPLIM	0020								SPLIN	1								0000 0000 0000 0000
ACCAL	0022								ACCA	L								0000 0000 0000 0000
ACCAH	0024								ACCA	4								0000 0000 0000 0000
ACCAU	0026			Sign-E	xtension (A	ACCA<39) >)						ACC	AU				0000 0000 0000 0000
ACCBL	0028								ACCB	L								0000 0000 0000 0000
ACCBH	002A								ACCB	4								0000 0000 0000 0000
ACCBU	002C			Sign-E	xtension (A	ACCB<39	Ə>)						ACC	BU				0000 0000 0000 0000
PCL	002E								PCL									0000 0000 0000 0000
PCH	0030		_	—	_	_	_	_	_	—				PCH				0000 0000 0000 0000
TBLPAG	0032	-	—	—	_	—	—	_	—				TBLP	AG				0000 0000 0000 0000
PSVPAG	0034	-	—	—	_	—	—	_	—				PSVF	PAG				0000 0000 0000 0000
RCOUNT	0036								RCOUN	ΙT								uuuu uuuu uuuu uuuu
DCOUNT	0038								DCOUN	ΙT								uuuu uuuu uuuu uuuu
DOSTARTL	003A							DC	STARTL								0	uuuu uuuu uuuu uuu0
DOSTARTH	003C	_	_	—	—	—	—	_	—	_			DC	OSTARTH				0000 0000 0uuu uuuu
DOENDL	003E							D	OENDL								0	uuuu uuuu uuuu uuu0
DOENDH	0040	_		_	_	_	_		_	_			D	OENDH				0000 0000 0uuu uuuu

Legend: u = uninitialized bit

Note: Refer to "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

5.1 Interrupt Priority

The user assignable interrupt priority (IP<2:0>) bits for each individual interrupt source are located in the Least Significant 3 bits of each nibble within the IPCx register(s). Bit 3 of each nibble is not used and is read as a '0'. These bits define the priority level assigned to a particular interrupt by the user.

Note:	The user selectable priority levels start at
	0 as the lowest priority and level 7 as the
	highest priority.

Natural Order Priority is determined by the position of an interrupt in the vector table, and only affects interrupt operation when multiple interrupts with the same user-assigned priority become pending at the same time.

Table 5-1 lists the interrupt numbers and interrupt sources for the dsPIC DSC device and their associated vector numbers.

- **Note 1:** The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.
 - **2:** The natural order priority number is the same as the INT number.

The ability for the user to assign every interrupt to one of seven priority levels implies that the user can assign a very high overall priority level to an interrupt with a low natural order priority. For example, the PLVD (Low-Voltage Detect) can be given a priority of 7. The INTO (External Interrupt 0) may be assigned to priority level 1, thus giving it a very low effective priority.

TABLE 5-1:INTERRUPT VECTOR TABLE

INT Number	Vector Number	Interrupt Source						
Hiahest N	atural Orde	er Priority						
0	8	INT0 – External Interrupt 0						
1	9	IC1 – Input Capture 1						
2	10	OC1 – Output Compare 1						
3	11	T1 – Timer 1						
4	12	IC2 – Input Capture 2						
5	13	OC2 – Output Compare 2						
6	14	T2 – Timer 2						
7	15	T3 – Timer 3						
8	16	SPI1						
9	17	U1RX – UART1 Receiver						
10	18	U1TX – UART1 Transmitter						
11	19	ADC – ADC Convert Done						
12	20	NVM – NVM Write Complete						
13	21	SI2C – I ² C Slave Interrupt						
14	22	MI2C – I ² C Master Interrupt						
15	23	Input Change Interrupt						
16	24	INT1 – External Interrupt 1						
17	25	IC7 – Input Capture 7						
18	26	IC8 – Input Capture 8						
19	27	OC3 – Output Compare 3						
20	28	OC4 – Output Compare 4						
21	29	T4 – Timer 4						
22	30	T5 – Timer 5						
23	31	INT2 – External Interrupt 2						
24	32	U2RX – UART2 Receiver						
25	33	U2TX – UART2 Transmitter						
26	34	SPI2						
27	35	C1 – Combined IRQ for CAN1						
28	36	IC3 – Input Capture 3						
29	37	IC4 – Input Capture 4						
30	38	IC5 – Input Capture 5						
31	39							
32	40	OC5 – Output Compare 5						
33	41	OC6 – Output Compare 6						
34	42							
35	43	UC8 – Output Compare 8						
30	44							
<u>ः</u>	40	C2 Combined IDO for CANO						
ა ბ	40							
39-40	47-48	Reserved						
41	49							
42	51 61							
LOWEST N	atural Orde	r Priority						

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- 5. Execution of a "BRA #literal" instruction or a "GOTO #literal" instruction, where literal is an unimplemented program memory address.
- Executing instructions after modifying the PC to point to unimplemented program memory addresses. The PC may be modified by loading a value into the stack and executing a RETURN instruction.

Stack Error Trap:

This trap is initiated under the following conditions:

- The Stack Pointer is loaded with a value which is greater than the (user programmable) limit value written into the SPLIM register (stack overflow).
- 2. The Stack Pointer is loaded with a value which is less than 0x0800 (simple stack underflow).

Oscillator Fail Trap:

This trap is initiated if the external oscillator fails and operation becomes reliant on an internal RC backup.

5.3.2 HARD AND SOFT TRAPS

It is possible that multiple traps can become active within the same cycle (e.g., a misaligned word stack write to an overflowed address). In such a case, the fixed priority shown in Figure 5-1 is implemented, which may require the user to check if other traps are pending in order to completely correct the fault.

'Soft' traps include exceptions of priority level 8 through level 11, inclusive. The arithmetic error trap (level 11) falls into this category of traps.

'Hard' traps include exceptions of priority level 12 through level 15, inclusive. The address error (level 12), stack error (level 13) and oscillator error (level 14) traps fall into this category.

Each hard trap that occurs must be Acknowledged before code execution of any type may continue. If a lower priority hard trap occurs while a higher priority trap is pending, Acknowledged, or is being processed, a hard trap conflict will occur.

The device is automatically reset in a hard trap conflict condition. The TRAPR status bit (RCON<15>) is set when the Reset occurs so that the condition may be detected in software.

FIGURE 5-1: TRAP VECTORS



5.4 Interrupt Sequence

All interrupt event flags are sampled in the beginning of each instruction cycle by the IFSx registers. A pending interrupt request (IRQ) is indicated by the flag bit being equal to a '1' in an IFSx register. The IRQ will cause an interrupt to occur if the corresponding bit in the Interrupt Enable (IECx) register is set. For the remainder of the instruction cycle, the priorities of all pending interrupt requests are evaluated.

If there is a pending IRQ with a priority level greater than the current processor priority level in the IPL bits, the processor will be interrupted.

The processor then stacks the current program counter and the low byte of the processor STATUS register (SRL), as shown in Figure 5-2. The low byte of the STATUS register contains the processor priority level at the time prior to the beginning of the interrupt cycle. The processor then loads the priority level for this interrupt into the STATUS register. This action will disable all lower priority interrupts until the completion of the Interrupt Service Routine.

6.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*dsPIC30F/ 33F Programmer's Reference Manual*" (DS70157).

The dsPIC30F family of devices contains internal program Flash memory for executing user code. There are two methods by which the user can program this memory:

- 1. Run-Time Self-Programming (RTSP)
- 2. In-Circuit Serial Programming (ICSP)

6.1 In-Circuit Serial Programming (ICSP)

dsPIC30F devices can be serially programmed while in the end application circuit. This is simply done with two lines for Programming Clock and Programming Data (which are named PGC and PGD respectively), and three other lines for Power (VDD), Ground (Vss) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

6.2 Run-Time Self-Programming (RTSP)

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions.

With RTSP, the user may erase program memory, 32 instructions (96 bytes) at a time and can write program memory data, 32 instructions (96 bytes) at a time.

6.3 Table Instruction Operation Summary

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in Word or Byte mode.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can access program memory in Word or Byte mode.

A 24-bit program memory address is formed using bits<7:0> of the TBLPAG register and the effective address (EA) from a W register specified in the table instruction, as shown in Figure 6-1.

FIGURE 6-1: ADDRESSING FOR TABLE AND NVM REGISTERS



8.3 Input Change Notification Module

The input change notification module provides the dsPIC30F devices the ability to generate interrupt requests to the processor, in response to a change of state on selected input pins. This module is capable of detecting input change of states even in Sleep mode, when the clocks are disabled. There are up to 24 external signals (CN0 through CN23) that may be selected (enabled) for generating an interrupt request on a change of state.

TABLE 8-10: INPUT CHANGE NOTIFICATION REGISTER MAP FOR dsPIC30F6011/6012 (BITS 15-8)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset State
CNEN1	00C0	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	0000 0000 0000 0000
CNEN2	00C2	_	_	_	_	_	_	_	_	0000 0000 0000 0000
CNPU1	00C4	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	0000 0000 0000 0000
CNPU2	00C6	_		-	_	_	_		_	0000 0000 0000 0000

Note: Refer to "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

TABLE 8-11: INPUT CHANGE NOTIFICATION REGISTER MAP FOR dsPIC30F6011/6012 (BITS 7-0)

SFR Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CNEN1	00C0	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000 0000 0000 0000
CNEN2	00C2	_	_	_	_	_	CN18IE	CN17IE	CN16IE	0000 0000 0000 0000
CNPU1	00C4	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000 0000 0000 0000
CNPU2	00C6	—	—		—	—	CN18PUE	CN17PUE	CN16PUE	0000 0000 0000 0000
NL . A .	5				14	/" (DOTO)			· · ·	1 1 1 1 1

Note: Refer to "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

TABLE 8-12: INPUT CHANGE NOTIFICATION REGISTER MAP FOR dsPIC30F6013/6014 (BITS 15-8)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset State		
CNEN1	00C0	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	0000 0000 0000 0000		
CNEN2	00C2	_	—	—	_	_	—	_	—	0000 0000 0000 0000		
CNPU1	00C4	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	0000 0000 0000 0000		
CNPU2	00C6	_	_	_	_	_	_	_	_	0000 0000 0000 0000		
Mater												

Note: Refer to "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

TABLE 8-13: INPUT CHANGE NOTIFICATION REGISTER MAP FOR dsPIC30F6013/6014 (BITS 7-0)

SFR Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CNEN1	00C0	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000 0000 0000 0000
CNEN2	00C2	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000 0000 0000 0000
CNPU1	00C4	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000 0000 0000 0000
CNPU2	00C6	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000 0000 0000 0000

Note: Refer to "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

NOTES:

9.0 TIMER1 MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the 16-bit General Purpose Timer1 module and associated operational modes. Figure 9-1 depicts the simplified block diagram of the 16-bit Timer1 module.

The following sections provide a detailed description including setup and control registers, along with associated block diagrams for the operational modes of the timers.

The Timer1 module is a 16-bit timer which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter. The 16-bit timer has the following modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

Further, the following operational characteristics are supported:

- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

These Operating modes are determined by setting the appropriate bit(s) in the 16-bit SFR, T1CON. Figure 9-1 presents a block diagram of the 16-bit timer module.

16-bit Timer Mode: In the 16-bit Timer mode, the timer increments on every instruction cycle up to a match value preloaded into the Period register PR1, then resets to '0' and continues to count.

When the CPU goes into the Idle mode, the timer will stop incrementing unless the TSIDL (T1CON<13>) bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

16-bit Synchronous Counter Mode: In the 16-bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in PR1, then resets to '0' and continues.

When the CPU goes into the Idle mode, the timer will stop incrementing unless the respective TSIDL bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

16-bit Asynchronous Counter Mode: In the 16-bit Asynchronous Counter mode, the timer increments on every rising edge of the applied external clock signal. The timer counts up to a match value preloaded in PR1, then resets to '0' and continues.

When the timer is configured for the Asynchronous mode of operation and the CPU goes into the Idle mode, the timer will stop incrementing if TSIDL = 1.

dsPIC30F6011/6012/6013/6014

FIGURE 10-1: 32-BIT TIMER2/3 BLOCK DIAGRAM



16.2 Enabling and Setting Up UART

16.2.1 ENABLING THE UART

The UART module is enabled by setting the UARTEN bit in the UXMODE register (where x = 1 or 2). Once enabled, the UxTX and UxRX pins are configured as an output and an input respectively, overriding the TRIS and LATCH register bit settings for the corresponding I/O port pins. The UxTX pin is at logic '1' when no transmission is taking place.

16.2.2 DISABLING THE UART

The UART module is disabled by clearing the UARTEN bit in the UxMODE register. This is the default state after any Reset. If the UART is disabled, all I/O pins operate as port pins under the control of the latch and TRIS bits of the corresponding port pins.

Disabling the UART module resets the buffers to empty states. Any data characters in the buffers are lost and the baud rate counter is reset.

All error and status flags associated with the UART module are reset when the module is disabled. The URXDA, OERR, FERR, PERR, UTXEN, UTXBRK and UTXBF bits are cleared, whereas RIDLE and TRMT are set. Other control bits, including ADDEN, URXISEL<1:0>, UTXISEL, as well as the UxMODE and UxBRG registers, are not affected.

Clearing the UARTEN bit while the UART is active will abort all pending transmissions and receptions and reset the module as defined above. Re-enabling the UART will restart the UART in the same configuration.

16.2.3 SETTING UP DATA, PARITY AND STOP BIT SELECTIONS

Control bits PDSEL<1:0> in the UxMODE register are used to select the data length and parity used in the transmission. The data length may either be 8 bits with even, odd or no parity, or 9 bits with no parity.

The STSEL bit determines whether one or two Stop bits will be used during data transmission.

The default (power-on) setting of the UART is 8 bits, no parity and 1 Stop bit (typically represented as 8, N, 1).

16.3 Transmitting Data

16.3.1 TRANSMITTING IN 8-BIT DATA MODE

The following steps must be performed in order to transmit 8-bit data:

- 1. Set up the UART:
 - First, the data length, parity and number of Stop bits must be selected. Then, the transmit and receive interrupt enable and priority bits are setup in the UxMODE and UxSTA registers. Also, the appropriate baud rate value must be written to the UxBRG register.
- 2. Enable the UART by setting the UARTEN bit (UxMODE<15>).
- 3. Set the UTXEN bit (UxSTA<10>), thereby enabling a transmission.
- 4. Write the byte to be transmitted to the lower byte of UxTXREG. The value will be transferred to the Transmit Shift register (UxTSR) immediately and the serial bit stream will start shifting out during the next rising edge of the baud clock. Alternatively, the data byte may be written while UTXEN = 0, following which, the user may set UTXEN. This will cause the serial bit stream to begin immediately because the baud clock will start from a cleared state.
- 5. A transmit interrupt will be generated, depending on the value of the interrupt control bit UTXISEL (UxSTA<15>).

16.3.2 TRANSMITTING IN 9-BIT DATA MODE

The sequence of steps involved in the transmission of 9-bit data is similar to 8-bit transmission, except that a 16-bit data word (of which the upper 7 bits are always clear) must be written to the UxTXREG register.

16.3.3 TRANSMIT BUFFER (UXTXB)

The transmit buffer is 9 bits wide and 4 characters deep. Including the Transmit Shift register (UxTSR), the user effectively has a 5-deep FIFO (First-In, First-Out) buffer. The UTXBF status bit (UxSTA<9>) indicates whether the transmit buffer is full.

If a user attempts to write to a full buffer, the new data will not be accepted into the FIFO, and no data shift will occur within the buffer. This enables recovery from a buffer overrun condition.

The FIFO is reset during any device Reset but is not affected when the device enters or wakes up from a power-saving mode.

16.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding interrupt flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

- a) If UTXISEL = 0, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This implies that the transmit buffer has at least one empty word.
- b) If UTXISEL = 1, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two Interrupt modes during operation is possible and sometimes offers more flexibility.

16.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) will cause the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB, or starting other transmitter activity. Transmission of a break character does not generate a transmit interrupt.

16.4 Receiving Data

16.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

- 1. Set up the UART (see Section 16.3.1 "Transmitting in 8-bit data mode").
- 2. Enable the UART (see Section 16.3.1 "Transmitting in 8-bit data mode").
- A receive interrupt will be generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
- 4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
- 5. Read the received data from UxRXREG. The act of reading UxRXREG will move the next word to the top of the receive FIFO, and the PERR and

FERR values will be updated.

16.4.2 RECEIVE BUFFER (UXRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 implies that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer will be read and no data shift will occur within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a power-saving mode.

16.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding interrupt flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

- a) If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.
- b) If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 3 characters.
- c) If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

16.5 Reception Error Handling

16.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

- a) The receive buffer is full.
- b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.
- c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

17.5.6 TRANSMIT INTERRUPTS

Transmit interrupts can be divided into 2 major groups, each including various conditions that generate interrupts:

• Transmit Interrupt:

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. Reading the TXnIF flags will indicate which transmit buffer is available and caused the interrupt.

• Transmit Error Interrupts:

A transmission error interrupt will be indicated by the ERRIF flag. This flag shows that an error condition occurred. The source of the error can be determined by checking the error flags in the CAN Interrupt Status register, CiINTF. The flags in this register are related to receive and transmit errors.

- Transmitter Warning Interrupt:

The TXWAR bit indicates that the transmit error counter has reached the CPU warning limit of 96.

- Transmitter Error Passive:

The TXEP bit (CiINTF<12>) indicates that the transmit error counter has exceeded the error passive limit of 127 and the module has gone to error passive state.

- Bus Off:

The TXBO bit (CiINTF<13>) indicates that the transmit error counter has exceeded 255 and the module has gone to the bus off state.

17.6 Baud Rate Setting

All nodes on any particular CAN bus must have the same nominal bit rate. In order to set the baud rate, the following parameters have to be initialized:

- Synchronization Jump Width
- Baud Rate Prescaler
- Phase Segments
- Length determination of Phase Segment 2
- Sample Point
- Propagation Segment bits

17.6.1 BIT TIMING

All controllers on the CAN bus must have the same baud rate and bit length. However, different controllers are not required to have the same master oscillator clock. At different clock frequencies of the individual controllers, the baud rate has to be adjusted by adjusting the number of time quanta in each segment.

The nominal bit time can be thought of as being divided into separate non-overlapping time segments. These segments are shown in Figure 17-2.

- Synchronization Segment (Sync Seg)
- Propagation Time Segment (Prop Seg)
- Phase Segment 1 (Phase1 Seg)
- Phase Segment 2 (Phase2 Seg)

The time segments and also the nominal bit time are made up of integer units of time called time quanta or Tq. By definition, the nominal bit time has a minimum of 8 Tq and a maximum of 25 Tq. Also, by definition, the minimum nominal bit time is 1 μ sec corresponding to a maximum bit rate of 1 MHz.



FIGURE 17-2: CAN BIT TIMING

19.9 Module Power-down Modes

The module has 2 internal Power modes.

When the ADON bit is '1', the module is in Active mode; it is fully powered and functional.

When ADON is '0', the module is in Off mode. The digital and analog portions of the circuit are disabled for maximum current savings.

In order to return to the Active mode from Off mode, the user must wait for the ADC circuitry to stabilize.

19.10 ADC Operation During CPU Sleep and Idle Modes

19.10.1 ADC OPERATION DURING CPU SLEEP MODE

When the device enters Sleep mode, all clock sources to the module are shutdown and stay at logic '0'.

If Sleep occurs in the middle of a conversion, the conversion is aborted. The converter will not continue with a partially completed conversion on exit from Sleep mode.

Register contents are not affected by the device entering or leaving Sleep mode.

The ADC module can operate during Sleep mode if the ADC clock source is set to RC (ADRC = 1). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is complete, the CONV bit will be cleared and the result loaded into the ADCBUF register.

If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the ADC module will then be turned off, although the ADON bit will remain set.

19.10.2 A/D OPERATION DURING CPU IDLE MODE

The ADSIDL bit selects if the module will stop on Idle or continue on Idle. If ADSIDL = 0, the module will continue operation on assertion of Idle mode. If ADSIDL = 1, the module will stop on Idle.

19.11 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the ADC module to be turned off, and any conversion and sampling sequence is aborted. The values that are in the ADCBUF registers are not modified. The A/D Result register will contain unknown data after a Power-on Reset.

19.12 Output Formats

The ADC result is 12 bits wide. The data buffer RAM is also 12 bits wide. The 12-bit data can be read in one of four different formats. The FORM<1:0> bits select the format. Each of the output formats translates to a 16-bit result on the data bus.

FIGURE 19-5:	ADC OUTPUT DATA FORMATS

RAM Contents:					d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Read to Bus:																
Signed Fractional	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0
Fractional	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0
Signed Integer	d11	d11	d11	d11	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
		1		1		1									1	
Integer	0	0	0	0	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
	L	1		1		1		1		1					1	





TABLE 23-26: INPUT CAPTURE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characte	ristic ⁽¹⁾	Min	Мах	Units	Conditions			
IC10	10 TccL ICx Input Low Time		No Prescaler	0.5 Tcy + 20		ns				
			With Prescaler	10		ns				
IC11	TccH	ICx Input High Time	No Prescaler	0.5 Tcy + 20		ns				
			With Prescaler	10	-	ns				
IC15	TccP	ICx Input Period		(2 Tcy + 40)/N		ns	N = prescale value (1, 4, 16)			

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 23-10: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



TABLE 23-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Мах	Units	Conditions			
OC10	TccF	OCx Output Fall Time	_	—		ns	See Parameter D032			
OC11	TccR	OCx Output Rise Time	_	_	_	ns	See Parameter D031			

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 23-30: DCI MODULE (AC-LINK MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	o. Symbol Characteristic ⁽¹⁾⁽²⁾		Min	Typ ⁽³⁾	Max	Units	Conditions			
CS78	TFACL	Fall Time, SYNC, SDATA_OUT	_	TBD	TBD	ns	CLOAD = 50 pF, VDD = 3V			
CS80	TOVDACL	Output valid delay from rising edge of BIT_CLK	_	—	15	ns	_			

Note 1: These parameters are characterized but not tested in manufacturing.

2: These values assume BIT_CLK frequency is 12.288 MHz.

3: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 23-14: SPI MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



TABLE 23-31: SPI MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions			
SP10	TscL	SCKx Output Low Time ⁽³⁾	Tcy / 2	—	_	ns	_			
SP11	TscH	SCKX Output High Time ⁽³⁾	TCY/2	—	_	ns	_			

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCK is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.

TABLE 23-38: 12-BIT ADC MODULE SPECIFICATIONS

			Standard Operating Conditions: 2.7V to 5.5V (unless otherwise stated)								
AC CHA	ARACTERIS	STICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial								
				$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extende							
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions				
Device Supply											
AD01	AVdd	Module VDD Supply	Greater of VDD - 0.3 or 2.7	—	Lesser of VDD + 0.3 or 5.5	V	_				
AD02	AVss	Module Vss Supply	Vss - 0.3	_	Vss + 0.3	V	_				
	•		Reference	Inputs			•				
AD05	Vrefh	Reference Voltage High	AVss + 2.7	—	AVdd	V	_				
AD06	Vrefl	Reference Voltage Low	AVss	_	AVDD - 2.7	V	_				
AD07	Vref	Absolute Reference Voltage	AVss - 0.3	—	AVDD + 0.3	V	—				
AD08	IREF	Current Drain		180 .001	300 2	μΑ μΑ	A/D operating A/D off				
	Analog Input ⁽¹⁾										
AD10	VINH-VINL	Full-Scale Input Span	Vrefl		Vrefh	V	See Note 1				
AD11	Vin	Absolute Input Voltage	AVss - 0.3		AVDD + 0.3	V	—				
AD12	_	Leakage Current	_	±0.001	±0.610	μΑ	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V Source Impedance = $2.5 \text{ K}\Omega$				
AD13	_	Leakage Current	_	±0.001	±0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = $3V$ Source Impedance = 2.5 K Ω				
AD17	Rin	Recommended Impedance of Analog Voltage Source	—	—	2.5K	Ω	_				
			DC Accur	acy ⁽¹⁾							
AD20	Nr	Resolution	1	2 data b	its	bits					
AD21	INL	Integral Nonlinearity ⁽²⁾	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V				
AD21A	INL	Integral Nonlinearity ⁽²⁾	—	-	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V				
AD22	DNL	Differential Nonlinearity ⁽²⁾	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V				
AD22A	DNL	Differential Nonlinearity ⁽²⁾	—	-	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V				
AD23	Gerr	Gain Error ⁽²⁾	+1.25	+1.5	+3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V				
AD23A	Gerr	Gain Error ⁽²⁾	+1.25	+1.5	+3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V				
AD24	EOFF	Offset Error	-2	-1.5	-1.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V				

Note 1: These parameters are characterized but not tested in manufacturing.

2: Measurements taken with external VREF+ and VREF- used as the ADC voltage references.

3: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.