Renesas - D12670VFC33V Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	IrDA, SCI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	103
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12670vfc33v

Table 2.9 System Control Instructions

Instruction	Size*	Function
TRAPA	—	Starts trap-instruction exception handling.
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition to a power-down state.
LDC	B/W	(EAs) → CCR, (EAs) → EXR Moves the contents of a general register or memory, or immediate data to CCR or EXR. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
STC	B/W	CCR → (EAd), EXR → (EAd) Transfers CCR or EXR contents to a general register or memory. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
ANDC	B	CCR ∧ #IMM → CCR, EXR ∧ #IMM → EXR Logically ANDs the CCR or EXR contents with immediate data.
ORC	B	CCR ∨ #IMM → CCR, EXR ∨ #IMM → EXR Logically ORs the CCR or EXR contents with immediate data.
XORC	B	CCR ⊕ #IMM → CCR, EXR ⊕ #IMM → EXR Logically exclusive-ORs the CCR or EXR contents with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Note: * Size refers to the operand size.
B: Byte
W: Word

Bit	Bit Name	Initial Value	R/W	Description
10 9 8	W22 W21 W20	1 1 1	R/W R/W R/W	Area 2 Wait Control 2 to 0 These bits select the number of program wait states when accessing area 2 while AST2 bit in ASTCR = 1. A CAS latency is set when the synchronous DRAM is connected*. The setting of area 2 is reflected to the setting of areas 2 to 5. A CAS latency can be set regardless of whether or not an ASTCR wait state insertion is enabled. 000: Program wait not inserted 001: 1 program wait state inserted 010: 2 program wait states inserted 011: 3 program wait states inserted 100: 4 program wait states inserted 101: 5 program wait states inserted 110: 6 program wait states inserted 111: 7 program wait states inserted 000: Synchronous DRAM of CAS latency 1 is connected to areas 2 to 5. 001: Synchronous DRAM of CAS latency 2 is connected to areas 2 to 5. 010: Synchronous DRAM of CAS latency 3 is connected to areas 2 to 5. 011: Synchronous DRAM of CAS latency 4 is connected to areas 2 to 5. 1XXX: Setting prohibited.

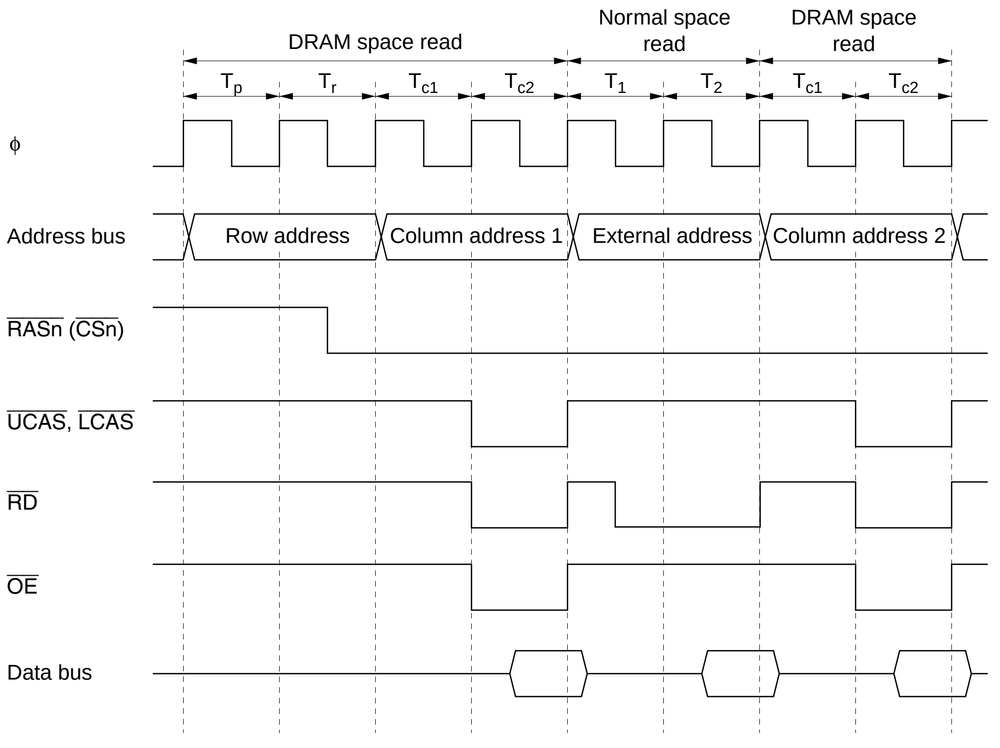
Note: * The synchronous DRAM interface is not supported in the H8S/2678 Group.

Legend: x: Don’t care.

Bit	Bit Name	Initial Value	R/W	Description
9 8	RCD1 RCD0	0 0	R/W R/W	RAS-CAS Wait Control These bits select a wait cycle to be inserted between the $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle. A 1- to 4-state wait cycle can be inserted. 00: Wait cycle not inserted 01: 1-state wait cycle inserted 10: 2-state wait cycle inserted 11: 3-state wait cycle inserted
7 to 4	—	All 0	R/W	Reserved These bits can be read from or written to. However, the write value should always be 0.
3	CKSPE	0	R/W	Clock Suspend Enable Enables clock suspend mode for extend read data during DMAC and EXDMAC single address transfer with the synchronous DRAM interface. 0: Disables clock suspend mode 1: Enables clock suspend mode
2	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.
1 0	RDXC1 RDXC0	0 0	R/W R/W	Read Data Extension Cycle Number Selection Selects the number of read data extension cycle (Tsp) insertion state in clock suspend mode. These bits are valid when the CKSPE bit is set to 1. 00: Inserts 1state 01: Inserts 2state 10: Inserts 3state 11: Inserts 4state

— self-refreshing is performed
— the chip enters software standby mode
— the external bus is released
— the RCDM bit or BE bit is cleared to 0

If a transition is made to the all-module-clocks-stopped mode in the $\overline{RAS}$ down state, the clock will stop with $\overline{RAS}$ low. To enter the all-module-clocks-stopped mode with $\overline{RAS}$ high, the RCDM bit must be cleared to 0 before executing the SLEEP instruction.



Note: n = 2 to 5

Figure 6.32 Example of Operation Timing in RAS Down Mode (RAST = 0, CAST = 0)

When the interval specification from the REF command to the ACTV cannot be satisfied, setting the RLW1 and RLW0 bits of REFCR enables one to three wait states to be inserted in the refresh cycle. Set the optimum number of waits according to the synchronous DRAM connected and the operating frequency of this LSI. Figure 6.56 shows the timing when one wait state is inserted.

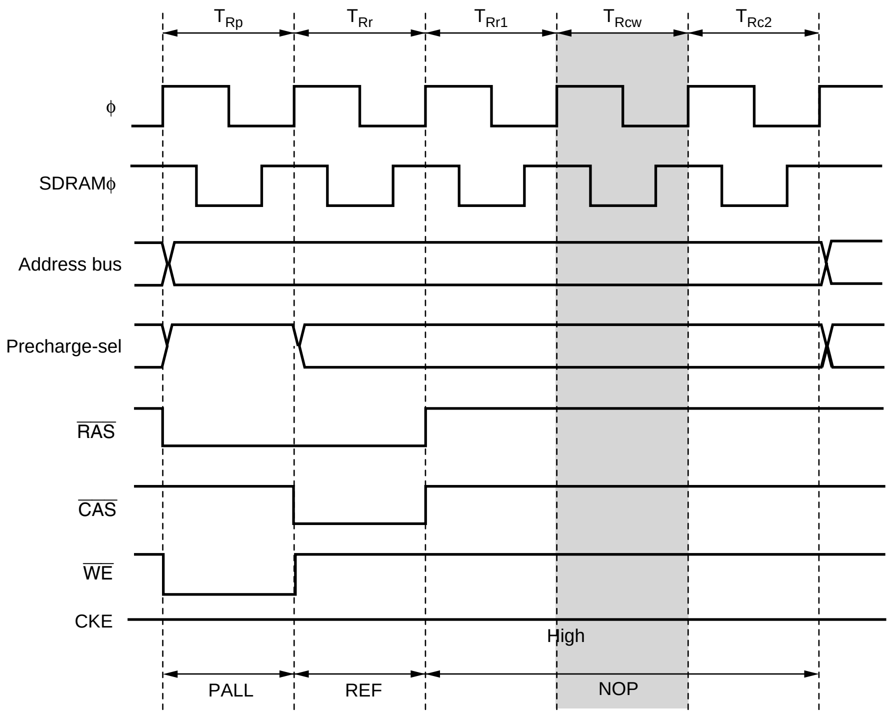


Figure 6.56 Auto Refresh Timing
(TPC = 0, TPC0 = 0, RLW1 = 0, RLW0 = 1)

Self-Refreshing: A self-refresh mode (battery backup mode) is provided for synchronous DRAM as a kind of standby mode. In this mode, refresh timing and refresh addresses are generated within the synchronous DRAM.

To select self-refreshing, set the RFSHE bit to 1 in REFCR. When a SLEEP instruction is executed to enter software standby mode, the SELF command is issued, as shown in figure 6.57.

When software standby mode is exited, the SLFRF bit in REFCR is cleared to 0 and self-refresh mode is exited automatically. If an auto refresh request occurs when making a transition to software standby mode, auto refreshing is executed, then self-refresh mode is entered.

6.7.15 DMAC and EXDMAC Single Address Transfer Mode and Synchronous DRAM Interface

When burst mode is selected on the synchronous DRAM interface, the $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ output timing can be selected with the DDS and EDDS bits in DRAMCR. When continuous synchronous DRAM space is accessed in DMAC/EXDMAC single address mode at the same time, these bits select whether or not burst access is to be performed. The establishment time for the read data can be extended in the clock suspend mode irrespective of the settings of the DDS and EDDS bits.

(1) Output Timing of $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$

When DDS = 1 or EDDS = 1: Burst access is performed by determining the address only, irrespective of the bus master. With the synchronous DRAM interface, the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output goes low from the T_{c1} state.

Figure 6.60 shows the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output timing for the synchronous DRAM interface when DDS = 1 or EDDS = 1.

6.11.1 Operation

In externally expanded mode, the bus can be released to an external device by setting the BRLE bit to 1 in BCR. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus request to this LSI. When the $\overline{\text{BREQ}}$ pin is sampled, at the prescribed timing the $\overline{\text{BACK}}$ pin is driven low, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus released state.

In the external bus released state, internal bus masters except the EXDMAC can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers initiation of the bus cycle, and waits for the bus request from the external bus master to be canceled. If a refresh request is generated in the external bus released state, or if a SLEEP instruction is executed to place the chip in software standby mode or all-module-clocks-stopped mode, refresh control and software standby or all-module-clocks-stopped control is deferred until the bus request from the external bus master is canceled.

If the BREQOE bit is set to 1 in BCR, the $\overline{\text{BREQO}}$ pin can be driven low when any of the following requests are issued, to request cancellation of the bus request externally.

- When an internal bus master wants to perform an external access
- When a refresh request is generated
- When a SLEEP instruction is executed to place the chip in software standby mode or all-module-clocks-stopped mode

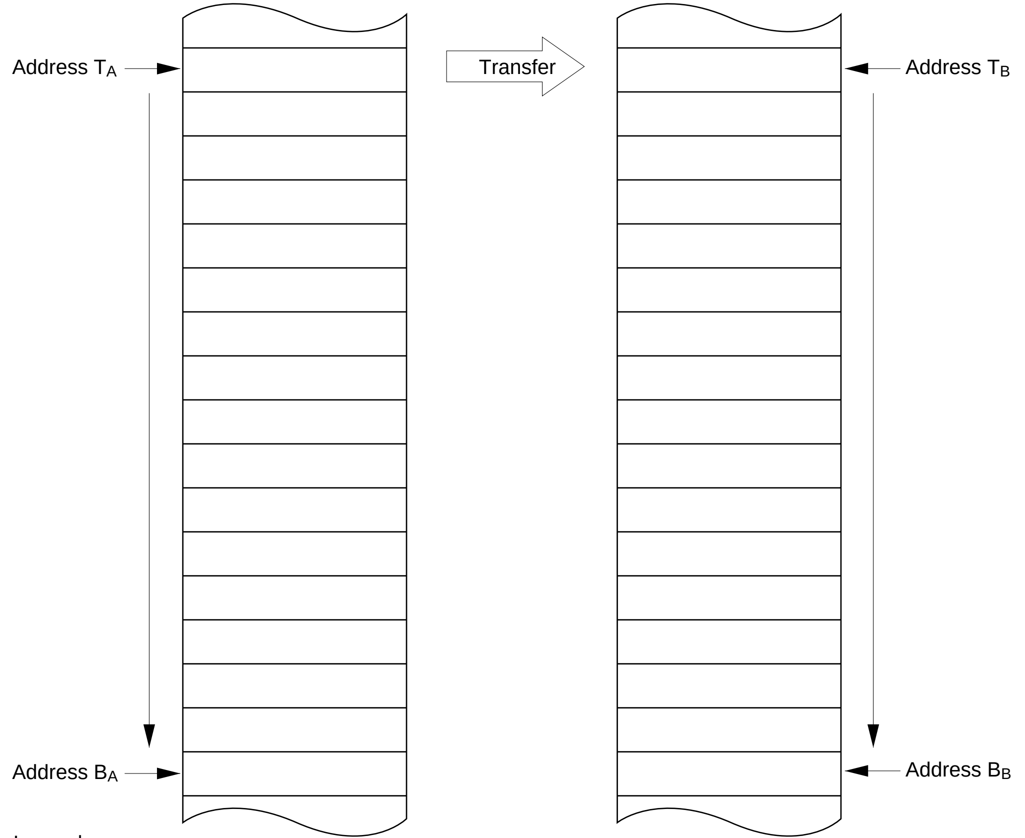
When the $\overline{\text{BREQ}}$ pin is driven high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus released state is terminated.

If an external bus release request and external access occur simultaneously, the order of priority is as follows:

(High) External bus release > External access by internal bus master (Low)

If a refresh request and external bus release request occur simultaneously, the order of priority is as follows:

(High) Refresh > External bus release (Low)



Legend:
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \cdot (-1)^{SAID} \cdot (2^{DTSZ} \cdot (N - 1))$
Address $B_B = L_B + DAIDE \cdot (-1)^{DAID} \cdot (2^{DTSZ} \cdot (N - 1))$
Where: L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRA

Figure 7.11 Operation in Normal Mode

Transfer requests (activation sources) are external requests and auto-requests. With auto-request, the DMAC is only activated by register setting, and the specified number of transfers are performed automatically. With auto-request, cycle steal mode or burst mode can be selected. In cycle steal mode, the bus is released to another bus master each time a transfer is performed. In burst mode, the bus is held continuously until transfer ends.

Figure 7.12 shows an example of the setting procedure for normal mode.

Bit	Bit Name	Initial Value	R/W	Description
12 11 10 9 8	SARA4 SARA3 SARA2 SARA1 SARA0	0 0 0 0 0	R/W R/W R/W R/W R/W	Source Address Repeat Area These bits specify the source address (EDSAR) repeat area. The repeat area function updates the specified lower address bits, leaving the remaining upper address bits always the same. A repeat area size of 2 bytes to 8 Mbytes can be specified. The setting interval is a power-of-two number of bytes. When repeat area overflow results from incrementing or decrementing an address, the lower address is the start address of the repeat area in the case of address incrementing, or the last address of the repeat area in the case of address decrementing. If the SARIE bit is set to 1, an interrupt can be requested when repeat area overflow occurs. 00000: Not designated as repeat area 00001: Lower 1 bit (2-byte area) designated as repeat area 00010: Lower 2 bits (4-byte area) designated as repeat area 00011: Lower 3 bits (8-byte area) designated as repeat area 00100: Lower 4 bits (16-byte area) designated as repeat area : : 10011: Lower 19 bits (512-kbyte area) designated as repeat area 10100: Lower 20 bits (1-Mbyte area) designated as repeat area 10101: Lower 21 bits (2-Mbyte area) designated as repeat area 10110: Lower 22 bits (4-Mbyte area) designated as repeat area 10111: Lower 23 bits (8-Mbyte area) designated as repeat area 11XXX: Setting prohibited

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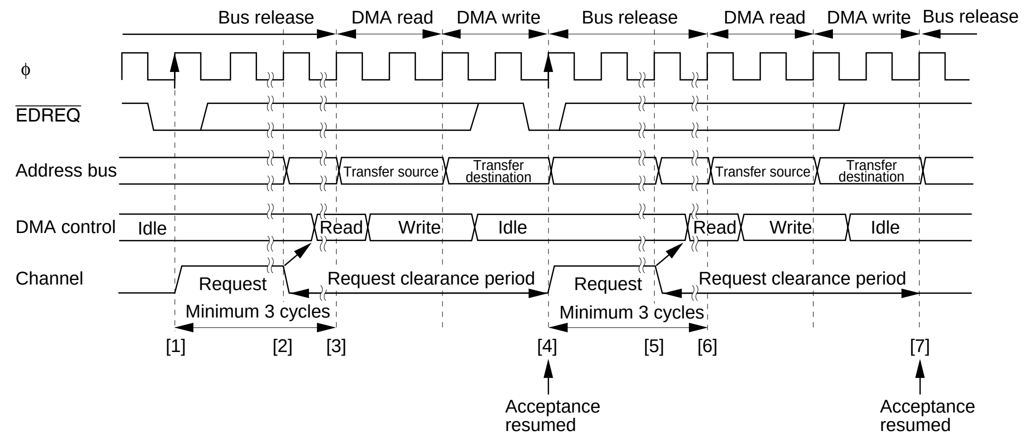
$\overline{\text{EDREQ}}$ Pin Falling Edge Activation Timing: Figure 8.18 shows an example of normal mode transfer activated by the $\overline{\text{EDREQ}}$ pin falling edge.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of φ, and request is held.
[2], [5] Request is cleared at end of next bus cycle, and activation is started in EXDMAC.
[3], [6] DMA cycle start; $\overline{\text{EDREQ}}$ pin high level sampling is started at rise of φ.
[4], [7] When $\overline{\text{EDREQ}}$ pin high level has been sampled, acceptance is resumed after completion of write cycle. (As in [1], $\overline{\text{EDREQ}}$ pin low level is sampled at rise of ø, and request is held.)

Figure 8.18 Example of Normal Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Falling Edge

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of φ after the end of the EDMDR write cycle for setting the transfer-enabled state.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared, and $\overline{\text{EDREQ}}$ pin high level sampling for edge sensing is started. If $\overline{\text{EDREQ}}$ pin high level sampling is completed by the end of the DMA write cycle, acceptance resumes after the end of the write cycle, and $\overline{\text{EDREQ}}$ pin low level sampling is performed again; this sequence of operations is repeated until the end of the transfer.

Figure 8.19 shows an example of block transfer mode transfer activated by the $\overline{\text{EDREQ}}$ pin falling edge.

10.8.4 Pin Functions

Port 8 pins also function as interrupt inputs and EXDMAC I/Os. The correspondence between the register specification and the pin functions is shown below.

- P85/($\overline{\text{IRQ5}}$)/$\overline{\text{EDACK3}}$

  The pin function is switched as shown below according to the combination of bit AMS in EDMDR_3 of the EXDMAC, bit P85DDR, and bit ITS5 in ITSR.

  Modes 1, 2, 3 (EXPE = 1), 4, 5, 6, 7 (EXPE = 1)

AMS	0		1
P85DDR	0	1	—
Pin function	P85 input	P85 output	$\overline{\text{EDACK3}}$ output
	$\overline{\text{IRQ5}}$ interrupt input*		

  Modes 3, 7 (EXPE = 0)

AMS	—	
P85DDR	0	1
Pin function	P85 input	P85 output
	$\overline{\text{IRQ5}}$ interrupt input*	

Note: * $\overline{\text{IRQ5}}$ input when ITS5 = 1.

- P84/($\overline{\text{IRQ4}}$)/$\overline{\text{EDACK2}}$

  The pin function is switched as shown below according to the combination of bit AMS in EDMDR_2 of the EXDMAC, bit P84DDR, and bit ITS4 in ITSR.

  Modes 1, 2, 3*2 (EXPE = 1), 4, 5, 6, 7 (EXPE = 1)

AMS	0		1
P84DDR	0	1	—
Pin function	P84 input	P84 input/output	$\overline{\text{EDACK2}}$ output
	$\overline{\text{IRQ4}}$ interrupt input*1		

10.9.4 Port A Pull-Up MOS Control Register (PAPCR)

PAPCR controls the input pull-up MOS function. Bits 7 to 5 are valid in modes 1, 2, 5, and 6, and all the bits are valid in modes 3*, 4, and 7.

Note: * Only in H8S/2678R Group.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7PCR	0	R/W	When a pin function is specified to an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PA6PCR	0	R/W	
5	PA5PCR	0	R/W	
4	PA4PCR	0	R/W	
3	PA3PCR	0	R/W	
2	PA2PCR	0	R/W	
1	PA1PCR	0	R/W	
0	PA0PCR	0	R/W	

10.9.5 Port A Open Drain Control Register (PAODR)

PAODR specifies an output type of port A.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7ODR	0	R/W	Setting the corresponding bit to 1 specifies a pin output type to NMOS open-drain output, while clearing this bit to 0 specifies that to CMOS output.
6	PA6ODR	0	R/W	
5	PA5ODR	0	R/W	
4	PA4ODR	0	R/W	
3	PA3ODR	0	R/W	
2	PA2ODR	0	R/W	
1	PA1ODR	0	R/W	
0	PA0ODR	0	R/W	

10.9.6 Port Function Control Register 1 (PFCR1)

PFCR1 performs I/O port control. Bits 7 to 5 are valid in modes 1, 2, 5, and 6, and all the bits are valid in modes 3*, 4, and 7.

Note: * Only in H8S/2678R Group.

10.11 Port C

Port C is an 8-bit I/O port that also has other functions. The port C has the following registers.

- Port C data direction register (PCDDR)
- Port C data register (PCDR)
- Port C register (PORTC)
- Port C pull-up MOS control register (PCPCR)

10.11.1 Port C Data Direction Register (PCDDR)

The individual bits of PCDDR specify input or output for the pins of port C.

PCDDR cannot be read; if it is, an undefined value will be read.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>PC7DDR</td><td>0</td><td>W</td><td rowspan="8">• Modes 1, 2, 5, and 6
Port C pins are address outputs regardless of the PCDDR settings.
• Modes 3* (EXPE = 1), 4, and 7 (when EXPE = 1)
Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.
• Modes 3* (EXPE = 1) and 7 (when EXPE = 0)
Port C is an I/O port, and its pin functions can be switched with PCDDR.</td></tr>
<tr><td>6</td><td>PC6DDR</td><td>0</td><td>W</td></tr>
<tr><td>5</td><td>PC5DDR</td><td>0</td><td>W</td></tr>
<tr><td>4</td><td>PC4DDR</td><td>0</td><td>W</td></tr>
<tr><td>3</td><td>PC3DDR</td><td>0</td><td>W</td></tr>
<tr><td>2</td><td>PC2DDR</td><td>0</td><td>W</td></tr>
<tr><td>1</td><td>PC1DDR</td><td>0</td><td>W</td></tr>
<tr><td>0</td><td>PC0DDR</td><td>0</td><td>W</td></tr>
</table>

Note: * Only in H8S/2678R Group.

- PF1/$\overline{\text{UCAS}}$/DQMU*2/$\overline{\text{IRQ14}}$

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bits RMTS2 to RMTS0 in DRAMCR, and bit PF1DDR.

Operating mode	1, 2, 4, 5,			3*2, 7				
EXPE	—			0		1		
Areas 2 to 5	Any of areas 2 to 5 is DRAM space	Areas 2 to 5 are all normal space		—		Any of areas 2 to 5 is DRAM space	Areas 2 to 5 are all normal space	
PF1DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{UCAS}}$ output	PF1 input	PF1 output	PF1 input	PF1 output	$\overline{\text{UCAS}}$ output	PF1 input	PF1 output
	$\overline{\text{IRQ14}}$ interrupt*1							

Notes: 1. $\overline{\text{IRQ14}}$ interrupt input when bit ITS14 is cleared to 0 in ITSR.
2. Only in H8S/2678R Group.

- PF0/$\overline{\text{WAIT}}$

  The pin function is switched as shown below according to the operating mode, bit EXPE, bit WAITE in BCR, and bit PF0DDR.

Operating mode	1, 2, 4, 5, 6			3*, 7				
EXPE	—			0		1		
WAITE	0		1	—		0		1
PF0DDR	0	1	—	0	1	0	1	—
Pin function	PF0 input	PF0 output	$\overline{\text{WAIT}}$ input	PF0 input	PF0 output	PF0 input	PF0 output	$\overline{\text{WAIT}}$ input

Note: * Only in H8S/2678R Group.

Figure 11.19 illustrates the operation when counting upon TCNT_2 overflow/underflow has been set for TCNT_1, and phase counting mode has been designated for channel 2.

TCNT_1 is incremented by TCNT_2 overflow and decremented by TCNT_2 underflow.

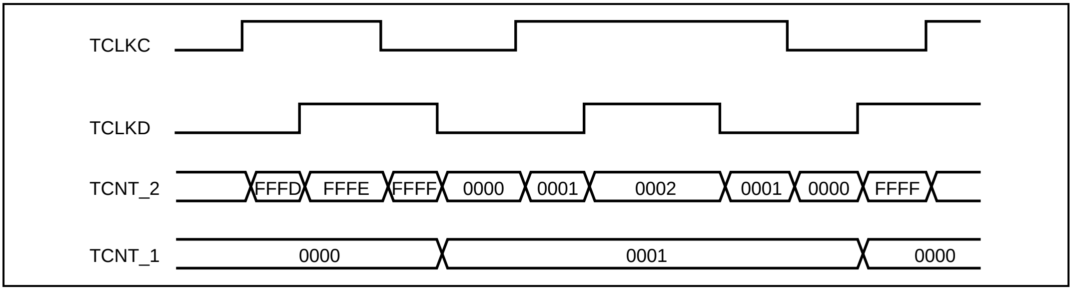


Figure 11.19 Example of Cascaded Operation (2)

11.4.5 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. 0, 1, or toggle output can be selected as the output level in response to compare match of each TGR.

Settings of TGR registers can output a PWM waveform in the range of 0% to 100% duty cycle.

Designating TGR compare match as the counter clearing source enables the cycle to be set in that register. All channels can be designated for PWM mode independently. Synchronous operation is also possible.

There are two PWM modes, as described below.

- PWM mode 1

  PWM output is generated from the TIOCA and TIOCC pins by pairing TGRA with TGRB and TGRC with TGRD. The outputs specified by bits IOA3 to IOA0 and IOC3 to IOC0 in TIOR are output from the TIOCA and TIOCC pins at compare matches A and C, respectively. The outputs specified by bits IOB3 to IOB0 and IOD3 to IOD0 in TIOR are output at compare matches B and D, respectively. The initial output value is the value set in TGRA or TGRC. If the set values of paired TGRs are identical, the output value does not change when a compare match occurs.

  In PWM mode 1, a maximum 8-phase PWM output is possible.

3. Phase counting mode 3

Figure 11.27 shows an example of phase counting mode 3 operation, and table 11.34 summarizes the TCNT up/down-count conditions.

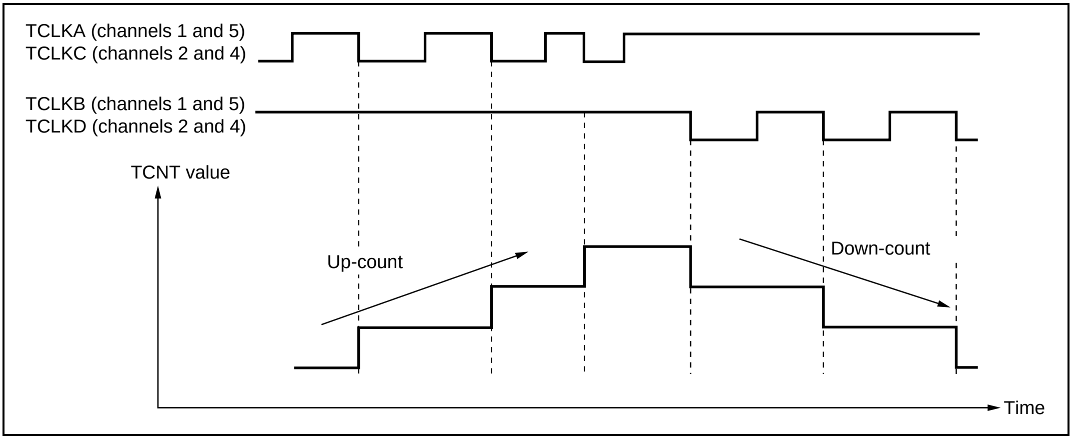


Figure 11.27 Example of Phase Counting Mode 3 Operation

Table 11.34 Up/Down-Count Conditions in Phase Counting Mode 3

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	↑	Don’t care
Low level	↓	
↑	Low level	
↓	High level	Up-count
High level	↓	Down-count
Low level	↑	Don’t care
↑	High level	
↓	Low level	

Legend:

↑ : Rising edge

↓ : Falling edge

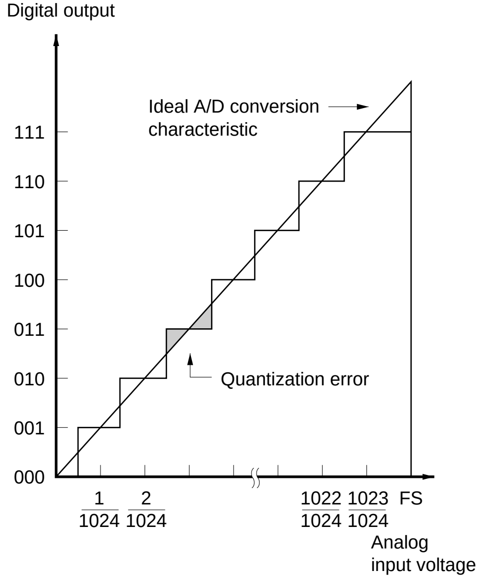


Figure 16.4 A/D Conversion Accuracy Definitions

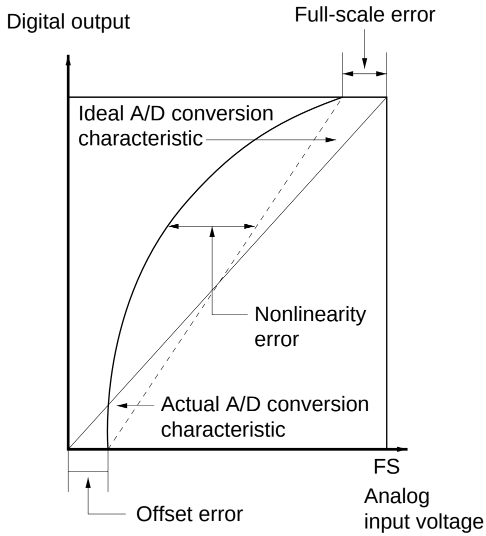


Figure 16.5 A/D Conversion Accuracy Definitions

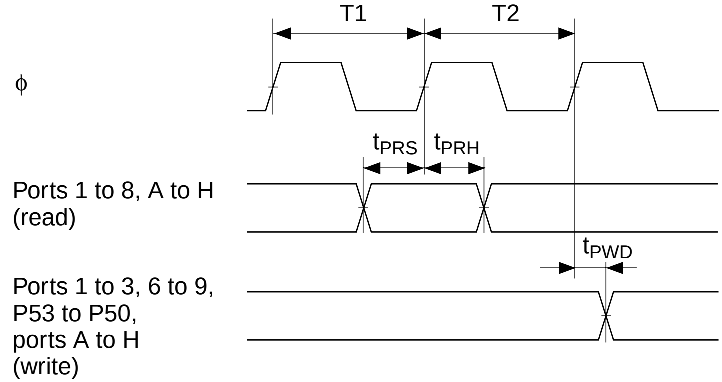


Figure 24.34 I/O Port Input/Output Timing

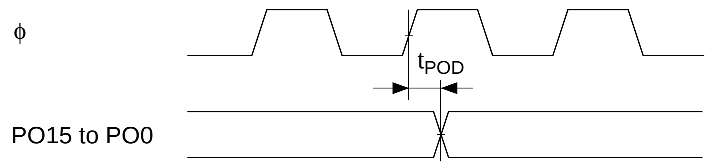
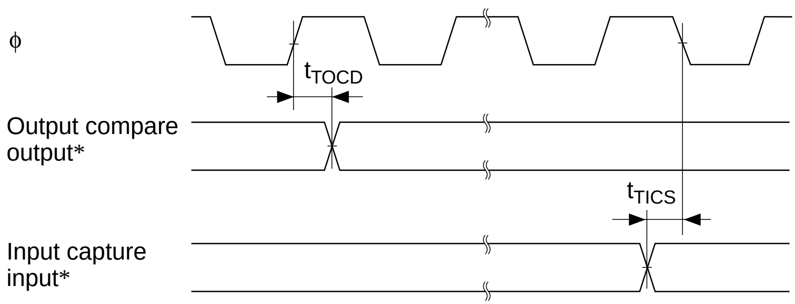


Figure 24.35 PPG Output Timing



Note: * TIOCA0 to TIOCA5, TIOCB0 to TIOCB5, TIOCC0, TIOCC3, TIOCD0, TIOCD3

Figure 24.36 TPU Input/Output Timing

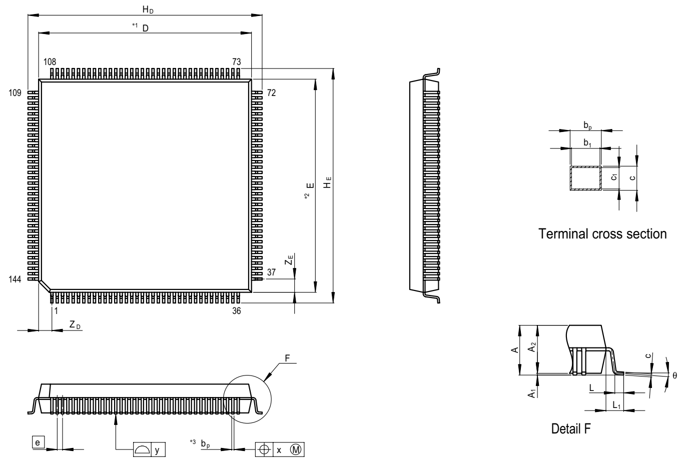
24.6 Flash Memory Characteristics

Table 24.13 Flash Memory Characteristics

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to 75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to 85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*1 *2 *4		t_P		—	10	200	ms/ 128 bytes	
Erase time*1 *3 *6		t_E		—	50	1000	ms/ 128 bytes	
Reprogramming count		N_{WEC}		100*7	10,000*8	—	Times	
Data retention time*9		t_{DRP}		10	—	—	Years	
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after PSU bit setting*1	y		50	—	—	µs	
	Wait time after P bit setting*1 *4	z	z1	—	—	30	µs	1 ≤ n ≤ 6
			z2	—	—	200	µs	7 ≤ n ≤ 1000
			z3	—	—	10	µs	Additional program-ming wait
	Wait time after P bit clearing*1	α		5	—	—	µs	
	Wait time after PSU bit clearing*1	β		5	—	—	µs	
	Wait time after PV bit setting*1	γ		4	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after PV bit clearing*1	η		2	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of writes*1 *4	N		—	—	1000*5	Times	
Erasing	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after ESU bit setting*1	y		100	—	—	µs	
	Wait time after E bit setting*1 *6	z		—	—	10	µs	Erase time wait
	Wait time after E bit clearing*1	α		10	—	—	µs	
	Wait time after ESU bit clearing*1	β		10	—	—	µs	
	Wait time after EV bit setting*1	γ		20	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after EV bit clearing*1	η		4	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of erases*1 *6	N		—	—	100	Times	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP144-20x20-0.50	PRQP0144KA-A	FP-144G/FP-144GV	2.4g



NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	20	—
E	—	20	—
A_2	—	2.70	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	3.05
A_1	0.00	0.10	0.25
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure C.2 Package Dimensions (FP-144G)