Section 1 Overview

1.1 Features

- High-speed H8S/2600 central processing unit with an internal 16-bit architecture
  Upward-compatible with H8/300 and H8/300H CPUs on an object level
  Sixteen 16-bit general registers
  69 basic instructions
- Various peripheral functions
  DMA controller (DMAC)
  EXDMA controller (EXDMAC)
  Data transfer controller (DTC)
  16-bit timer-pulse unit (TPU)
  Programmable pulse generator (PPG)
  8-bit timer (TMR)
  Watchdog timer (WDT)
  Asynchronous or clocked synchronous serial communication interface (SCI)
  10-bit A/D converter
  8-bit D/A converter
  Clock pulse generator
- On-chip memory

ROM Type	Model	ROM	RAM
Flash memory version	HD64F2676	256 kbytes	8 kbytes
Masked ROM version	HD6432676	256 kbytes	8 kbytes
	HD6432675	128 kbytes	8 kbytes
	HD6432673	64 kbytes	8 kbytes
ROMless version	HD6412674R	—	32 kbytes
	HD6412670	—	8 kbytes

- General I/O ports
  I/O pins: 103
  Input-only pins: 12
- Supports various power-down states

Table 19.6 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate Is Possible

Host Bit Rate	System Clock Frequency Range of LSI
19,200 bps	8 to 25 MHz
9,600 bps	8 to 25 MHz

19.6.2 User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the program/erase program or a program which provides the program/erase program from external memory. Because the flash memory itself cannot be read during programming/erasing, transfer the program/erase program to on-chip RAM, as like in boot mode. Figure 19.7 shows a sample procedure for programming/erasing in user program mode. Prepare a program/erase program in accordance with the description in section 19.8, Flash Memory Programming/Erasing.

Section 20 Masked ROM

This Group microcomputer has 64, 128, or 256 kbytes of on-chip masked ROM. The on-chip ROM is connected to the CPU, data transfer controller (DTC), and DMA controller (DMAC) with a 16-bit data bus. The on-chip ROM can be accessed by the CPU, DTC, and DMAC in 8 or 16-bit units. The data in the on-chip ROM can always be accessed in one state.

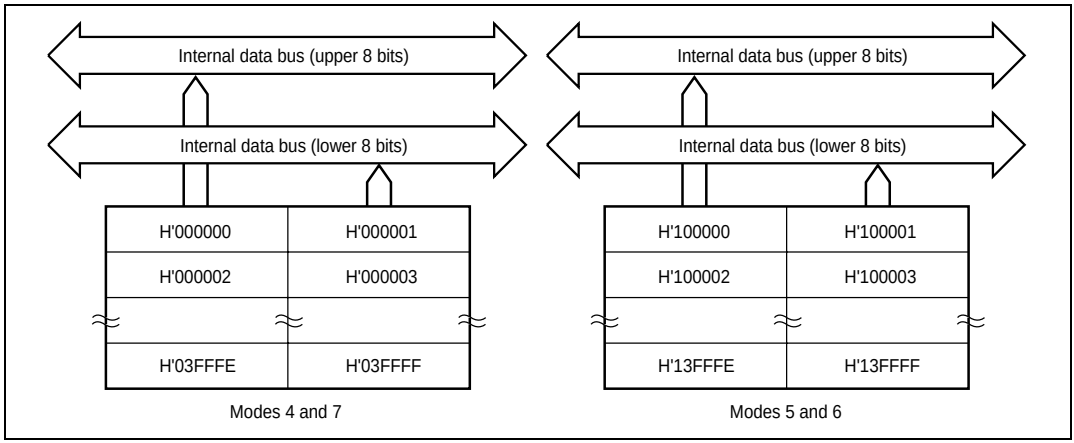

Figure 20.1 Block Diagram of 256-kbyte Masked ROM (HD6432676)

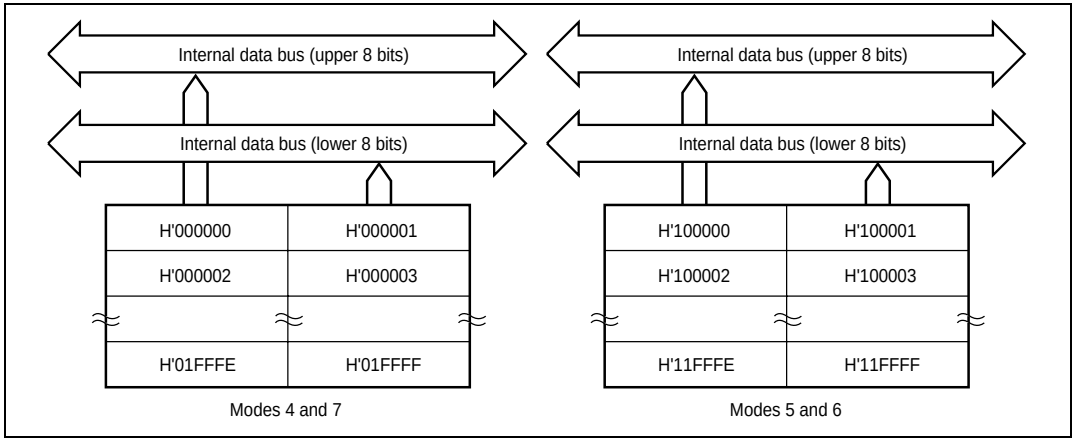

Figure 20.2 Block Diagram of 128-kbyte Masked ROM (HD6432675)

Bit	Bit Name	Initial Value	R/W	Description
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select the division ratio.
0	SCK0	0	R/W	000: 1/1
				001: 1/2
				010: 1/4
				011: 1/8
				100: 1/16
				101: 1/32
				11X: Setting prohibited

Legend: X: Don't care

21.1.2 PLL Control Register (PLLCR)

PLLCR sets the frequency multiplication factor used by the PLL circuit.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.
3	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.
2	—	0	R/W	Reserved This bit is always read as 0 and cannot be modified.
1	STC1	0	R/W	Frequency Multiplication Factor
0	STC0	0	R/W	The STC bits specify the frequency multiplication factor used by the PLL circuit.
				00: × 1
				01: × 2
				10: × 4
				11: Setting prohibited

Register Abbreviation	Reset	High-Speed	Clock Division	Sleep	Module Stop	All Module Clock Stop	Software Standby	Hardware Standby	Module
PORT7	—	—	—	—	—	—	—	—	PORT
PORT8	—	—	—	—	—	—	—	—	
PORTA	—	—	—	—	—	—	—	—	
PORTB	—	—	—	—	—	—	—	—	
PORTC	—	—	—	—	—	—	—	—	
PORTD	—	—	—	—	—	—	—	—	
PORTE	—	—	—	—	—	—	—	—	
PORTF	—	—	—	—	—	—	—	—	
PORTG	—	—	—	—	—	—	—	—	
P1DR	Initialized	—	—	—	—	—	Initialized	—	
P2DR	Initialized	—	—	—	—	—	Initialized	—	
P3DR	Initialized	—	—	—	—	—	Initialized	—	
P5DR	Initialized	—	—	—	—	—	Initialized	—	
P6DR	Initialized	—	—	—	—	—	Initialized	—	
P7DR	Initialized	—	—	—	—	—	Initialized	—	
P8DR	Initialized	—	—	—	—	—	Initialized	—	
PADR	Initialized	—	—	—	—	—	Initialized	—	
PBDR	Initialized	—	—	—	—	—	Initialized	—	
PCDR	Initialized	—	—	—	—	—	Initialized	—	
PDDR	Initialized	—	—	—	—	—	Initialized	—	
PEDR	Initialized	—	—	—	—	—	Initialized	—	
PFDR	Initialized	—	—	—	—	—	Initialized	—	
PGDR	Initialized	—	—	—	—	—	Initialized	—	
PORTH	Initialized	—	—	—	—	—	—	—	
PHDR	Initialized	—	—	—	—	—	Initialized	—	
PHDDR	Initialized	—	—	—	—	—	Initialized	—	
SMR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	SCI_0
BRR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	
SCR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	
TDR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	
SSR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	
RDR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	
SCMR_0	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	

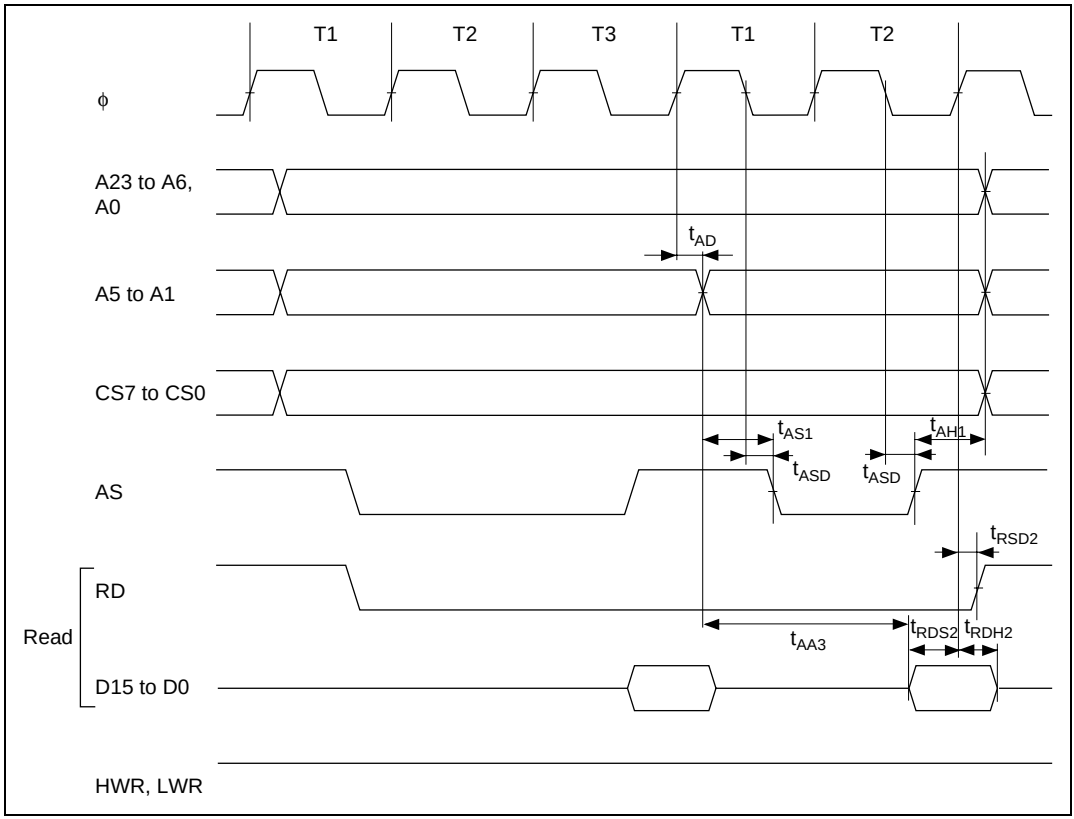

Figure 24.13 Burst ROM Access Timing: Two-State Burst Access