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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	IrDA, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2676vfc33v

Section 13 8-Bit Timers (TMR)

Section 14 Watchdog Timer

Section 15 Serial Communication Interface (SCI, IrDA)

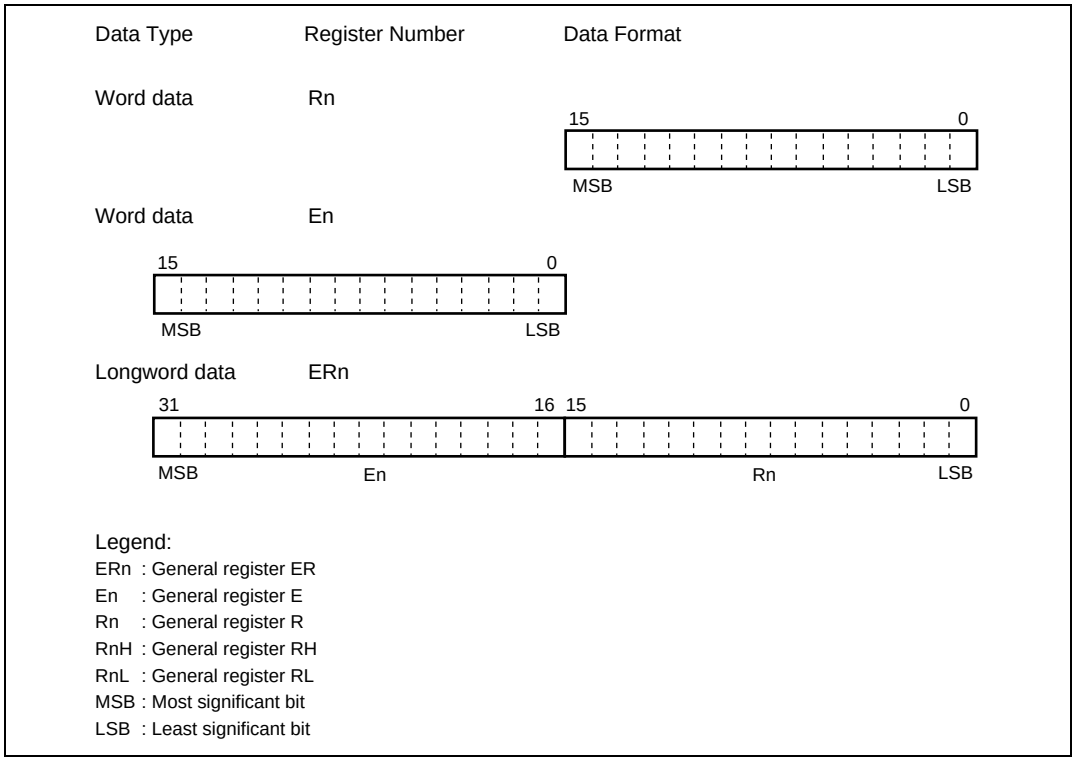


Figure 2.9 General Register Data Formats (2)

Bit	Bit Name	Initial Value	R/W	Descriptions
3	FLSHE	0	R/W	Flash Memory Control Register Enable Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). If this bit is set to 1, the flash memory control registers can be read/written to. If this bit is cleared to 0, the flash memory control registers are not selected. At this time, the contents of the flash memory control registers are maintained. This bit should be written to 0 other than flash memory version. 0: Flash memory control registers are not selected for area H'FFFFC8 to H'FFFFCB 1: Flash memory control registers are selected for area H'FFFFC8 to H'FFFFCB
2	—	0	—	Reserved This bit is always read as 0 and cannot be modified.
1	EXPE	—	R/W	External Bus Mode Enable Sets external bus mode. In modes 1, 2, and 4 to 6, this bit is fixed at 1 and cannot be modified. In mode 3* and 7, this bit has an initial value of 0, and can be read and written. Writing of 0 to EXPE when its value is 1 should only be carried out when an external bus cycle is not being executed. 0: External bus disabled 1: External bus enabled
0	RAME	1	R/W	RAM Enable Enables or disables the on-chip RAM. The RAME bit is initialized when the reset status is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

Note: * Mode 3 is available only in the F-ZTAT version of H8S/2678R Group.

Bit	Bit Name	Initial Value	R/W	Description
10	ICIS0	1	R/W	Idle Cycle Insert 0 When an external read cycle and external write cycle are performed consecutively, an idle cycle can be inserted between the bus cycles. 0: Idle cycle not inserted 1: Idle cycle inserted
9	WDBE	0	R/W	Write Data Buffer Enable The write data buffer function can be used for an external write cycle or DMAC single address transfer cycle. 0: Write data buffer function not used 1: Write data buffer function used
8	WAITE	0	R/W	$\overline{\text{WAIT}}$ Pin Enable Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin. 0: Wait input by $\overline{\text{WAIT}}$ pin disabled $\overline{\text{WAIT}}$ pin can be used as I/O port 1: Wait input by $\overline{\text{WAIT}}$ pin enabled
7 to 3	—	0	R/W	Reserved These are readable/writable bits, but the write value should always be 0.
2	ICIS2	0	R/W	Idle Cycle Insert 2 When an external write cycle and external read cycle are performed consecutively, an idle cycle can be inserted between the bus cycles. 0: Idle cycle not inserted 1: Idle cycle inserted Note: Bit 2 is a reserved bit in the H8S/2678 Group. This bit is readable/writable, but the write value should always be 0.
1, 0	—	All 0	R/W	Reserved These bits can be read from or written to. However, the write value should always be 0.

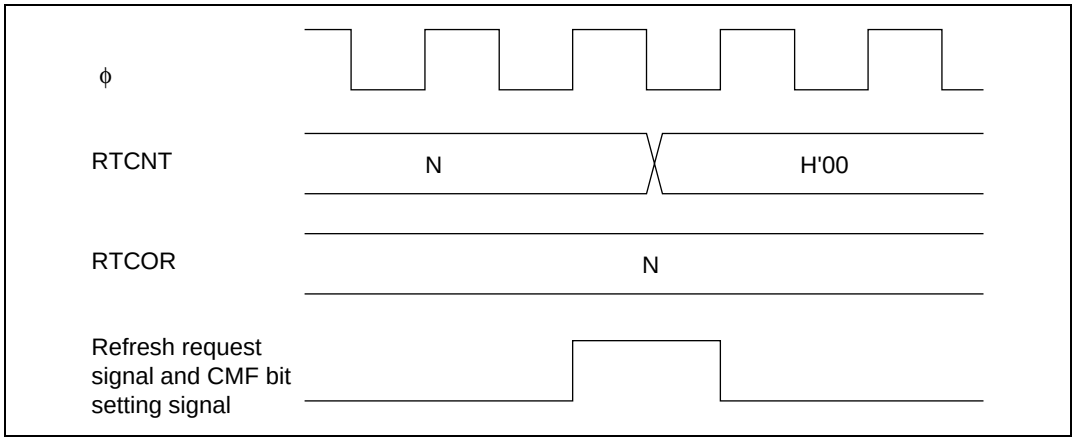


Figure 6.35 Compare Match Timing

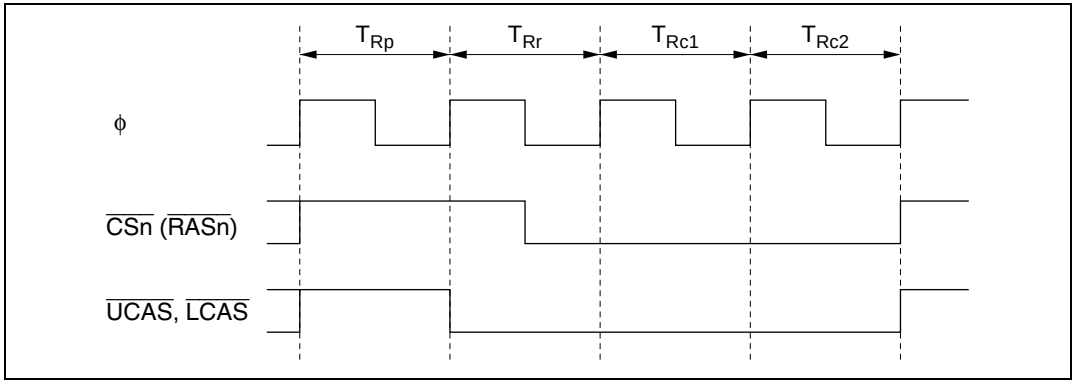


Figure 6.36 CBR Refresh Timing

A setting can be made in bits RCW1 and RCW0 in REFCR to delay $\overline{\text{RAS}}$ signal output by one to three cycles. Use bits RLW1 and RLW0 in REFCR to adjust the width of the $\overline{\text{RAS}}$ signal. The settings of bits RCW1, RCW0, RLW1, and RLW0 are valid only in refresh operations.

Figure 6.37 shows the timing when bits RCW1 and RCW0 are set.

Section 8 EXDMA Controller

This LSI has a built-in four-channel external bus transfer DMA controller (EXDMAC). The EXDMAC can carry out high-speed data transfer, in place of the CPU, to and from external devices and external memory with a DACK (DMA transfer notification) facility.

8.1 Features

- Direct specification of 16-Mbyte address space
- Selection of byte or word transfer data length
- Maximum number of transfers: 16M (16,777,215)/infinite (free-running)
- Selection of dual address mode or single address mode
- Selection of cycle steal mode or burst mode as bus mode
- Selection of normal mode or block transfer mode as transfer mode
- Two kinds of transfer requests: external request and auto-request
- An interrupt request can be sent to the CPU at the end of the specified number of transfers.
- Repeat area designation function:
- Operation in parallel with internal bus master:
- Acceptance of a transfer request and the start of transfer processing can be reported to an external device via the $\overline{\text{EDRAK}}$ pin.
- Module stop mode can be set.

Figure 8.1 shows a block diagram of the EXDMAC.

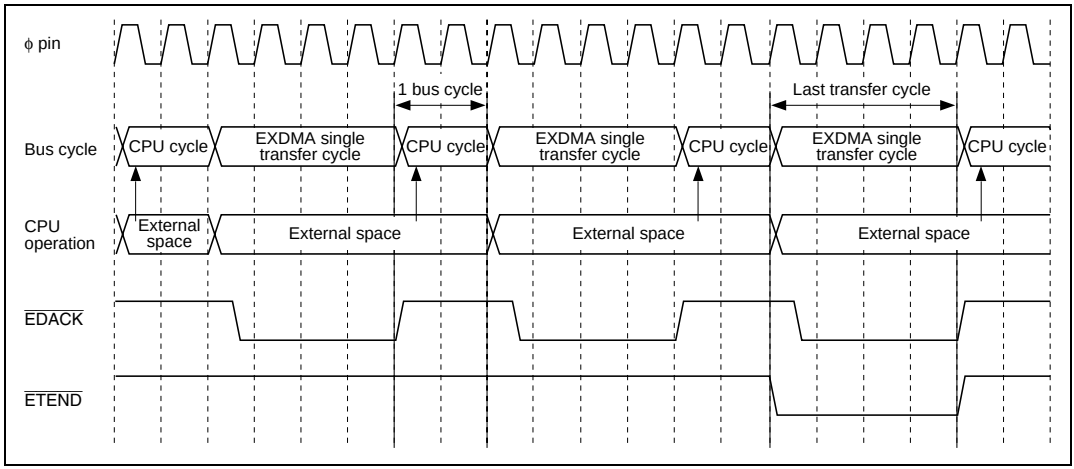


Figure 8.29 Auto Request/Cycle Steal Mode/Normal Transfer Mode (CPU Cycles/Single Address Mode)

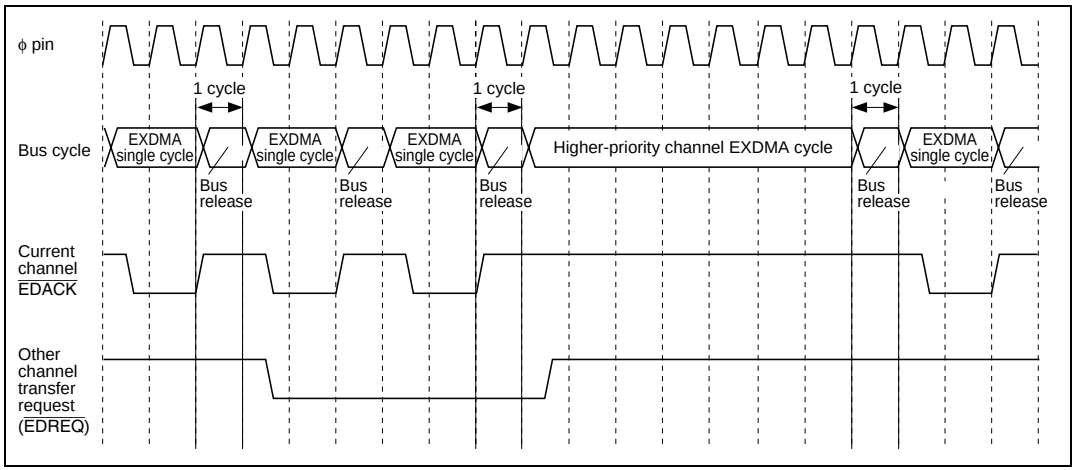


Figure 8.30 Auto Request/Cycle Steal Mode/Normal Transfer Mode (Contention with Another Channel/Single Address Mode)

- P56/AN14/DA2/$\overline{\text{IRQ6}}$

  The pin function is switched as shown below according to bit ITS6 in ITSR.

Pin function	$\overline{\text{IRQ6}}$ interrupt input pin*
	AN14 input
	DA2 output

Note: * $\overline{\text{IRQ6}}$ input when ITS6 = 0.

- P55/AN13/$\overline{\text{IRQ5}}$

  The pin function is switched as shown below according to bit ITS5 in ITSR.

Pin function	$\overline{\text{IRQ5}}$ interrupt input*
	AN13 input

Note: * $\overline{\text{IRQ5}}$ input when ITS5 = 0.

- P54/AN12/$\overline{\text{IRQ4}}$

  The pin function is switched as shown below according to bit ITS4 in ITSR.

Pin function	$\overline{\text{IRQ4}}$ interrupt input*
	AN12 input

Note: * $\overline{\text{IRQ4}}$ input when ITS4 = 0.

- P53/ADTRG/IRQ3

  The pin function is switched as shown below according to the combination of bits TRGS1 and TRGS0 in the A/D control register (ADCR), bit ITS3 in ITSR, and bit P53DDR.

P53DDR	0	1
Pin function	P53 input	P53 output
	$\overline{\text{ADTRG}}$ input*1	
	$\overline{\text{IRQ3}}$ interrupt input*2	

Notes: 1. $\overline{\text{ADTRG}}$ input when TRGS1 = TRGS0 = 0.
2. $\overline{\text{IRQ3}}$ input when ITS3 = 0.

10.11 Port C

Port C is an 8-bit I/O port that also has other functions. The port C has the following registers.

- Port C data direction register (PCDDR)
- Port C data register (PCDR)
- Port C register (PORTC)
- Port C pull-up MOS control register (PCPCR)

10.11.1 Port C Data Direction Register (PCDDR)

The individual bits of PCDDR specify input or output for the pins of port C.

PCDDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PC7DDR	0	W	• Modes 1, 2, 5, and 6 Port C pins are address outputs regardless of the PCDDR settings. • Modes 3* (EXPE = 1), 4, and 7 (when EXPE = 1) Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port. • Modes 3* (EXPE = 1) and 7 (when EXPE = 0) Port C is an I/O port, and its pin functions can be switched with PCDDR.
6	PC6DDR	0	W	
5	PC5DDR	0	W	
4	PC4DDR	0	W	
3	PC3DDR	0	W	
2	PC2DDR	0	W	
1	PC1DDR	0	W	
0	PC0DDR	0	W	

Note: * Only in H8S/2678R Group.

11.10.12 Contention between TCNT Write and Overflow/Underflow

If there is an up-count or down-count in the T2 state of a TCNT write cycle, when overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 11.53 shows the operation timing when there is contention between TCNT write and overflow.

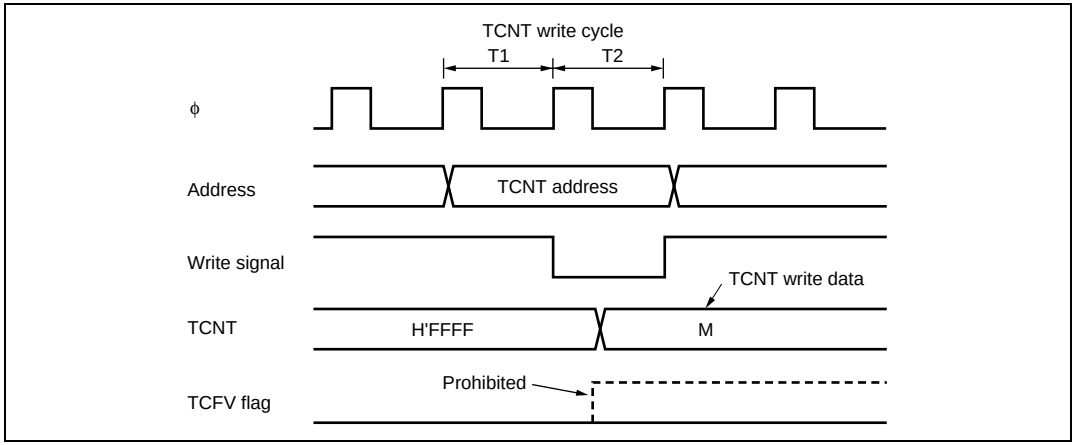


Figure 11.53 Contention between TCNT Write and Overflow

11.10.13 Multiplexing of I/O Pins

In this LSI, the TCLKA input pin is multiplexed with the TIOCC0 I/O pin, the TCLKB input pin with the TIOCD0 I/O pin, the TCLKC input pin with the TIOCB1 I/O pin, and the TCLKD input pin with the TIOCB2 I/O pin. When an external clock is input, compare match output should not be performed from a multiplexed pin.

11.10.14 Interrupts and Module Stop Mode

If module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DMAC or DTC activation source. Interrupts should therefore be disabled before entering module stop mode.

13.8 Usage Notes

13.8.1 Contention between TCNT Write and Clear

If a timer counter clock pulse is generated during the T_2 state of a TCNT write cycle, the clear takes priority, so that the counter is cleared and the write is not performed.

Figure 13.10 shows this operation.

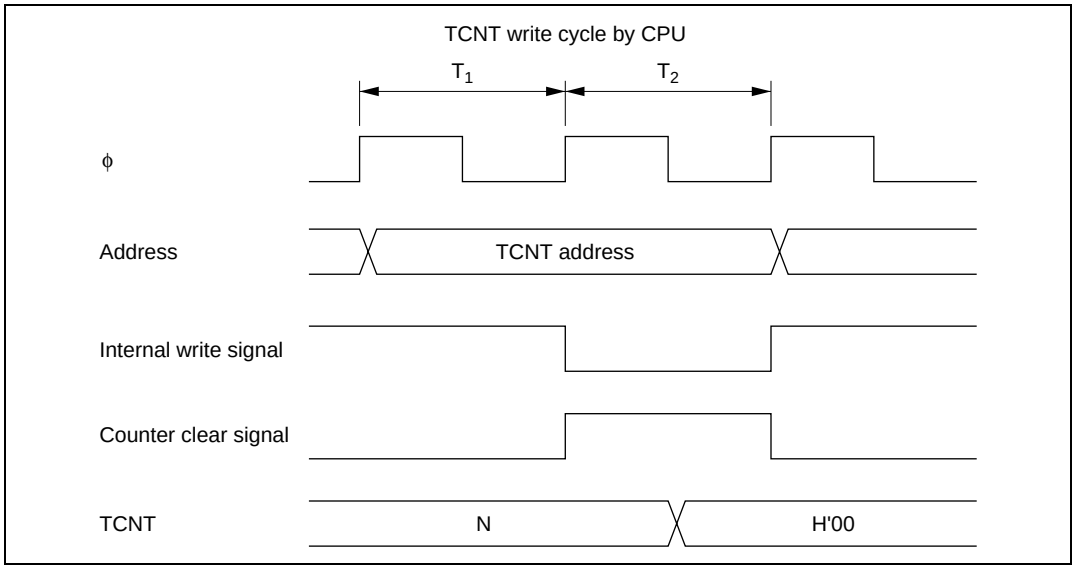
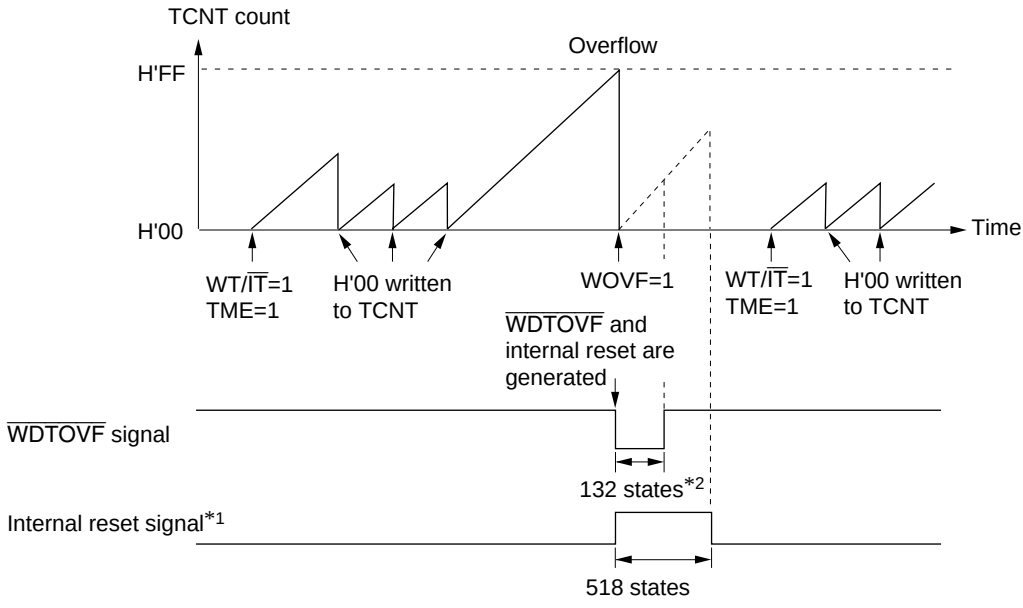


Figure 13.10 Contention between TCNT Write and Clear



Legend:
WT/$\overline{IT}$: Timer mode select bit
TME : Timer enable bit

Notes: 1. If TCNT overflows when the RSTE bit is set to 1, an internal reset signal is generated.
2. 130 states when the RSTE bit is cleared to 0.

Figure 14.2 Operation in Watchdog Timer Mode

14.4.2 Interval Timer Mode

To use the WDT as an interval timer, set the WT/$\overline{IT}$ bit to 0 and TME bit in TCSR to 1.

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. Therefore, an interrupt can be generated at intervals.

When the TCNT overflows in interval timer mode, an interval timer interrupt (WOVI) is requested at the same time the OVF bit in the TCSR is set to 1.

15.4.5 Data Transmission (Asynchronous Mode)

Figure 15.6 shows an example of the operation for transmission in asynchronous mode. In transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if is cleared to 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a transmit data empty interrupt request (TXI) is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. Data is sent from the TxD pin in the following order: start bit, transmit data, parity bit or multiprocessor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks the TDRE flag at the timing for sending the stop bit.
5. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
6. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the “mark state” is entered in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated.

Figure 15.7 shows a sample flowchart for transmission in asynchronous mode.

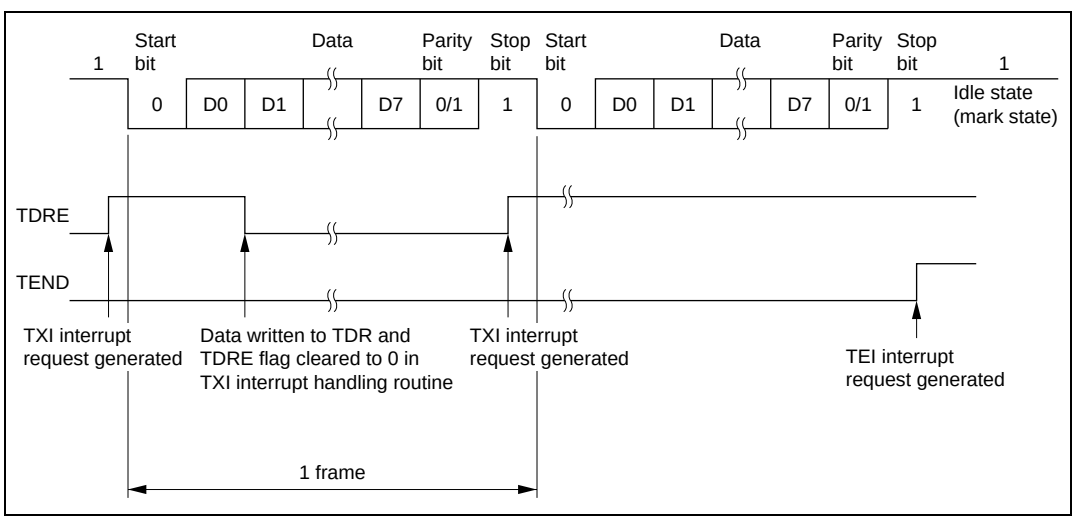


Figure 15.6 Example of Operation in Transmission in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)

Section 19 Flash Memory (F-ZTAT Version)

The features of the flash memory included in the flash memory version are summarized below. The block diagram of the flash memory is shown in figure 19.1.

19.1 Features

- Size

Product Classification		ROM Size	ROM Address
H8S/2678 Group	HD64F2676	256 kbytes	H'000000 to H'03FFFF (Modes 3, 4, 7, 10, and 11) H'100000 to H'13FFFF (Modes 5, 6, 13, and 14)

- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erase is performed in single-block units. The flash memory of 384 kbytes is configured as follows: 64 kbytes × 5 blocks, 32 kbytes × 1 block, and 4 kbytes × 8 blocks. The 256-kbyte flash memory is configured as follows: 64 kbytes × 3 blocks, 32 kbytes × 1 block, and 4 kbytes × 8 blocks. To erase the entire flash memory, each block must be erased in turn.
- Reprogramming capability

  The flash memory can be reprogrammed up to 100 times.
- Two on-board programming modes

  Boot mode

  User program mode

  On-board programming/erasing can be done in boot mode in which the on-chip boot program is started for erase or programming of the entire flash memory. In normal user program mode, individual blocks can be erased or programmed.
- Programmer mode

  Flash memory can be programmed/erased in programmer mode, using a PROM programmer, as well as in on-board programming mode.
- Automatic bit rate adjustment

  With data transfer in boot mode, the bit rate of this LSI can be automatically adjusted to match the transfer bit rate of the host.
- Flash memory emulation by RAM

  Part of the RAM area can be overlapped onto flash memory, to emulate flash memory updates in real time.

3. Block area EB0 contains the vector table. When performing RAM emulation, the vector table is needed in the overlap RAM.

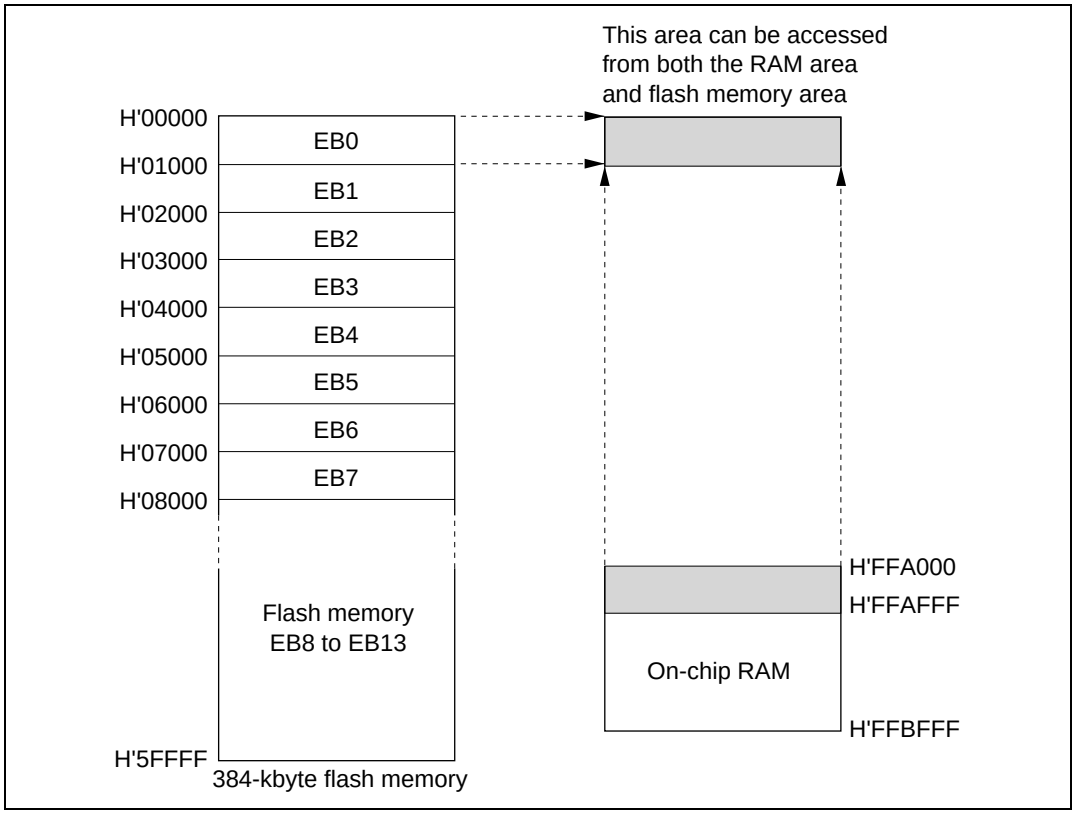


Figure 19.9 Example of RAM Overlap Operation

19.8 Flash Memory Programming/Erasing

A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. Depending on the FLMCR1 and FLMCR2 setting, the flash memory operates in one of the following four modes: program mode, erase mode, program-verify mode, and erase-verify mode. The programming control program in boot mode and the user program/erase program in user mode use these operating modes in combination to perform programming/erasing. Flash memory programming and erasing should be performed in accordance with the descriptions in section 19.8.1, Program/Program-Verify, and section 19.8.2, Erase/Erase-Verify, respectively.

MSTPCRL

Bit	Bit Name	Initial Value	R/W	Module
7	MSTP7	1	R/W	—
6	MSTP6	1	R/W	A/D converter
5	MSTP5	1	R/W	—
4	MSTP4	1	R/W	—
3	MSTP3	1	R/W	Serial communication interface 2 (SCI_2)
2	MSTP2	1	R/W	Serial communication interface 1 (SCI_1)
1	MSTP1	1	R/W	Serial communication interface 0 (SCI_0)
0	MSTP0	1	R/W	8-bit timer (TMR)

22.2 Operation

22.2.1 Clock Division Mode

When bits SCK2 to SCK0 in SCKCR are set to a value from 001 to 101, a transition is made to clock division mode at the end of the bus cycle. In clock division mode, the CPU, bus masters, and on-chip peripheral functions all operate on the operating clock (1/2, 1/4, 1/8, 1/16, or 1/32) specified by bits SCK2 to SCK0.

Clock division mode is cleared by clearing all of bits SCK2 to SCK0 to 0. A transition is made to high-speed mode at the end of the bus cycle, and clock division mode is cleared.

If a SLEEP instruction is executed while the SSBY bit in SBYCR is cleared to 0, the chip enters sleep mode. When sleep mode is cleared by an interrupt, clock division mode is restored.

If a SLEEP instruction is executed while the SSBY bit in SBYCR is set to 1, the chip enters software standby mode. When software standby mode is cleared by an external interrupt, clock division mode is restored.

When the $\overline{\text{RES}}$ pin is driven low, the reset state is entered and clock division mode is cleared. The same applies to a reset caused by watchdog timer overflow.

When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

Register Name	Abbreviation	Bit No.	Address	Module	Data Width	Access States
Timer general register B_0	TGRB_0	16	H'FFDA	TPU_0	16	2
Timer general register C_0	TGRC_0	16	H'FFDC	TPU_0	16	2
Timer general register D_0	TGRD_0	16	H'FFDE	TPU_0	16	2
Timer control register_1	TCR_1	8	H'FFE0	TPU_1	16	2
Timer mode register_1	TMDR_1	8	H'FFE1	TPU_1	16	2
Timer I/O control register_1	TIOR_1	8	H'FFE2	TPU_1	16	2
Timer interrupt enable register_1	TIER_1	8	H'FFE4	TPU_1	16	2
Timer status register_1	TSR_1	8	H'FFE5	TPU_1	16	2
Timer counter_1	TCNT_1	16	H'FFE6	TPU_1	16	2
Timer general register A_1	TGRA_1	16	H'FFE8	TPU_1	16	2
Timer general register B_1	TGRB_1	16	H'FFEA	TPU_1	16	2
Timer control register_2	TCR_2	8	H'FFF0	TPU_2	16	2
Timer mode register_2	TMDR_2	8	H'FFF1	TPU_2	16	2
Timer I/O control register_2	TIOR_2	8	H'FFF2	TPU_2	16	2
Timer interrupt enable register_2	TIER_2	8	H'FFF4	TPU_2	16	2
Timer status rgister_2	TSR_2	8	H'FFF5	TPU_2	16	2
Timer counter_2	TCNT_2	16	H'FFF6	TPU_2	16	2
Timer general register A_2	TGRA_2	16	H'FFF8	TPU_2	16	2
Timer general register B_2	TGRB_2	16	H'FFFA	TPU_2	16	2

Notes: 1. Not available in the H8S/2678 Group.

2. In the H8S/2678 Group: 8 bits, in the H8S/2678R Group: 16 bits.
3. Register of the flash memory version. Not available in the masked ROM version and ROM-less version.
4. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.
5. For writing, refer to section 14.6.1, Notes on Register Access.

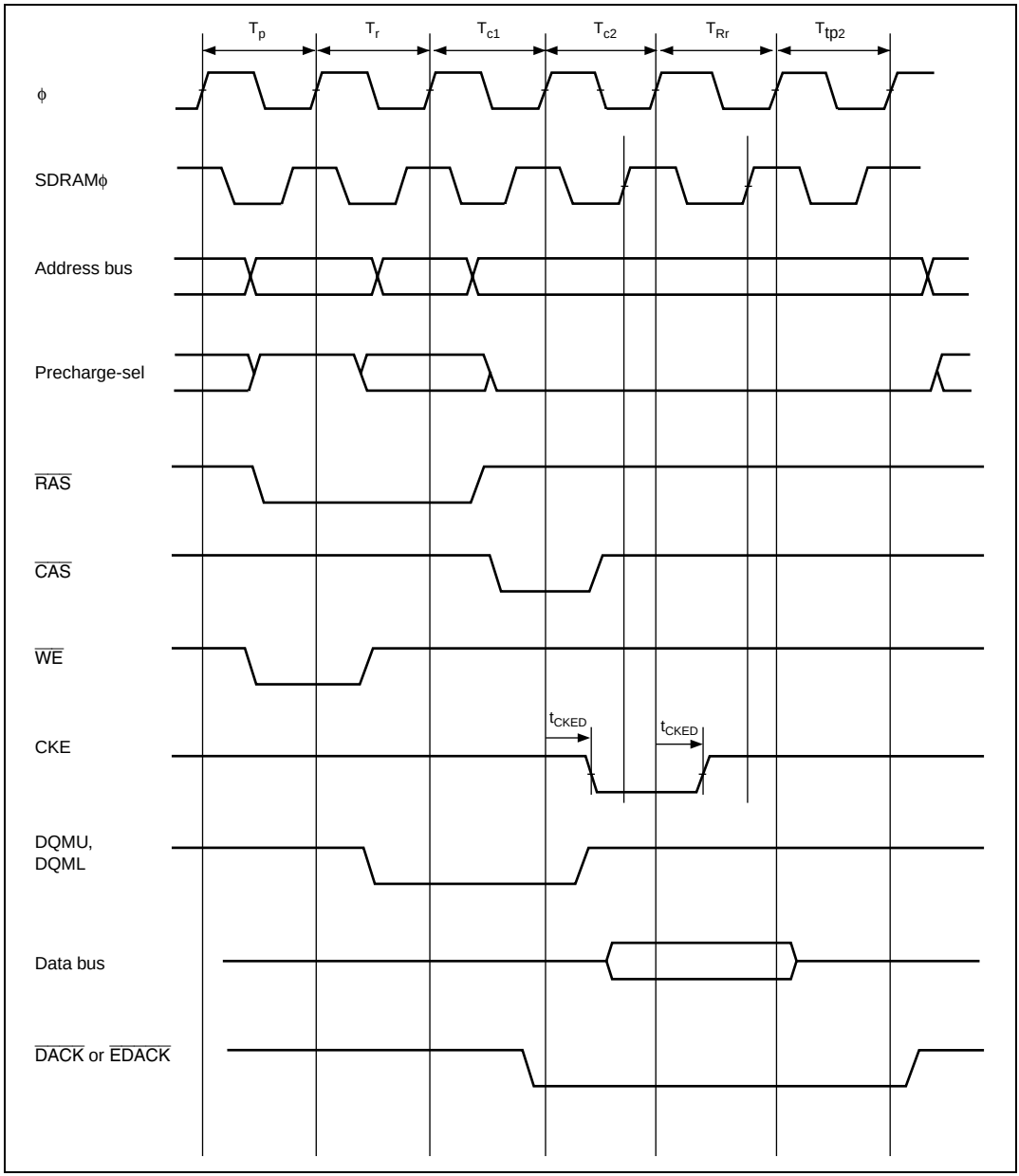


Figure 24.28 Read Data: Two-State Expansion (CAS Latency 2)

Note: Not supported in the H8S/2678 Group.

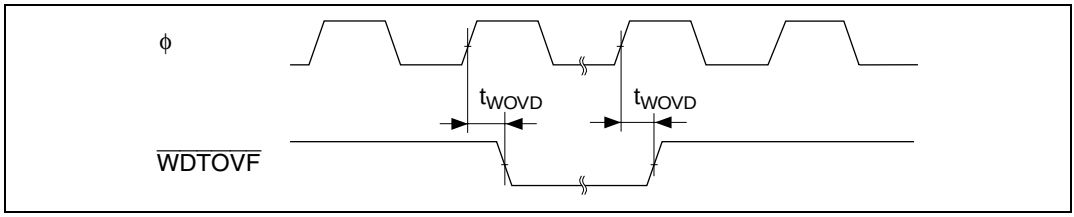


Figure 24.41 WDT Output Timing

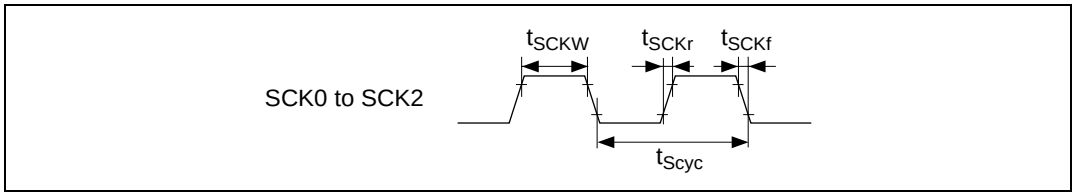


Figure 24.42 SCK Clock Input Timing

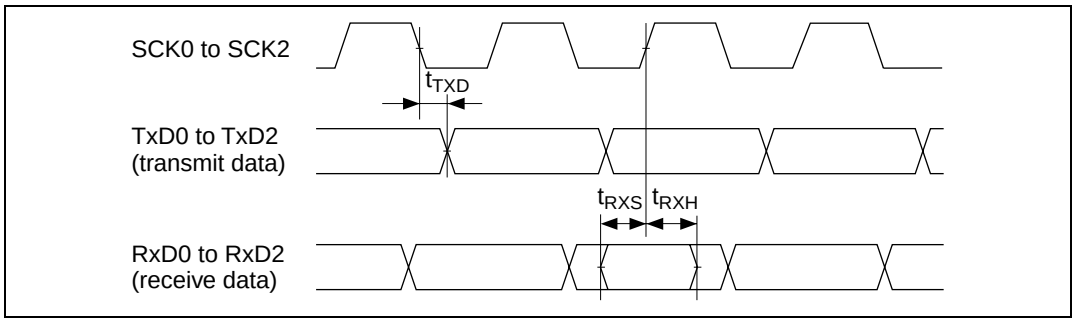


Figure 24.43 SCI Input/Output Timing: Synchronous Mode

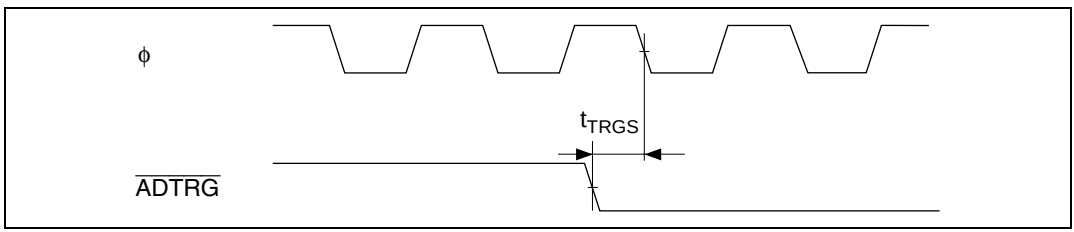


Figure 24.44 A/D Converter External Trigger Input Timing