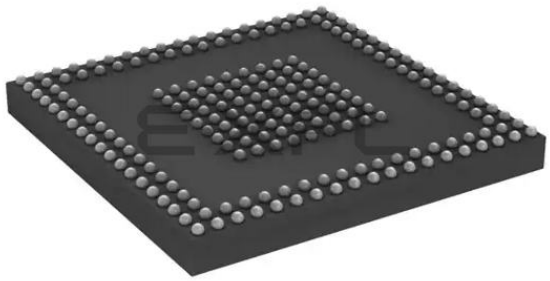

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 12-Core
Speed	800MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	90
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.90V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	217-LFBGA
Supplier Device Package	217-FBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-a12a-128-fb217-i8

2 XS1-A12A-128-FB217 Features

- **Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - 12 real-time logical cores on 2 xCORE tiles
  - Cores share up to 1000 MIPS
  - Each logical core has:
    - Guaranteed throughput of between 1/4 and 1/6 of tile MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **12b 1MSPS 8-channel SAR Analog-to-Digital Converter**
- **1 x LDO**
- **2 x DC-DC converters and Power Management Unit**
- **Watchdog Timer**
- **Onchip clocks/oscillators**
  - Crystal oscillator
  - 20MHz/31kHz silicon oscillators
- **Programmable I/O**
  - 90 general-purpose I/O pins, configurable as input or output
    - Up to 32 x 1bit port, 12 x 4bit port, 8 x 8bit port, 4 x 16bit port
    - 4 xCONNECT links
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 64 channel ends for communication with other cores, on or off-chip
- **Memory**
  - 128KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
  - 16KB internal OTP (max 8KB per tile) for application boot code
  - 128 bytes Deep Sleep Memory
- **Hardware resources**
  - 12 clock blocks (6 per tile)
  - 20 timers (10 per tile)
  - 8 locks (4 per tile)
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0°C to 70°C
  - Industrial qualification: -40°C to 85°C
- **Speed Grade**
  - 10: 1000 MIPS
  - 8: 800 MIPS
- **Power Consumption (typical)**
  - 600 mW at 500 MHz (typical)
  - Sleep Mode: 500 µW
- **217-pin FBGA package 0.8 mm pitch**

3 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	X0D00	X0D02	X0D04	X0D06	X0D08	X0D10	X0D12	X0D14	X0D16	X0D18	X0D20	X0D22	X0D24	X0D25	X0D26	X0D28	X0D30	X0D32	VDDIO_OUT
B	X0D01	X0D03	X0D05	X0D07	X0D09	X0D11	X0D13	X0D15	X0D17	X0D19	X0D21	X0D23	X0D70	ADC_SAMPLE	X0D27	X0D29	X0D31	X0D33	X0D36
C	TDO	DEBUG_N																X0D38	X0D37
D	TCK	RST_N																X0D40	X0D39
E	TMS	TDI																X0D42	X0D41
F	MODE[2]	MODE[3]				GND	GND	GND	GND	GND	GND	GND	GND	GND				X0D34	X0D43/WAKE
G	AVDD	ADC7				GND	GND	GND	GND	GND	GND	GND	GND	GND				X1D00	X0D35
H	ADC5	ADC6				GND	GND	GND	GND	GND	GND	GND	GND	GND				X1D02	X1D01
J	ADC3	ADC4				AVSS	GND	GND	GND	GND	GND	GND	GND	GND				X1D04	X1D03
K	ADC1	ADC2				MODE[0]	MODE[1]	GND	GND	GND	GND	GND	GND	GND				X1D06	X1D05
L	NC	ADC0				OSC_EXT_N	MODE[4]	GND	GND	GND	GND	GND	GND	GND				X1D08	X1D07
M	XI/CLK	NC				NC	NC	GND	GND	GND	GND	GND	GND	GND				X1D10	X1D09
N	XO	NC				NC	NC	GND	GND	GND	GND	GND	GND	GND				X1D12	X1D11
P	NC	VSUP				GND	GND	GND	GND	GND	GND	GND	GND	GND				X1D14	X1D13
R	SW1	SW1																X1D16	X1D15
T	SW1	VDDCORE																X1D18	X1D17
U	VDDCORE	VDDCORE																X1D20	X1D19
V	PGND	PGND	VDDIO	PGND	VDD1V8	SW2	NC	X1D35	X1D43	X1D41	X1D39	X1D37	X1D33	X1D31	X1D29	X1D27	X1D25	X1D22	X1D21
W	VSUP	VSUP	VDDIO	PGND	VDD1V8	SW2	NC	X1D34	X1D42	X1D40	X1D38	X1D36	X1D32	X1D30	X1D28	X1D26	X1D24	X1D70	X1D23

Signal	Function						Type	Properties
X0D17	XLB^0_{out}		$4D^1$	$8B^3$	$16A^{11}$		I/O	PD_S, R_U
X0D18	XLB^0_{in}		$4D^2$	$8B^4$	$16A^{12}$		I/O	PD_S, R_U
X0D19	XLB^1_{in}		$4D^3$	$8B^5$	$16A^{13}$		I/O	PD_S, R_U
X0D20	XLB^2_{in}		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	I/O	PD_S, R_U
X0D21	XLB^3_{in}		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	I/O	PD_S, R_U
X0D22	XLB^4_{in}	$1G^0$					I/O	PD_S, R_U
X0D23		$1H^0$					I/O	PD_S, R_U
X0D24		$1I^0$					I/O	PD_S
X0D25		$1J^0$					I/O	PD_S
X0D26			$4E^0$	$8C^0$	$16B^0$		I/O	PD_S, R_U
X0D27			$4E^1$	$8C^1$	$16B^1$		I/O	PD_S, R_U
X0D28			$4F^0$	$8C^2$	$16B^2$		I/O	PD_S, R_U
X0D29			$4F^1$	$8C^3$	$16B^3$		I/O	PD_S, R_U
X0D30			$4F^2$	$8C^4$	$16B^4$		I/O	PD_S, R_U
X0D31			$4F^3$	$8C^5$	$16B^5$		I/O	PD_S, R_U
X0D32			$4E^2$	$8C^6$	$16B^6$		I/O	PD_S, R_U
X0D33			$4E^3$	$8C^7$	$16B^7$		I/O	PD_S, R_U
X0D34		$1K^0$					I/O	PD_S
X0D35		$1L^0$					I/O	PD_S
X0D36		$1M^0$		$8D^0$	$16B^8$		I/O	PD_S
X0D37		$1N^0$		$8D^1$	$16B^9$		I/O	PD_S, R_U
X0D38		$1O^0$		$8D^2$	$16B^{10}$		I/O	PD_S, R_U
X0D39		$1P^0$		$8D^3$	$16B^{11}$		I/O	PD_S, R_U
X0D40				$8D^4$	$16B^{12}$		I/O	PD_S, R_U
X0D41				$8D^5$	$16B^{13}$		I/O	PD_S, R_U
X0D42				$8D^6$	$16B^{14}$		I/O	PD_S, R_U
X0D43/WAKE				$8D^7$	$16B^{15}$		I/O	PU_S, R_U
X0D70						$32A^{19}$	I/O	PD_S
X1D00		$1A^0$					I/O	PD_S, R_S
X1D01	XLA^4_{out}	$1B^0$					I/O	PD_S, R_S
X1D02	XLA^3_{out}		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	I/O	PD_S, R_U
X1D03	XLA^2_{out}		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	I/O	PD_S, R_U
X1D04	XLA^1_{out}		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	I/O	PD_S, R_U
X1D05	XLA^0_{out}		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	I/O	PD_S, R_U
X1D06	XLA^0_{in}		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	I/O	PD_S, R_U
X1D07	XLA^1_{in}		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	I/O	PD_S, R_U
X1D08	XLA^2_{in}		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	I/O	PD_S, R_U
X1D09	XLA^3_{in}		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	I/O	PD_S, R_U
X1D10	XLA^4_{in}	$1C^0$					I/O	PD_S, R_S
X1D11		$1D^0$					I/O	PD_S, R_S
X1D12		$1E^0$					I/O	PD_S, R_U
X1D13	XLB^4_{out}	$1F^0$					I/O	PD_S, R_U
X1D14	XLB^3_{out}		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	I/O	PD_S, R_U

(continued)

Signal	Function					Type	Properties
X1D15	XLB^{2}_{out}	$4C^{1}$	$8B^{1}$	$16A^{9}$	$32A^{29}$	I/O	PD_S, R_U
X1D16	XLB^{1}_{out}	$4D^{0}$	$8B^{2}$	$16A^{10}$		I/O	PD_S, R_U
X1D17	XLB^{0}_{out}	$4D^{1}$	$8B^{3}$	$16A^{11}$		I/O	PD_S, R_U
X1D18	XLB^{0}_{in}	$4D^{2}$	$8B^{4}$	$16A^{12}$		I/O	PD_S, R_U
X1D19	XLB^{1}_{in}	$4D^{3}$	$8B^{5}$	$16A^{13}$		I/O	PD_S, R_U
X1D20	XLB^{2}_{in}	$4C^{2}$	$8B^{6}$	$16A^{14}$	$32A^{30}$	I/O	PD_S, R_U
X1D21	XLB^{3}_{in}	$4C^{3}$	$8B^{7}$	$16A^{15}$	$32A^{31}$	I/O	PD_S, R_U
X1D22	XLB^{4}_{in}	$1G^{0}$				I/O	PD_S, R_U
X1D23		$1H^{0}$				I/O	PD_S, R_U
X1D24		$1I^{0}$				I/O	PD_S
X1D25		$1J^{0}$				I/O	PD_S
X1D26		$4E^{0}$	$8C^{0}$	$16B^{0}$		I/O	PD_S, R_U
X1D27		$4E^{1}$	$8C^{1}$	$16B^{1}$		I/O	PD_S, R_U
X1D28		$4F^{0}$	$8C^{2}$	$16B^{2}$		I/O	PD_S, R_U
X1D29		$4F^{1}$	$8C^{3}$	$16B^{3}$		I/O	PD_S, R_U
X1D30		$4F^{2}$	$8C^{4}$	$16B^{4}$		I/O	PD_S, R_U
X1D31		$4F^{3}$	$8C^{5}$	$16B^{5}$		I/O	PD_S, R_U
X1D32		$4E^{2}$	$8C^{6}$	$16B^{6}$		I/O	PD_S, R_U
X1D33		$4E^{3}$	$8C^{7}$	$16B^{7}$		I/O	PD_S, R_U
X1D34		$1K^{0}$				I/O	PD_S
X1D35		$1L^{0}$				I/O	PD_S
X1D36		$1M^{0}$	$8D^{0}$	$16B^{8}$		I/O	PD_S
X1D37		$1N^{0}$	$8D^{1}$	$16B^{9}$		I/O	PD_S, R_U
X1D38		$1O^{0}$	$8D^{2}$	$16B^{10}$		I/O	PD_S, R_U
X1D39		$1P^{0}$	$8D^{3}$	$16B^{11}$		I/O	PD_S, R_U
X1D40			$8D^{4}$	$16B^{12}$		I/O	PD_S, R_U
X1D41			$8D^{5}$	$16B^{13}$		I/O	PD_S, R_U
X1D42			$8D^{6}$	$16B^{14}$		I/O	PD_S, R_U
X1D43			$8D^{7}$	$16B^{15}$		I/O	PU_S, R_U
X1D70					$32A^{19}$	I/O	PD_S

6 Product Overview

The XS1-A12A-128-FB217 comprises a digital and an analog node, as shown in Figure 3. The digital node comprises an xCORE Tile, a Switch, and a PLL (Phase-locked-loop). The analog node comprises a multi-channel ADC (Analog to Digital Converter), deep sleep memory, an oscillator, a real-time counter, and power supply control.

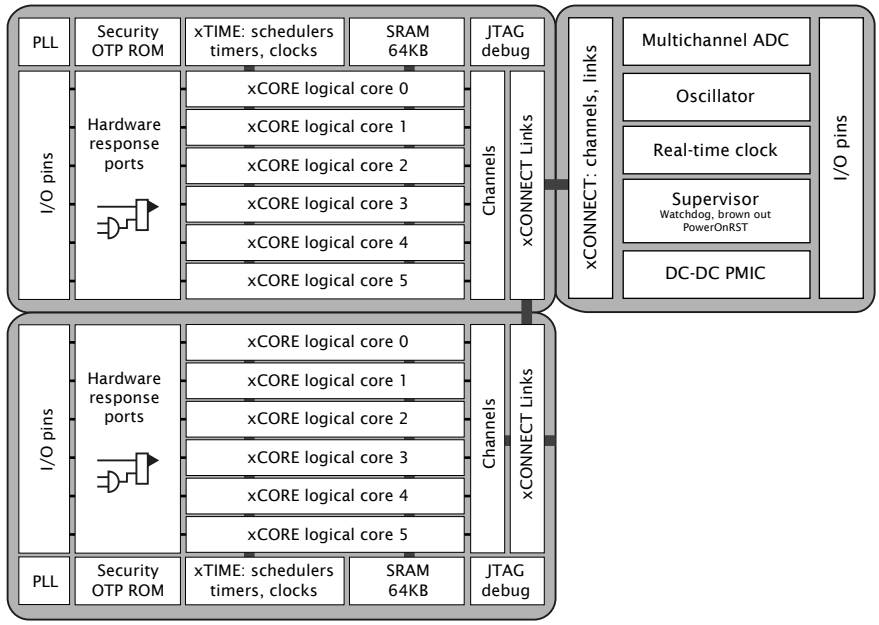

Figure 3: Block Diagram

All communication between the digital and analog node takes place over a link that is connected to the Switch of the digital node. As such, the analog node can be controlled from any node on the system. The analog functions can be configured using a set of node configuration registers, and a set of registers for each of the peripherals.

The device can be programmed using high-level languages such as C/C++ and the XMOS-originated XC language, which provides extensions to C that simplify the control over concurrency, I/O and timing, or low-level assembler.

6.1 XCore Tile

The xCORE Tile is a flexible multicore microcontroller component with tightly integrated I/O and on-chip memory. The tile contains multiple logical cores that run simultaneously, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. The logical cores use channels to exchange data within a tile or across tiles. The tiles are connected via an integrated switch network, called xCONNECT, which uses a

proprietary physical layer protocol and can also be used to add additional resources to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

6.2 ADC and Power Management

Each XS1-A12A-128-FB217 device includes a set of analog components, including a 12b, 8-channel ADC, power management unit, watchdog timer, real-time counter and deep sleep memory. The device reduces the number of additional external components required and allows designs to be implemented using simple 2-layer boards.

7 xCORE Tile Resources

7.1 Logical cores

Each tile has 6 active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 4 shows the guaranteed core performance depending on the number of cores used.

Figure 4: Logical core performance

Speed grade	MIPS	Frequency	Minimum MIPS per core (for *n* cores)							
			1	2	3	4	5	6		
8	800 MIPS	400 MHz	100	100	100	100	80	67		
10	1000 MIPS	500 MHz	125	125	125	125	100	83		

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum but cannot be guaranteed.

The logical cores are triggered by events instead of interrupts and run to completion. A logical core can be paused to wait for an event.

7.2 xTIME scheduler

The xTIME scheduler handles the events generated by xCORE Tile resources, such as channel ends, timers and I/O pins. It ensures that all events are serviced and synchronized, without the need for an RTOS. Events that occur at the I/O pins are handled by the Hardware-Response ports and fed directly to the appropriate xCORE Tile. An xCORE Tile can also choose to wait for a specified time to elapse, or for data to become available on a channel.

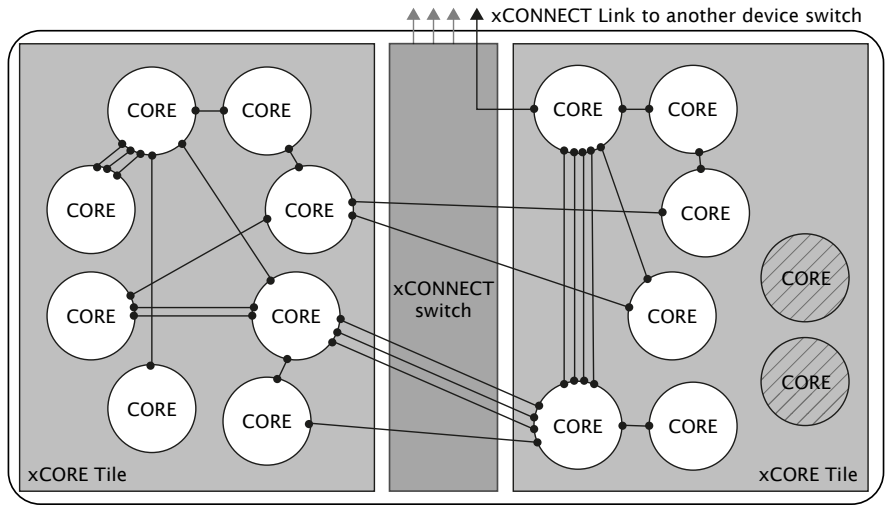

Figure 7: Switch, links and channel ends

between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between tiles , but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

8 Oscillator

The oscillator block provides:

- An oscillator circuit. Together with an external resonator (crystal or ceramic), the oscillator circuit can provide a clock-source for both the real-time counter and the xCORE Tile. The external resonator can be chosen by the designer to have the appropriate frequency and accuracy. If desired, an external oscillator can be used on the XI/CLK input pin, this must be a 1.8 V oscillator.
- A 20 MHz silicon oscillator. This enables the device to boot and execute code without requiring an external crystal. The silicon oscillator is not as accurate as an external crystal.

- A 31,250 Hz oscillator. This enables the real-time counter to operate whilst the device is in low-power mode. This oscillator is not as accurate as an external crystal.

The oscillator can be controlled through package pins, a set of peripheral registers, and a digital node control register.

A package pin OSC_EXT_N is used to select the oscillator to use on boot. It must be grounded to select an external resonator or connected to VDDIO to select the on-chip 20 MHz oscillator. If an external resonator is used, then it must be in the range 5-100 MHz. Two more package pins, MODE0 and MODE1 are used to inform the node of the frequency.

The analog node runs at the frequency provided by the oscillator. Hence, increasing the clock frequency will speed up operation of the analog node, and will speed up communicating data with the digital node. The digital node has a PLL.

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock.

The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 8:

Figure 8: PLL multiplier values and MODE pins

Oscillator Frequency	MODE 1	MODE 0	Tile Frequency	PLL Ratio	PLL settings OD	F	R
5-13 MHz	0	0	130-399.75 MHz	30.75	1	122	0
13-20 MHz	1	1	260-400.00 MHz	20	2	119	0
20-48 MHz	1	0	167-400.00 MHz	8.33	2	49	0
48-100 MHz	0	1	196-400.00 MHz	4	2	23	0

Figure 8 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, F and R must be chosen so that $0 \leq R \leq 63$, $0 \leq F \leq 4095$, $0 \leq OD \leq 7$, and $260MHz \leq F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \leq 1.3GHz$. The OD, F, and R values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset.

If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the XS1-L Clock Frequency Control document, X1433.

The program size and CRC are stored least significant byte first. The program is loaded into the lowest memory address of RAM, and the program is started from that address. The CRC is calculated over the byte stream represented by the program size and the program itself. The polynomial used is 0xEDB88320 (IEEE 802.3); the CRC register is initialized with 0xFFFFFFFF and the residue is inverted to produce the CRC.

9.1 Boot from SPI master

If set to boot from SPI master, the processor enables the four pins specified in Figure 11, and drives the SPI clock at 2.5 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Figure 11: SPI master pins

Pin	Signal	Description
X0D00	MISO	Master In Slave Out (Data)
X0D01	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. Programmers who write bytes into an SPI interface using the most significant bit first may have to reverse the bits in each byte of the image stored in the SPI device.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

9.2 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables Link B around 200 ns after the boot process starts. Enabling the Link switches off the pull-down on resistors X0D16..X0D19, drives X0D16 and X0D17 low (the initial state for the Link), and monitors pins X0D18 and X0D19 for boot-traffic. X0D18 and X0D19 must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

The boot-rom on the core will then:

1. Allocate channel-end 0.
2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
3. Input the boot image specified above, including the CRC.

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
Secure Boot	5	The processor is forced to boot from address 0 of the OTP, allowing the processor boot ROM to be bypassed (*see* §9).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	21..15	General purpose software accessable security register available to end-users.
	31..22	General purpose user programmable JTAG UserID code extension.

Figure 12: Security register features

32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10.3 Deep Sleep Memory

The XS1-A12A-128-FB217 device includes 128 bytes of deep sleep memory for state storage during sleep mode. Deep sleep memory is volatile and if device input power is remove, the data will be lost.

11 Analog-to-Digital Converter

The device has a 12-bit 1MSample/second Successive Approximation Register (SAR) Analogue to Digital Converter (ADC). It has 8 input pins which are multiplexed into the ADC. The sampling of the ADC is controlled using the ADC_SAMPLE pin that should be wired to a GPIO pin, for example X0D24 (port 1I). The sampling is triggered either by writing to the port, or by driving the pin externally. On each

17.5 Digital I/O Characteristics

Figure 28: Digital I/O characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		3.60	V	A
V(IL)	Input low voltage	-0.30		0.70	V	A
V(OH)	Output high voltage	2.00			V	B, C
V(OL)	Output low voltage			0.60	V	B, C
R(PU)	Pull-up resistance		35K		Ω	D
R(PD)	Pull-down resistance		35K		Ω	D

A All pins except power supply pins.

B Ports 1A, 1D, 1E, 1H, 1I, 1J, 1K and 1L are nominal 8 mA drivers, the remainder of the general-purpose I/Os are 4 mA.

C Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.

D Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.

17.6 ESD Stress Voltage

Figure 29: ESD stress voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model			2.00	kV	
CDM	Charged Device Model			500	V	

17.7 Device Timing Characteristics

Figure 30: Device timing characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			µs	
T(INIT)	Initialisation (On Silicon Oscillator)			TBC	ms	A
	Initialisation (Crystal Oscillator)			TBC	ms	
T(WAKE)	Wake up time (Sleep to Active)			TBC	ms	
T(SLEEP)	Sleep Time (Active to Sleep)			TBC	ms	

A Shows the time taken to start booting after RST_N has gone high.

17.8 Crystal Oscillator Characteristics

Figure 31: Crystal oscillator characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
F(FO)	Input Frequency	5		30	MHz	

18.1 Part Marking

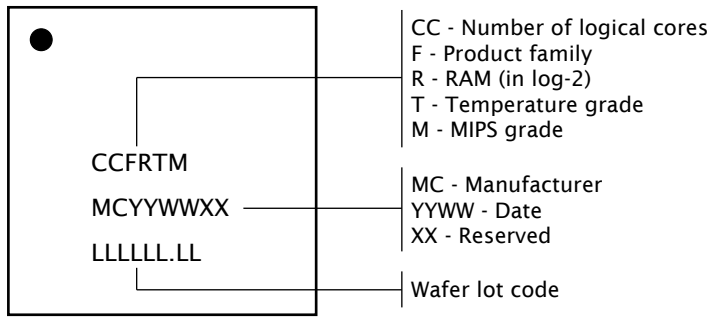

Figure 38: Part marking scheme

19 Ordering Information

Product Code	Marking	Qualification	Speed Grade
XS1-A12A-128-FB217-C8	12A7C8	Commercial	800 MIPS
XS1-A12A-128-FB217-C10	12A7C10	Commercial	1000 MIPS
XS1-A12A-128-FB217-I8	12A7I8	Industrial	800 MIPS
XS1-A12A-128-FB217-I10	12A7I10	Industrial	1000 MIPS

Figure 39: Orderable part numbers

B.19 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over JTAG. This is the same set of registers as the Debug Scratch registers in the xCORE tile configuration.

0x20 .. 0x27: Debug scratch

Bits	Perm	Init	Description
31:0	DRW		Value.

B.20 Instruction breakpoint address: 0x30 .. 0x33

This register contains the address of the instruction breakpoint. If the PC matches this address, then a debug interrupt will be taken. There are four instruction breakpoints that are controlled individually.

0x30 .. 0x33: Instruction breakpoint address

Bits	Perm	Init	Description
31:0	DRW		Value.

B.21 Instruction breakpoint control: 0x40 .. 0x43

This register controls which logical cores may take an instruction breakpoint, and under which condition.

0x40 .. 0x43: Instruction breakpoint control

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each logical core in the tile allowing the breakpoint to be enabled individually for each logical core.
15:2	RO	-	Reserved
1	DRW	0	Set to 1 to cause an instruction breakpoint if the PC is not equal to the breakpoint address. By default, the breakpoint is triggered when the PC is equal to the breakpoint address.
0	DRW	0	When 1 the instruction breakpoint is enabled.

B.22 Data watchpoint address 1: 0x50 .. 0x53

This set of registers contains the first address for the four data watchpoints.

D.13 PLink status and network: 0x40 .. 0x43

These registers contain status information and the network number that each processor-link belongs to.

0x40 .. 0x43: PLink status and network

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

D.14 Link configuration and initialization: 0x80 .. 0x87

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links C, D, A, B, G, H, E, and F in that order.

0x04: Node configuration register

Bits	Perm	Init	Description
31	RW	0	Set to 1 to disable further updates to the node configuration and link control and status registers.
30:1	RO	-	Reserved
0	RW	0	Header mode. 0: 3-byte headers; 1: 1-byte headers.

E.3 Node identifier: 0x05

0x05: Node identifier

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	16-bit node identifier. This does not need to be set, and is present for compatibility with XS1-switches.

E.4 Reset and Mode Control: 0x50

The XS1-S has two main reset signals: a system-reset and an xCORE Tile-reset. System-reset resets the whole system including external devices, whilst xCORE Tile-reset resets the xCORE Tile(s) only. The resets are induced either by software (by a write to the register below) or by one of the following:

* External reset on RST_N (System reset)

* Brown out on one of the power supplies (System reset)

* Watchdog timer (System reset)

* Sleep sequence (xCORE Tile reset)

* Clock source change (xCORE Tile reset)

The minimum system reset duration is achieved when the fastest permissible clock is used. The reset durations will be proportionately longer when a slower clock is used. Note that the minimum system reset duration allows for all power rails except the VOUT2 to turn off, and decay.

The length of the system reset comes from an internal counter, counting 524,288 oscillator clock cycles which gives the maximum time allowable for the supply rails to discharge. The system reset duration is a balance between leaving a long time for the supply rails to discharge, and a short time for the system to boot. Example reset times are 44 ms with a 12 MHz oscillator or 5.5 ms with a 96 MHz oscillator.

0x0C: ADC Control input pin 3

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

F.5 ADC Control input pin 4: 0x10

Controls specific to ADC input pin 4.

0x10: ADC Control input pin 4

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

F.6 ADC Control input pin 5: 0x14

Controls specific to ADC input pin 5.

0x14: ADC Control input pin 5

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

F.7 ADC Control input pin 6: 0x18

Controls specific to ADC input pin 6.

J.5 Power supply states whilst WAKING1: 0x10

This register controls what state the power control block should be in when in the WAKING1 state. It also defines the minimum time that the system shall stay in this state. When the minimum time is expired, the next state is entered if all enabled power supplies are good.

0x10: Power supply states whilst WAKING1

Bits	Perm	Init	Description
31:21	RO	-	Reserved
20:16	RW	16	Log2 number of cycles to stay in this state: 0: 1 clock cycles 1: 2 clock cycles 2: 4 clock cycles ... 31: 2147483648 clock cycles
15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	1	Set to 1 to enable VOUT6 (IO supply).
4	RW	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	0	Set to 1 to enable DCDC2 (analogue supply).
0	RW	0	Set to 1 to enable DCDC1 (core supply).

J.6 Power supply states whilst WAKING2: 0x14

This register controls what state the power control block should be in when in the WAKING2 state. It also defines the minimum time that the system shall stay in this state. When the minimum time is expired, the next state is entered if all enabled power supplies are good.

M JTAG, xSCOPE and Debugging

If you intend to design a board that can be used with the XMOS toolchain and xTAG debugger, you will need an xSYS header on your board. Figure 51 shows a decision diagram which explains what type of xSYS connectivity you need. The three subsections below explain the options in detail.

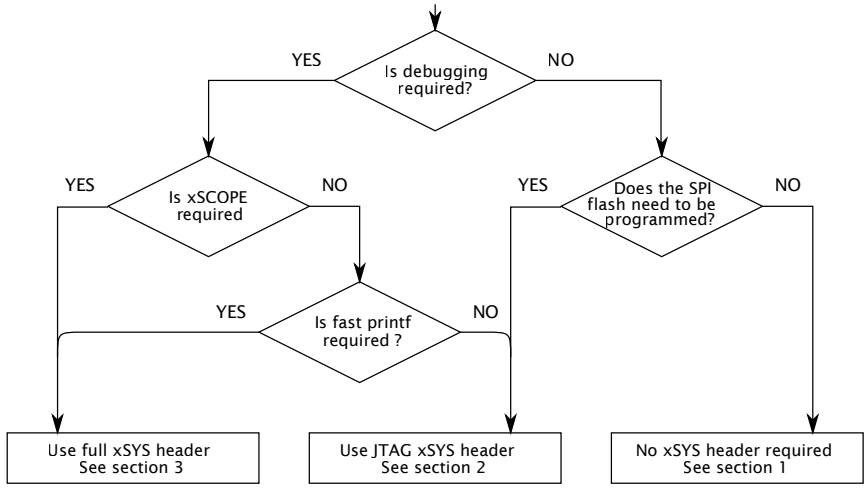

Figure 51: Decision diagram for the xSYS header

M.1 No xSYS header

The use of an xSYS header is optional, and may not be required for volume production designs. However, the XMOS toolchain expects the xSYS header; if you do not have an xSYS header then you must provide your own method for writing to flash/OTP and for debugging.

M.2 JTAG-only xSYS header

The xSYS header connects to an xTAG debugger, which has a 20-pin 0.1" female IDC header. The design will hence need a male IDC header. We advise to use a boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB.

Connect pins 4, 8, 12, 16, 20 of the xSYS header to ground, and then connect:

- TDI to pin 5 of the xSYS header
- TMS to pin 7 of the xSYS header
- TCK to pin 9 of the xSYS header
- DEBUG_N to pin 11 of the xSYS header

- TDO to pin 13 of the xSYS header
- RST_N to pin 15 of the xSYS header
- If MODE2 is configured high, connect MODE2 to pin 3 of the xSYS header. Do not connect to VDDIO.
- If MODE3 is configured high, connect MODE3 to pin 3 of the xSYS header. Do not connect to VDDIO.

The RST_N net should be open-drain, active-low, and have a pull-up to VDDIO.

M.3 Full xSYS header

For a full xSYS header you will need to connect the pins as discussed in Section M.2, and then connect a 2-wire xCONNECT Link to the xSYS header. The links can be found in the Signal description table (Section 4): they are labelled XLA, XLB, etc in the function column. The 2-wire link comprises two inputs and outputs, labelled ${}^{1}_{out}$, ${}^{0}_{out}$, ${}^{0}_{in}$, and ${}^{1}_{in}$. For example, if you choose to use XLB of tile 0 for xSCOPE I/O, you need to connect up XLB^{1}_{out}, XLB^{0}_{out}, XLB^{0}_{in}, XLB^{1}_{in} as follows:

- XLB^{1}_{out} (X0D16) to pin 6 of the xSYS header with a 33R series resistor close to the device.
- XLB^{0}_{out} (X0D17) to pin 10 of the xSYS header with a 33R series resistor close to the device.
- XLB^{0}_{in} (X0D18) to pin 14 of the xSYS header.
- XLB^{1}_{in} (X0D19) to pin 18 of the xSYS header.

P Associated Design Documentation

Document Title	Information	Document Number
Programming XC on XMOS Devices	Timers, ports, clocks, cores and channels	X9577
xTIMEcomposer User Guide	Compilers, assembler and linker/mapper Timing analyzer, xScope, debugger Flash and OTP programming utilities	X3766

Q Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
xCONNECT Architecture	Link, switch and system information	X4249
XS1-L Link Performance and Design Guidelines	Link timings	X2999
XS1-L Clock Frequency Control	Advanced clock control	X1433