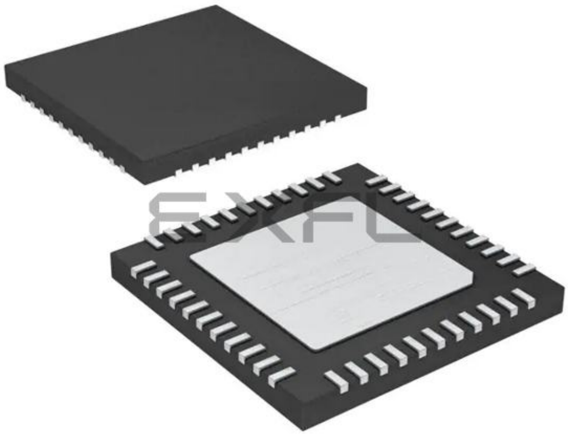

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f46j13t-i-ml

TABLE 1-3: PIC18F2XJ13 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number 28-SPDIP/ SSOP/ SOIC	Pin Number 28-QFN	Pin Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/C3IND/INT0/RP3	21	18			
RB0			I/O	TTL/DIG	Digital I/O.
AN12			I	Analog	Analog Input 12.
C3IND			I	Analog	Comparator 3 Input D.
INT0			I	ST	External Interrupt 0.
RP3			I/O	ST/DIG	Remappable Peripheral Pin 3 input/output.
RB1/AN10/C3INC/RTCC/RP4	22	19			
RB1			I/O	TTL/DIG	Digital I/O.
AN10			I	Analog	Analog Input 10.
C3INC			I	Analog	Comparator 3 input.
RTCC			O	DIG	Real-Time Clock Calendar output.
RP4			I/O	ST/DIG	Remappable Peripheral Pin 4 input/output.
RB2/AN8/C2INC/CTED1/ REFO/RP5	23	20			
RB2			I/O	TTL/DIG	Digital I/O.
AN8			I	Analog	Analog Input 8.
C2INC			I	Analog	Comparator 2 Input C.
CTED1			I	ST	CTMU Edge 1 input.
REFO			O	DIG	Reference output clock.
RP5			I/O	ST/DIG	Remappable Peripheral Pin 5 input/output.
RB3/AN9/C3INA/CTED2/ RP6	24	21			
RB3			I/O	TTL/DIG	Digital I/O.
AN9			I	Analog	Analog Input 9.
C3INA			I	Analog	Comparator 3 Input A.
CTED2			I	ST	CTMU edge 2 Input.
RP6			I	ST/DIG	Remappable Peripheral Pin 6 input/output.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
DIG = Digital output
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)
I^2C = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

2: 5.5V tolerant.

TABLE 1-4: PIC18F4XJ13 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
					PORTA is a bidirectional I/O port.
RA0/AN0/C1INA/ULPWU/PMA6/RP0	19	19			
RA0			I/O	TTL/DIG	Digital I/O.
AN0			I	Analog	Analog Input 0.
C1INA			I	Analog	Comparator 1 Input A.
ULPWU			I	Analog	Ultra low-power wake-up input.
PMA6			I/O	ST/TTL/DIG	Parallel Master Port digital I/O.
RP0			I/O	ST/DIG	Remappable Peripheral Pin 0 input/output.
RA1/AN1/C2INA/VBG/CTDIN/PMA7/RP1	20	20			
RA1			I/O	TTL/DIG	Digital I/O.
AN1			O	Analog	Analog Input 1.
C2INA			I	Analog	Comparator 2 Input A.
VBG			O	Analog	Band Gap Reference Voltage (VBG) output.
CTDIN			I	ST	CTMU pulse delay input.
PMA7			I/O	ST/TTL/DIG	Parallel Master Port digital I/O.
RP1			I/O	ST/DIG	Remappable Peripheral Pin 1 input/output.
RA2/AN2/C2INB/C1IND/C3INB/VREF-/CVREF	21	21			
RA2			I/O	TTL/DIG	Digital I/O.
AN2			I	Analog	Analog Input 2.
C2INB			I	Analog	Comparator 2 Input B.
C1IND			I	Analog	Comparator 1 Input D.
C3INB			I	Analog	Comparator 3 Input B.
VREF-			I	Analog	A/D reference voltage (low) input.
CVREF			I	Analog	Comparator reference voltage output.
RA3/AN3/C1INB/VREF+	22	22			
RA3			I/O	TTL/DIG	Digital I/O.
AN3			I	Analog	Analog Input 3.
C1INB			I	Analog	Comparator 1 Input B.
VREF+			I	Analog	A/D reference voltage (high) input.
RA5/AN4/C1INC/$\overline{SS1}$/HLVDIN/RP2	24	24			
RA5			I/O	TTL/DIG	Digital I/O.
AN4			I	Analog	Analog Input 4.
C1INC			I	Analog	SPI slave select input.
$\overline{SS1}$			I	TTL	Comparator 1 Input C.
HLVDIN			I	Analog	High/Low-Voltage Detect input.
RP2			I/O	ST/DIG	Remappable Peripheral Pin 2 input/output.
RA6[1]					See the OSC2/CLKO/RA6 pin.
RA7[1]					See the OSC1/CLKI/RA7 pin.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
DIG = Digital output
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)
I^2C = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.
2: Available only on 44-pin devices (PIC18F46J13, PIC18F47J13, PIC18LF46J13 and PIC18LF47J13).
3: 5.5V tolerant.

TABLE 1-4: PIC18F4XJ13 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number 44-QFN	Pin Number 44-TQFP	Pin Type	Buffer Type	Description
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI/RP11	34	32			
RC0			I/O	STDIG	Digital I/O.
T1OSO			O	Analog	Timer1 oscillator output.
T1CKI			I	ST	Timer1/Timer3 external clock input.
RP11			I/O	ST/DIG	Remappable Peripheral Pin 11 input/output.
RC1/CCP8/T1OSI/RP12	35	35			
RC1			I/O	ST/DIG	Digital I/O.
CCP8			I/O	ST/DIG	Capture/Compare/PWM input/output.
T1OSI			I	Analog	Timer1 oscillator input.
RP12			I/O	ST/DIG	Remappable Peripheral Pin 12 input/output.
RC2/AN11/C2IND/CTPLS/RP13	36	36			
RC2			I/O	ST/DIG	Digital I/O.
AN11			I	Analog	Analog Input 11.
C2IND			I	Analog	Comparator 2 Input D.
CTPLS			O	DIG	CTMU pulse generator output.
RP13			I/O	ST/DIG	Remappable Peripheral Pin 13 input/output.
RC3/SCK1/SCL1/RP14	37	37			
RC3			I/O	ST/DIG	Digital I/O.
SCK1			I/O	ST/DIG	SPI clock input/output.
SCL1			I/O	I^2C	I^2C clock input/output.
RP14			I/O	ST/DIG	Remappable Peripheral Pin 14 input/output.
RC4/SDI1/SDA1/RP15	42	42			
RC4			I/O	ST/DIG	Digital I/O.
SDI1			I	ST	SPI data input.
SDA1			I/O	I^2C	I^2C data input/output.
RP15			I/O	ST/DIG	Remappable Peripheral Pin 15 input/output.
RC5/SDO1/RP16	43	43			
RC5			I/O	ST/DIG	Digital I/O.
SDO1			O	DIG	SPI data output.
RP16			I/O	ST/DIG	Remappable Peripheral Pin 16 input/output.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
DIG = Digital output
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})
I^2C = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.
2: Available only on 44-pin devices (PIC18F46J13, PIC18F47J13, PIC18LF46J13 and PIC18LF47J13).
3: 5.5V tolerant.

4.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a `SLEEP` instruction. If the device is in another Run mode, first set IDLEN, then clear the SCS bits and execute `SLEEP`. When the clock source is switched to the INTOSC block, the primary oscillator is shut down and the OSTS bit is cleared.

When a wake event occurs, the peripherals continue to be clocked from the internal oscillator block. After a delay of T_{CSD}, following the wake event, the CPU begins executing code being clocked by the INTRC. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the FSCM is enabled.

4.5 Exiting Idle and Sleep Modes

An exit from Sleep mode, or any of the Idle modes, is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes sections (see **Section 4.2 "Run Modes"**, **Section 4.3 "Sleep Mode"** and **Section 4.4 "Idle Modes"**).

4.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode, or the Sleep mode, to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see **Section 9.0 "Interrupts"**).

A fixed delay of interval, T_{CSD}, following the wake event, is required when leaving Sleep mode. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

4.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is, when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see **Section 4.2 "Run Modes"** and **Section 4.3 "Sleep Mode"**). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see **Section 27.2 "Watchdog Timer (WDT)"**).

The WDT and postscaler are cleared by one of the following events:

- Executing a `SLEEP` or `CLRWDT` instruction
- The loss of a currently selected clock source (if the FSCM is enabled)

4.5.3 EXIT BY RESET

Exiting an Idle or Sleep mode by Reset automatically forces the device to run from the INTRC.

4.6.9 DEEP SLEEP MODE REGISTERS

Deep Sleep mode registers are provided in Register 4-1 through Register 4-6.

REGISTER 4-1: DSCONH: DEEP SLEEP CONTROL HIGH BYTE REGISTER (BANKED F4Dh)

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
DSEN[(1)]	—	—	—	—	r	DSULPEN	RTCWDIS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **DSEN:** Deep Sleep Enable bit[(1)]
- `1` = Deep Sleep mode is entered on a `SLEEP` command
- `0` = Sleep mode is entered on a `SLEEP` command

bit 6-3 **Unimplemented:** Read as ‘`0`’

bit 2 **Reserved:** Maintain as ‘`0`’

bit 1 **DSULPEN:** Ultra Low-Power Wake-up Module Enable bit
- `1` = ULPWU module is enabled in Deep Sleep
- `0` = ULPWU module is disabled in Deep Sleep

bit 0 **RTCWDIS:** RTCC Wake-up Disable bit
- `1` = Wake-up from RTCC is disabled
- `0` = Wake-up from RTCC is enabled

Note 1: In order to enter Deep Sleep, Sleep must be executed within 2 instruction cycles after setting DSEN.

REGISTER 4-2: DSCONL: DEEP SLEEP LOW BYTE CONTROL REGISTER (BANKED F4Ch)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0[(1)]	R/W-0[(1)]
—	—	—	—	—	ULPWDIS	DSBOR	RELEASE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as ‘`0`’

bit 2 **ULPWDIS:** Ultra Low-Power Wake-up Disable bit
- `1` = ULPWU wake-up source is disabled
- `0` = ULPWU wake-up source is enabled (must also set DSULPEN = `1`)

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit
- `1` = DSBOREN was enabled and V_{DD} dropped below the DSBOR arming voltage during Deep Sleep, but did not fall below V_{DSBOR}
- `0` = DSBOREN was disabled or V_{DD} did not drop below the DSBOR arming voltage during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit

Upon waking from Deep Sleep, the I/O pins maintain their previous states. Clearing this bit will release the I/O pins and allow their respective TRIS and LAT bits to control their states.

Note 1: This is the value when V_{DD} is initially applied.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset, Wake From Deep Sleep	$\overline{MCLR}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
CCPR9H	PIC18F2XJ13	PIC18F4XJ13	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR9L	PIC18F2XJ13	PIC18F4XJ13	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP9CON	PIC18F2XJ13	PIC18F4XJ13	--00 0000	--00 0000	--uu uuuu
CCPR10H	PIC18F2XJ13	PIC18F4XJ13	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR10L	PIC18F2XJ13	PIC18F4XJ13	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP10CON	PIC18F2XJ13	PIC18F4XJ13	--00 0000	--00 0000	--uu uuuu
RPINR24	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR23	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR22	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR21	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR17	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR16	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR14	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR13	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR12	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR9	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR8	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR7	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR15	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR6	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR4	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR3	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR2	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPINR1	PIC18F2XJ13	PIC18F4XJ13	---1 1111	---1 1111	---u uuuu
RPOR24	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR23	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR22	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR21	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR20	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR19	—	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR18	PIC18F2XJ13	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu
RPOR17	PIC18F2XJ13	PIC18F4XJ13	---0 0000	---0 0000	---u uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

5: Not implemented on PIC18F2XJ13 devices.

6: Not implemented on "LF" devices.

TABLE 6-4: REGISTER FILE SUMMARY (PIC18F47J13 FAMILY) (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F4Bh	DSWAKEH	—	—	—	—	—	—	—	DSINT0	`---- ---0`
F4Ah	DSWAKEL	DSFLT	—	DSULP	DSWDT	DSRTC	DSMCLR	—	DSPOR	`0-00 00-1`
F49h	ANCON1	VBGEN	—	—	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	`0--0 0000`
F48h	ANCON0	PCFG7[2]	PCFG6[2]	PCFG5[2]	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	`0000 0000`
F47h	ALRMCFG	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	`0000 0000`
F46h	ALRMRPT	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	`0000 0000`
F45h	ALRMVALH	Alarm Value High Register Window based on ALRMPTR<1:0>								`xxxx xxxx`
F44h	ALRMVALL	Alarm Value Low Register Window based on ALRMPTR<1:0>								`xxxx xxxx`
F43h	—	—	—	—	—	—	—	—	—	`---- ----`
F42h	ODCON1	CCP8OD	CCP7OD	CCP6OD	CCP5OD	CCP4OD	ECCP3OD	ECCP2OD	ECCP1OD	`0000 0000`
F41h	ODCON2	—	—	—	—	CCP10OD	CCP9OD	U2OD	U1OD	`---- 0000`
F40h	ODCON3	CTMUDS	—	—	—	—	—	SPI2OD	SPI1OD	`0--- --00`
F3Fh	RTCCFG	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	`0-00 0000`
F3Eh	RTCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	`0000 0000`
F3Dh	REFOCON	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	`0-00 0000`
F3Ch	PADCFG1	—	—	—	—	—	RTSECSEL1	RTSECSEL0	PMPTTL[2]	`---- -000`
F3Bh	RTCVALH	RTCC Value High Register Window based on RTCPTR<1:0>								`0xxx xxxx`
F3Ah	RTCVALL	RTCC Value Low Register Window based on RTCPTR<1:0>								`0xxx xxxx`
F25h	CM3CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	`0001 1111`
F24h	TMR5H	Timer5 Register High Byte								`xxxx xxxx`
F23h	TMR5L	Timer5 Register Low Bytes								`xxxx xxxx`
F22h	T5CON	TMR5CS1	TMR5CS0	T5CKPS1	T5CKPS0	T5OSCEN	$\overline{\text{T5SYNC}}$	RD16	TMR5ON	`0000 0000`
F21h	T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/$\overline{\text{T5DONE}}$	T5GVAL	T5GSS1	T5GSS0	`0000 0x00`
F20h	TMR6	Timer6 Register								`0000 0000`
F1Fh	PR6	Timer6 Period Register								`1111 1111`
F1Eh	T6CON	—	T6OUTPS3	T6OUTPS2	T6OUTPS1	T6OUTPS0	TMR6ON	T6CKPS1	T6CKPS0	`-000 0000`
F1Dh	TMR8	Timer8 Register								`0000 0000`
F1Ch	PR8	Timer8 Period Register								`1111 1111`
F1Bh	T8CON	—	T8OUTPS3	T8OUTPS2	T8OUTPS1	T8OUTPS0	TMR8ON	T8CKPS1	T8CKPS0	`-000 0000`
F1Ah	PSTR3CON	CMPL1	CMPL0	—	STRSYNC	STRD	STRC	STRB	STRA	`00-0 0001`
F19h	ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	`0000 0000`
F18h	ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	`0000 0000`
F17h	CCPR3H	Capture/Compare/PWM Register 3 High Byte								`xxxx xxxx`
F16h	CCPR3L	Capture/Compare/PWM Register 3 Low Byte								`xxxx xxxx`
F15h	CCP3CON	P3M1	P3M0	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	`0000 0000`
F14h	CCPR4H	Capture/Compare/PWM Register 4 High Byte								`xxxx xxxx`
F13h	CCPR4L	Capture/Compare/PWM Register 4 Low Byte								`xxxx xxxx`
F12h	CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	`--00 0000`
F11h	CCPR5H	Capture/Compare/PWM Register 5 High Byte								`xxxx xxxx`
F10h	CCPR5L	Capture/Compare/PWM Register 5 Low Byte								`xxxx xxxx`
F0Fh	CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	`--00 0000`
F0Eh	CCPR6H	Capture/Compare/PWM Register 6 High Byte								`xxxx xxxx`
F0Dh	CCPR6L	Capture/Compare/PWM Register 6 Low Byte								`xxxx xxxx`
F0Ch	CCP6CON	—	—	DC6B1	DC6B0	CCP6M3	CCP6M2	CCP6M1	CCP6M0	`--00 0000`
F0Bh	CCPR7H	Capture/Compare/PWM Register 7 High Byte								`xxxx xxxx`
F0Ah	CCPR7L	Capture/Compare/PWM Register 7 Low Byte								`xxxx xxxx`
F09h	CCP7CON	—	—	DC7B1	DC7B0	CCP7M3	CCP7M2	CCP7M1	CCP7M0	`--00 0000`
F08h	CCPR8H	Capture/Compare/PWM Register 8 High Byte								`xxxx xxxx`

Note 1: Applicable for 28-pin devices (PIC18F26J13, PIC18F27J13, PIC18LF26J13 and PIC18LF27J13).
2: Applicable for 44-pin devices (PIC18F46J13, PIC18F47J13, PIC18LF46J13 and PIC18LF47J13).
3: Value on POR, BOR.

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

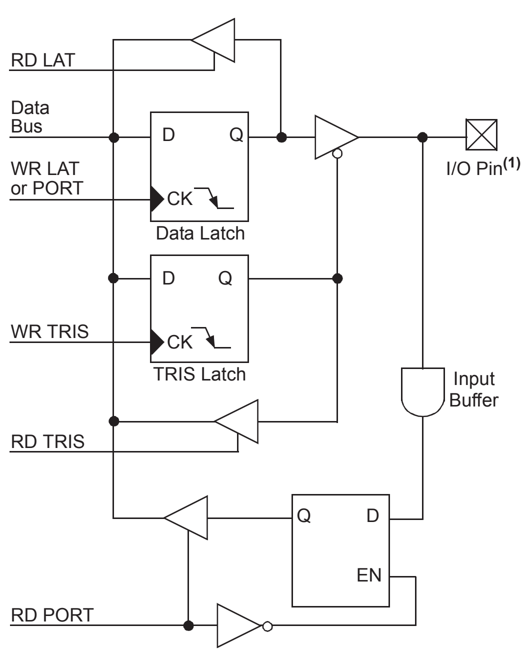
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Data Latch)

The Data Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

Figure 10-1 displays a simplified model of a generic I/O port, without the interfaces to other peripherals.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 I/O Port Pin Capabilities

When developing an application, the capabilities of the port pins must be considered. Outputs on some pins have higher output drive strength than others. Similarly, some pins can tolerate higher than VDD input levels.

10.1.1 PIN OUTPUT DRIVE

The output pin drive strengths vary for groups of pins intended to meet the needs for a variety of applications. PORTB and PORTC are designed to drive higher loads, such as LEDs. All other ports are designed for small loads, typically indication only. Table 10-1 summarizes the output capabilities. Refer to **Section 30.0 "Electrical Characteristics"** for more details.

TABLE 10-1: OUTPUT DRIVE LEVELS

Port	Drive	Description
PORTA	Minimum	Intended for indication.
PORTD		
PORTE		
PORTB	High	Suitable for direct LED drive levels.
PORTC		

10.1.2 INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Pins that are used as digital only inputs are able to handle DC voltages up to 5.5V; a level typical for digital logic circuits. In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins should be avoided. Table 10-2 summarizes the input capabilities. Refer to **Section 30.0 "Electrical Characteristics"** for more details.

TABLE 10-2: INPUT VOLTAGE LEVELS

Port or Pin	Tolerated Input	Description
PORTA<7:0>	VDD	Only VDD input levels are tolerated.
PORTB<3:0>		
PORTC<2:0>		
PORTE<2:0>		
PORTB<7:4>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTC<7:3>		
PORTD<7:0>		

TABLE 10-3: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0/C1INA/ULPWU/PMA6/RP0	RA0	1	I	TTL	PORTA<0> data input; disabled when analog input is enabled.
		0	O	DIG	LATA<0> data output; not affected by analog input.
	AN0	1	I	ANA	A/D Input Channel 0 and Comparator C1- input. Default input configuration on POR; does not affect digital output.
	C1INA	1	I	ANA	Comparator 1 Input A.
	ULPWU	1	I	ANA	Ultra low-power wake-up input.
	PMA6[(1)]	x	I/O	ST/TTL/DIG	Parallel Master Port digital I/O.
	RP0	1	I	ST	Remappable Peripheral Pin 0 input.
		0	O	DIG	Remappable Peripheral Pin 0 output.
RA1/AN1/C2INA/VBG/CTDIN/PMA7/RP1	RA1	1	I	TTL	PORTA<1> data input; disabled when analog input is enabled.
		0	O	DIG	LATA<1> data output; not affected by analog input.
	AN1	1	I	ANA	A/D Input Channel 1 and Comparator C2- input. Default input configuration on POR; does not affect digital output.
	C2INA	1	I	ANA	Comparator 1 Input A.
	VBG	x	O	ANA	Band Gap Voltage Reference output. (Enabled by setting the VBGOE bit (WDTCON<4>.)
	CTDIN	1	I	ST	CTMU pulse delay input.
	PMA7[(1)]	1	I	ST/TTL	Parallel Master Port (`io_addr_in[7]`).
		0	O	DIG	Parallel Master Port address.
	RP1	1	I	ST	Remappable Peripheral Pin 1 input.
		0	O	DIG	Remappable Peripheral Pin 1 output
RA2/AN2/C2INB/C1IND/C3INB/VREF-/CVREF	RA2	0	O	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output is enabled.
		1	I	TTL	PORTA<2> data input. Disabled when analog functions are enabled; disabled when CVREF output is enabled.
	AN2	1	I	ANA	A/D Input Channel 2 and Comparator C2+ input. Default input configuration on POR; not affected by analog output.
	C2INB	1	I	ANA	Comparator 2 Input B.
		0	O	ANA	CTMU pulse generator charger for the C2INB comparator input.
	C1IND	1	I	ANA	Comparator 1 Input D.
	C3INB	1	I	ANA	Comparator 3 Input B.
	VREF-	1	I	ANA	A/D and comparator voltage reference low input.
	CVREF	x	O	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/C1INB/VREF+	RA3	0	O	DIG	LATA<3> data output; not affected by analog input.
		1	I	TTL	PORTA<3> data input; disabled when analog input is enabled.
	AN3	1	I	ANA	A/D Input Channel 3 and Comparator C1+ input. Default input configuration on POR.
	C1INB	1	I	ANA	Comparator 1 Input B
	VREF+	1	I	ANA	A/D and comparator voltage reference high input.

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRISx bit does not affect port direction or is overridden for this option)

Note 1: This bit is only available on 44-pin devices (PIC18F46J13, PIC18F47J13, PIC18LF46J13 and PIC18LF47J13).

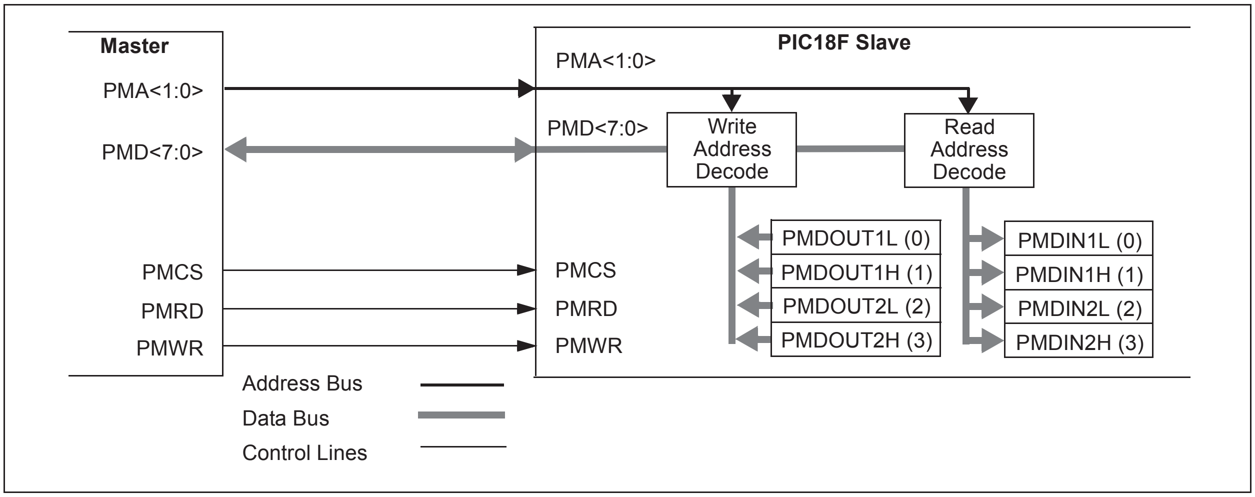
11.2.5 ADDRESSABLE PARALLEL SLAVE PORT MODE

In the Addressable Parallel Slave Port mode (PMMODEH<1:0> = 01), the module is configured with two extra inputs, PMA<1:0>, which are the Address Lines 1 and 0. This makes the 4-byte buffer space directly addressable as fixed pairs of read and write buffers. As with Legacy Buffered mode, data is output from PMDOUT1L, PMDOUT1H, PMDOUT2L and PMDOUT2H, and is read in PMDIN1L, PMDIN1H, PMDIN2L and PMDIN2H. Table 11-1 provides the buffer addressing for the incoming address to the input and output registers.

TABLE 11-1: SLAVE MODE BUFFER ADDRESSING

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1L (0)	PMDIN1L (0)
01	PMDOUT1H (1)	PMDIN1H (1)
10	PMDOUT2L (2)	PMDIN2L (2)
11	PMDOUT2H((3)	PMDIN2H (3)

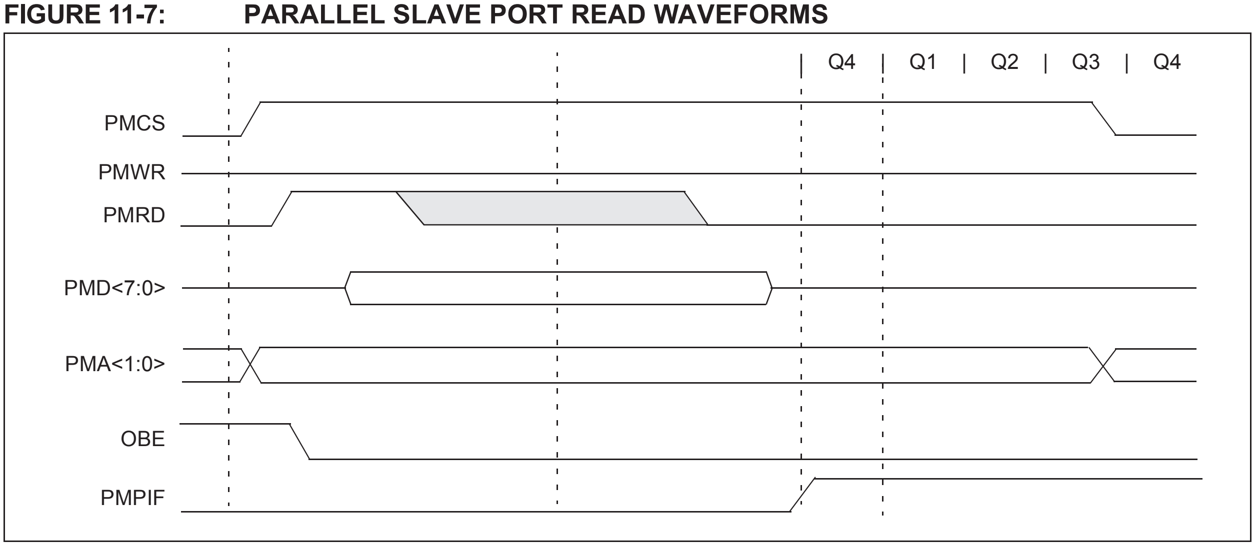
FIGURE 11-6: PARALLEL MASTER/SLAVE CONNECTION ADDRESSED BUFFER EXAMPLE



11.2.5.1 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs (PMCS = 1 and PMRD = 1), the data from one of the four output bytes is presented onto PMD<7:0>. Which byte is read depends on the 2-bit address placed on ADDR<1:0>. Table 11-1 provides the corresponding output registers and their associated address. When an output buffer is read, the corresponding OBxE bit is set. The OBxE flag bit is set when all the buffers are empty. If any buffer is already empty (OBxE = 1), the next read to that buffer will generate an OBUF event.

FIGURE 11-7: PARALLEL SLAVE PORT READ WAVEFORMS



12.1 Timer0 Operation

Timer0 can operate as either a timer or a counter. The mode is selected with the T0CS bit (T0CON<5>). In Timer mode (T0CS = `0`), the module increments on every clock by default unless a different prescaler value is selected (see **Section 12.3 "Prescaler"**). If the TMR0 register is written to, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

The Counter mode is selected by setting the T0CS bit (= `1`). In this mode, Timer0 increments either on every rising edge or falling edge of the pin, T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (T0CON<4>); clearing this bit selects the rising edge. Restrictions on the external clock input are discussed below.

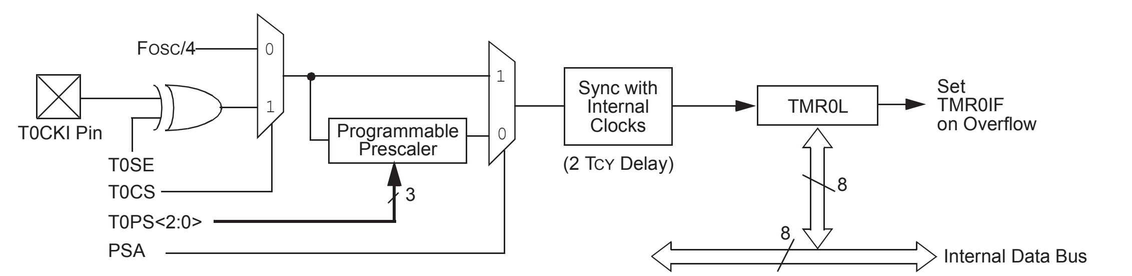
An external clock source can be used to drive Timer0; however, it must meet certain requirements to ensure that the external clock can be synchronized with the internal phase clock (TOSC). There is a delay between synchronization and the onset of incrementing the timer/counter.

12.2 Timer0 Reads and Writes in 16-Bit Mode

TMR0H is not the actual high byte of Timer0 in 16-bit mode. It is actually a buffered version of the real high byte of Timer0, which is not directly readable nor writable (refer to Figure 12-2). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte were valid, due to a rollover between successive reads of the high and low byte.

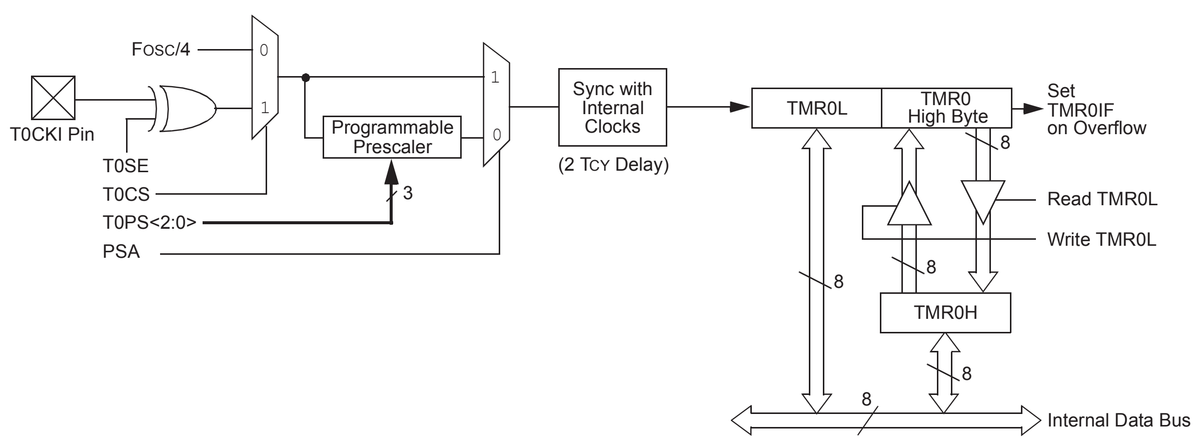
Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

FIGURE 12-1: TIMER0 BLOCK DIAGRAM (8-BIT MODE)



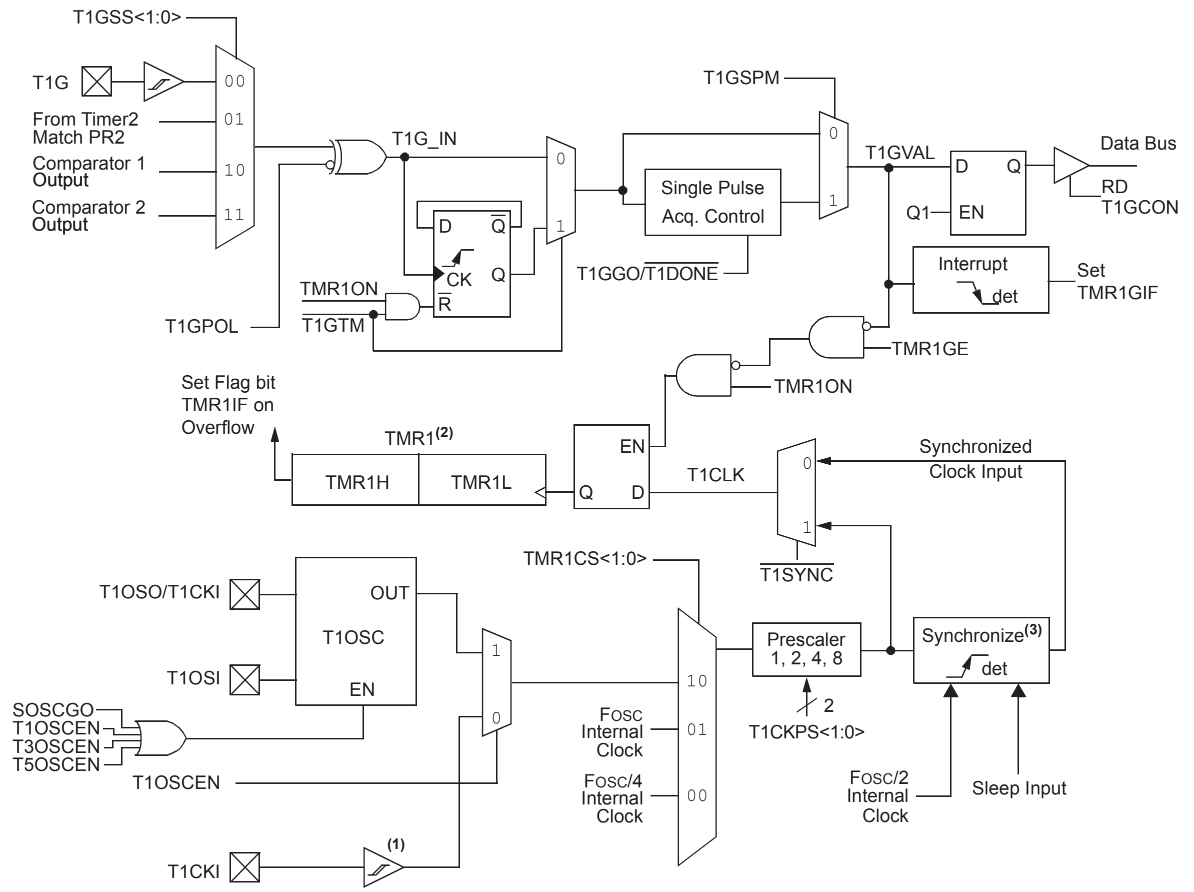
Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

FIGURE 12-2: TIMER0 BLOCK DIAGRAM (16-BIT MODE)



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note 1: ST buffer is high-speed type when using T1CKI.

2: Timer1 register increments on the rising edge.

3: Synchronization does not operate while in Sleep.

13.8.4 TIMER1 GATE SINGLE PULSE MODE

When Timer1 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/$\overline{\text{T1DONE}}$ bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/$\overline{\text{T1DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/$\overline{\text{T1DONE}}$ bit is once again set in software.

Clearing the T1GSPM bit of the T1GCON register will also clear the T1GGO/$\overline{\text{T1DONE}}$ bit. See Figure 13-6 for timing details.

Enabling the Toggle mode and the Single Pulse mode, simultaneously, will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 13-7 for timing details.

13.8.5 TIMER1 GATE VALUE STATUS

When the Timer1 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

FIGURE 13-6: TIMER1 GATE SINGLE PULSE MODE

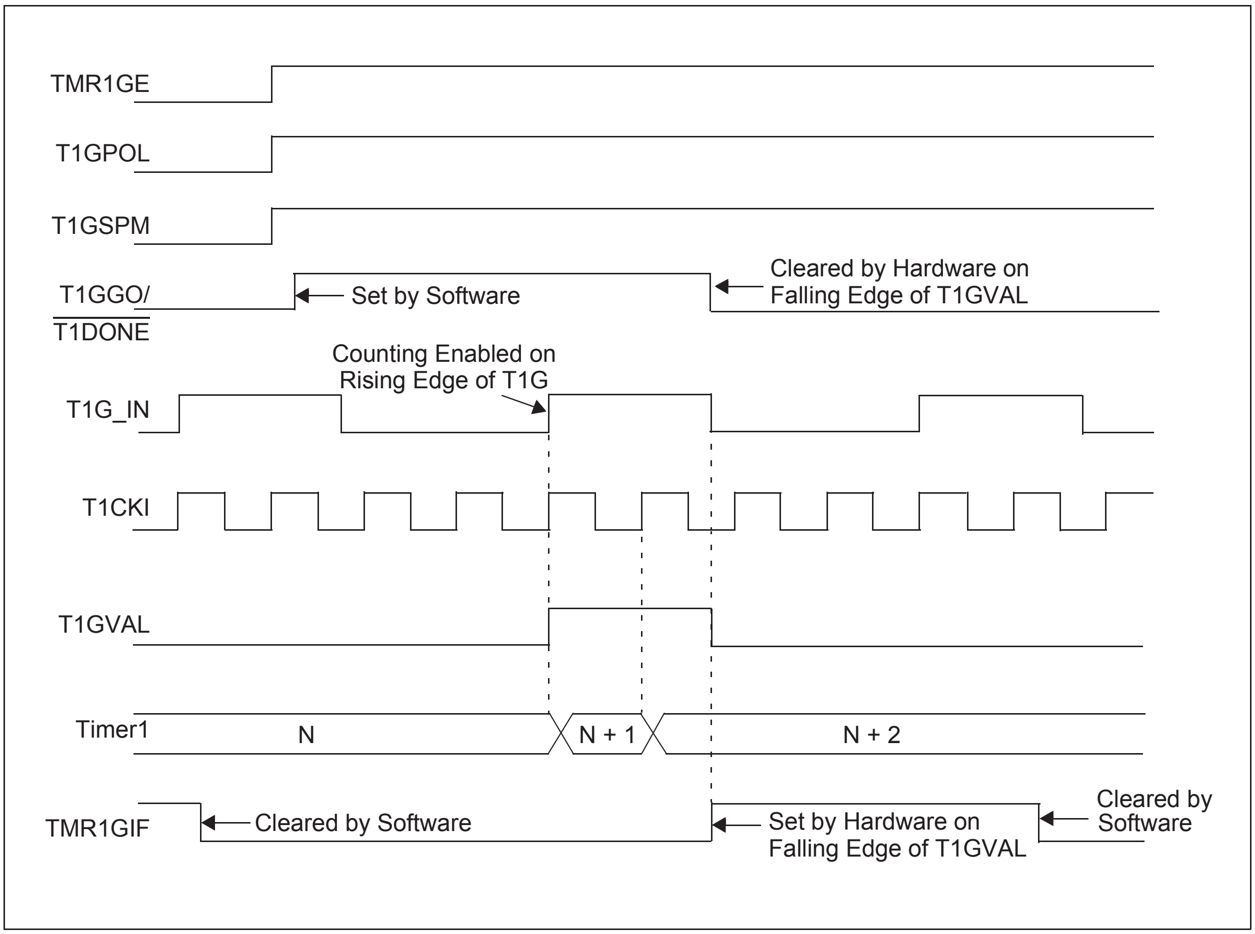


TABLE 18-6: REGISTERS ASSOCIATED WITH PWM AND TIMERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
RCON	IPEN	—	$\overline{\text{CM}}$	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
PIR4	CCP10IF	CCP9IF	CCP8IF	CCP7IF	CCP6IF	CCP5IF	CCP4IF	CCP3IF
PIE4	CCP10IE	CCP9IE	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	CCP3IE
IPR4	CCP10IP	CCP9IP	CCP8IP	CCP7IP	CCP6IP	CCP5IP	CCP4IP	CCP3IP
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
TRISE	$\overline{\text{RDPU}}$	$\overline{\text{REPU}}$	—	—	—	TRISE2	TRISE1	TRISE0
TMR2	Timer2 Register							
TMR4	Timer4 Register							
TMR6	Timer6 Register							
TMR8	Timer8 Register							
PR2	Timer2 Period Register							
PR4	Timer4 Period Register							
PR6	Timer6 Period Register							
PR8	Timer8 Period Register							
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0
T6CON	—	T6OUTPS3	T6OUTPS2	T6OUTPS1	T6OUTPS0	TMR6ON	T6CKPS1	T6CKPS0
T8CON	—	T8OUTPS3	T8OUTPS2	T8OUTPS1	T8OUTPS0	TMR8ON	T8CKPS1	T8CKPS0
CCPR4L	CCPR4L7	CCPR4L6	CCPR4L5	CCPR4L4	CCPR4L3	CCPR4L2	CCPR4L1	CCPR4L0
CCPR4H	CCPR4H7	CCPR4H6	CCPR4H5	CCPR4H4	CCPR4H3	CCPR4H2	CCPR4H1	CCPR4H0
CCPR5L	CCPR5L7	CCPR5L6	CCPR5L5	CCPR5L4	CCPR5L3	CCPR5L2	CCPR5L1	CCPR5L0
CCPR5H	CCPR5H7	CCPR5H6	CCPR5H5	CCPR5H4	CCPR5H3	CCPR5H2	CCPR5H1	CCPR5H0
CCPR6L	CCPR6L7	CCPR6L6	CCPR6L5	CCPR6L4	CCPR6L3	CCPR6L2	CCPR6L1	CCPR6L0
CCPR6H	CCPR6H7	CCPR6H6	CCPR6H5	CCPR6H4	CCPR6H3	CCPR6H2	CCPR6H1	CCPR6H0
CCPR7L	CCPR7L7	CCPR7L6	CCPR7L5	CCPR7L4	CCPR7L3	CCPR7L2	CCPR7L1	CCPR7L0
CCPR7H	CCPR7H7	CCPR7H6	CCPR7H5	CCPR7H4	CCPR7H3	CCPR7H2	CCPR7H1	CCPR7H0
CCPR8L	CCPR8L7	CCPR8L6	CCPR8L5	CCPR8L4	CCPR8L3	CCPR8L2	CCPR8L1	CCPR8L0
CCPR8H	CCPR8H7	CCPR8H6	CCPR8H5	CCPR8H4	CCPR8H3	CCPR8H2	CCPR8H1	CCPR8H0
CCPR9L	CCPR9L7	CCPR9L6	CCPR9L5	CCPR9L4	CCPR9L3	CCPR9L2	CCPR9L1	CCPR9L0
CCPR9H	CCPR9H7	CCPR9H6	CCPR9H5	CCPR9H4	CCPR9H3	CCPR9H2	CCPR9H1	CCPR9H0
CCPR10L	CCPR10L7	CCPR10L6	CCPR10L5	CCPR10L4	CCPR10L3	CCPR10L2	CCPR10L1	CCPR10L0
CCPR10H	CCPR10H7	CCPR10H6	CCPR10H5	CCPR10H4	CCPR10H3	CCPR10H2	CCPR10H1	CCPR10H0
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0
CCP6CON	—	—	DC6B1	DC6B0	CCP6M3	CCP6M2	CCP6M1	CCP6M0
CCP7CON	—	—	DC7B1	DC7B0	CCP7M3	CCP7M2	CCP7M1	CCP7M0
CCP8CON	—	—	DC8B1	DC8B0	CCP8M3	CCP8M2	CCP8M1	CCP8M0
CCP9CON	—	—	DC9B1	DC9B0	CCP9M3	CCP9M2	CCP9M1	CCP9M0
CCP10CON	—	—	DC10B1	DC10B0	CCP10M3	CCP10M2	CCP10M1	CCP10M0
CCPTMRS1	C7TSEL1	C7TSEL0	—	C6TSEL0	—	C5TSEL0	C4TSEL1	C4TSEL0
CCPTMRS2	—	—	—	C10TSEL0	—	C9TSEL0	C8TSEL1	C8TSEL0

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by PWM or Timer2/4/6/8.

20.4 SPI DMA MODULE

The SPI DMA module contains control logic to allow the MSSP2 module to perform SPI direct memory access transfers. This enables the module to quickly transmit or receive large amounts of data with relatively little CPU intervention. When the SPI DMA module is used, MSSP2 can directly read and write to general purpose SRAM. When the SPI DMA module is not enabled, MSSP2 functions normally, but without DMA capability.

The SPI DMA module is composed of control logic, a Destination Receive Address Pointer, a Transmit Source Address Pointer, an interrupt manager and a Byte Count register for setting the size of each DMA transfer. The DMA module may be used with all SPI Master and Slave modes, and supports both half-duplex and full-duplex transfers.

20.4.1 I/O PIN CONSIDERATIONS

When enabled, the SPI DMA module uses the MSSP2 module. All SPI input and output signals, related to MSSP2, are routed through the Peripheral Pin Select module. The appropriate initialization procedure, as described in **Section 20.4.6 "Using the SPI DMA Module"**, will need to be followed prior to using the SPI DMA module. The output pins assigned to the SDO2 and SCK2 functions can optionally be configured as open-drain outputs, such as for level shifting operations mentioned in the same section.

20.4.2 RAM TO RAM COPY OPERATIONS

Although the SPI DMA module is primarily intended to be used for SPI communication purposes, the module can also be used to perform RAM to RAM copy operations. To do this, configure the module for Full-Duplex Master mode operation, but assign the SDO2 output and SDI2 input functions onto the same RPn pin in the PPS module. Also assign SCK2 out and SCK2 in onto the same RPn pin (a different pin than used for SDO2 and SDI2). This will allow the module to operate in Loopback mode, providing RAM copy capability.

20.4.3 IDLE AND SLEEP CONSIDERATIONS

The SPI DMA module remains fully functional when the microcontroller is in Idle mode.

During normal Sleep, the SPI DMA module is not functional and should not be used. To avoid corrupting a transfer, user firmware should be careful to make certain that pending DMA operations are complete by polling the DMAEN bit in the DMACON1 register prior to putting the microcontroller into Sleep.

In SPI Slave modes, the MSSP2 module is capable of transmitting and/or receiving one byte of data while in Sleep mode. This allows the SSP2IF flag in the PIR3 register to be used as a wake-up source. When the DMAEN bit is cleared, the SPI DMA module is effectively disabled, and the MSSP2 module functions normally, but without DMA capabilities. If the DMAEN bit is clear prior to entering Sleep, it is still possible to use the SSP2IF as a wake-up source without any data loss.

Neither MSSP2 nor the SPI DMA module will provide any functionality in Deep Sleep. Upon exiting from Deep Sleep, all of the I/O pins, MSSP2 and SPI DMA related registers will need to be fully re-initialized before the SPI DMA module can be used again.

20.4.4 REGISTERS

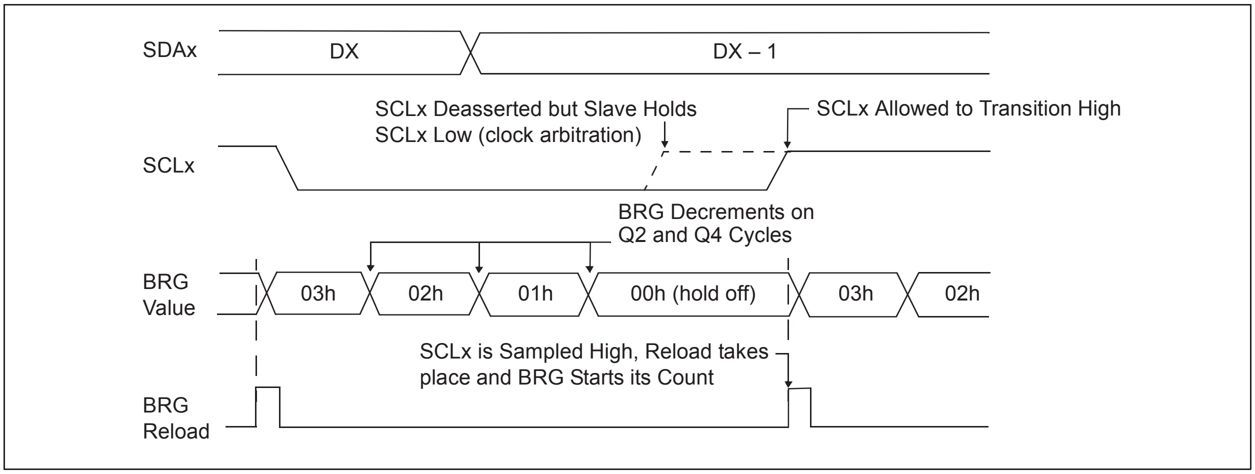
The SPI DMA engine is enabled and controlled by the following Special Function Registers:

- DMACON1
- DMACON2
- TXADDRH
- TXADDRL
- RXADDRH
- RXADDRL
- DMABCH
- DMABCL

20.5.7.2 Clock Arbitration

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, deasserts the SCLx pin (SCLx allowed to float high). When the SCLx pin is allowed to float high, the BRG is suspended from counting until the SCLx pin is actually sampled high. When the SCLx pin is sampled high, the BRG is reloaded with the contents of SSPxADD<6:0> and begins counting. This ensures that the SCLx high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 20-20).

FIGURE 20-20: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



20.5.8 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN (SSPxCON2<0>). If the SDAx and SCLx pins are sampled high, the BRG is reloaded with the contents of SSPxADD<6:0> and starts its count. If SCLx and SDAx are both sampled high when the Baud Rate Generator times out (T_{BRG}), the SDAx pin is driven low. The action of the SDAx being driven low while SCLx is high is the Start condition and causes the Start bit (SSPxSTAT<3>) to be set. Following this, the BRG is reloaded with the contents of SSPxADD<6:0> and resumes its count. When the BRG times out (T_{BRG}), the SEN bit (SSPxCON2<0>) will be automatically cleared by hardware. The BRG is suspended, leaving the SDAx line held low and the Start condition is complete.

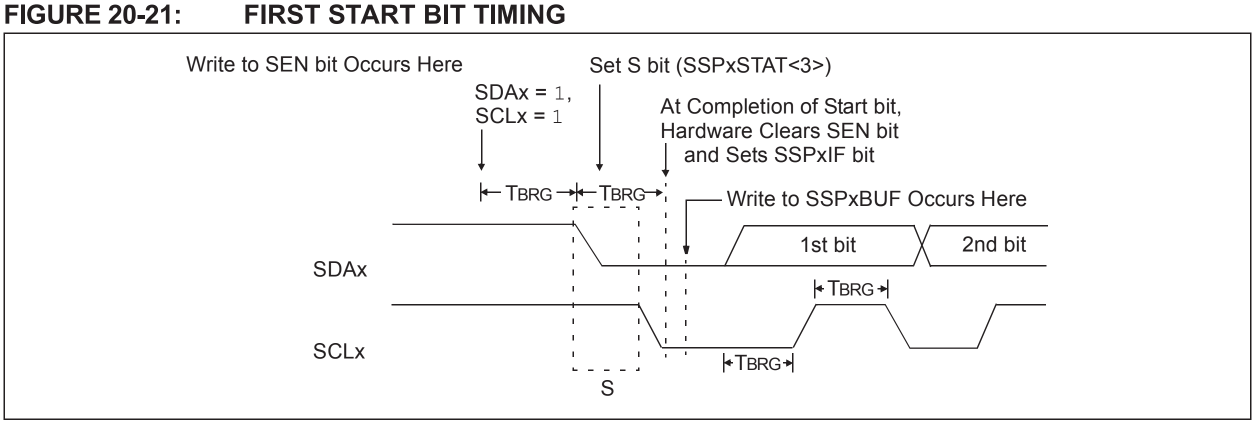
Note:	If, at the beginning of the Start condition, the SDAx and SCLx pins are already sampled low, or if during the Start condition, the SCLx line is sampled low before the SDAx line is driven low, a bus collision occurs. The Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

20.5.8.1 WCOL Status Flag

If the user writes the SSPxBUF when a Start sequence is in progress, the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

Note:	Because queueing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

FIGURE 20-21: FIRST START BIT TIMING



20.5.14 SLEEP OPERATION

While in Sleep mode, the I^{2}C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

20.5.15 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

20.5.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Start and Stop bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^{2}C bus may be taken when the P bit (SSPxSTAT<4>) is set, or the bus is Idle, with both the Start and Stop bits clear. When the bus is busy, enabling the MSSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDAx line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

20.5.17 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDAx pin, arbitration takes place when the master outputs a '1' on SDAx, by letting SDAx float high, and another master asserts a '0'. When the SCLx pin floats high, data should be stable. If the expected data on SDAx is a '1' and the data sampled on the SDAx pin = 0, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF, and reset the I^{2}C port to its Idle state (Figure 20-27).

If a transmit was in progress when the bus collision occurred, the transmission is Halted, the BF flag is cleared, the SDAx and SCLx lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine, and if the I^{2}C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDAx and SCLx lines are deasserted, and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine (ISR), and if the I^{2}C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDAx and SCLx pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^{2}C bus can be taken when the Stop bit is set in the SSPxSTAT register, or the bus is Idle and the Start and Stop bits are cleared.

FIGURE 20-27: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

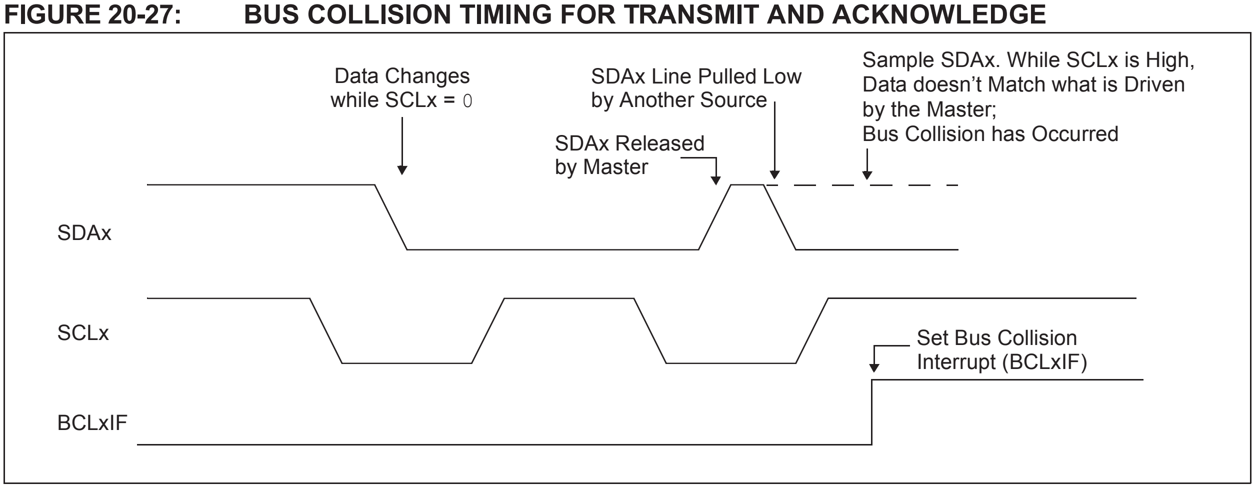


TABLE 21-3: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0											
	FOSC = 40.000 MHz			FOSC = 20.000 MHz			FOSC = 10.000 MHz			FOSC = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	—	—	—
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	—	—
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0								
	FOSC = 4.000 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—
9.6	8.929	-6.99	6	—	—	—	—	—	—
19.2	20.833	8.51	2	—	—	—	—	—	—
57.6	62.500	8.51	0	—	—	—	—	—	—
115.2	62.500	-45.75	0	—	—	—	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0											
	FOSC = 40.000 MHz			FOSC = 20.000 MHz			FOSC = 10.000 MHz			FOSC = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9615.	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0								
	FOSC = 4.000 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	0.300	-0.16	207
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25
9.6	9.615	0.16	25	9.615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

30.2 DC Characteristics: Power-Down and Supply Current PIC18F47J13 Family (Industrial) (Continued)

PIC18LF47J13 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial					
PIC18F47J13 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (I_{DD})(2)						
	PIC18LFXXJ13	0.41	0.98	mA	-40°C	V_{DD} = 2.0V, V_{DDCORE} = 2.0V	F_{OSC} = 4 MHz, **RC_IDLE** mode, Internal RC Oscillator
		0.44	0.98	mA	+25°C		
		0.48	1.12	mA	+85°C		
	PIC18LFXXJ13	0.48	1.14	mA	-40°C	V_{DD} = 2.5V, V_{DDCORE} = 2.5V	
		0.51	1.14	mA	+25°C		
		0.55	1.25	mA	+85°C		
	PIC18FXXJ13	0.45	1.21	mA	-40°C	V_{DD} = 2.15V, V_{DDCORE} = 10 μF	
		0.49	1.21	mA	+25°C		
		0.52	1.30	mA	+85°C		
	PIC18FXXJ13	0.52	1.20	mA	-40°C	V_{DD} = 3.3V, V_{DDCORE} = 10 μF	
		0.54	1.20	mA	+25°C		
		0.58	1.35	mA	+85°C		
	PIC18LFXXJ13	0.53	1.4	mA	-40°C	V_{DD} = 2.0V, V_{DDCORE} = 2.0V	F_{OSC} = 8 MHz, **RC_IDLE** mode, Internal RC Oscillator
		0.56	1.5	mA	+25°C		
		0.60	1.6	mA	+85°C		
	PIC18LFXXJ13	0.63	2.0	mA	-40°C	V_{DD} = 2.5V, V_{DDCORE} = 2.5V	
		0.67	2.0	mA	+25°C		
		0.72	2.2	mA	+85°C		
	PIC18FXXJ13	0.58	1.8	mA	-40°C	V_{DD} = 2.15V, V_{DDCORE} = 10 μF	
		0.62	1.8	mA	+25°C		
		0.66	2.0	mA	+85°C		
	PIC18FXXJ13	0.69	2.2	mA	-40°C	V_{DD} = 3.3V, V_{DDCORE} = 10 μF	
		0.70	2.2	mA	+25°C		
		0.74	2.3	mA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to V_{DD} or V_{SS}, and all features that add delta current are disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (such as WDT). The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}/V_{SS};
$\overline{MCLR}$ = V_{DD}; WDT disabled unless otherwise specified.

3: Low-power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

30.2 DC Characteristics: Power-Down and Supply Current PIC18F47J13 Family (Industrial) (Continued)

PIC18LF47J13 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for industrial					
PIC18F47J13 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔI_{WDT}, ΔI_{HLVD}, ΔI_{OSCB}, ΔI_{AD})						
D026 (ΔI_{AD})	**A/D Converter**	0.5	4	μA	-40°C	V_{DD} = 2.5V, V_{DDCORE} = 2.5V	PIC18LFXXJ13 A/D on, not converting
		0.5	4	μA	+25°C		
		0.5	4	μA	+85°C		
		1.1	5	μA	-40°C	V_{DD} = 2.15V, V_{DDCORE} = 10 μF Capacitor	PIC18FXXJ13 A/D on, not converting
		1.1	5	μA	+25°C		
		1.1	5	μA	+85°C		
		3.2	11	μA	-40°C	V_{DD} = 3.3V, V_{DDCORE} = 10 μF Capacitor	
		3.2	11	μA	+25°C		
		3.2	11	μA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to V_{DD} or V_{SS}, and all features that add delta current are disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (such as WDT). The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}/V_{SS};
$\overline{\text{MCLR}}$ = V_{DD}; WDT disabled unless otherwise specified.

3: Low-power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

