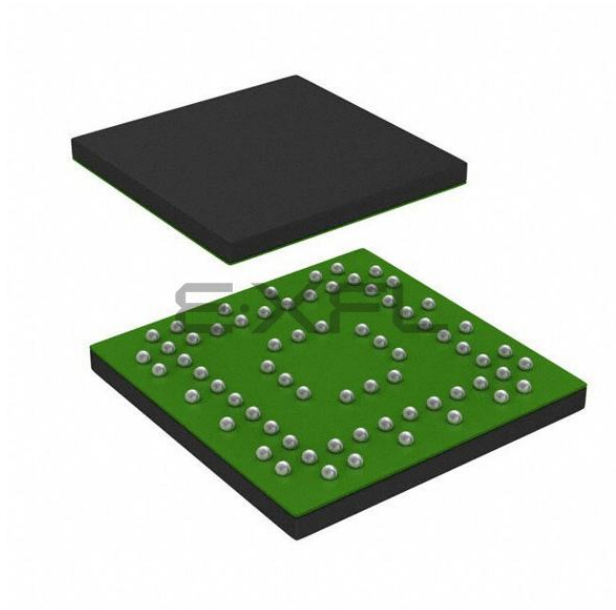

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8024 Keyboard Controller
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	LPC, Serial, UART
Number of I/O	19
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFBGA
Supplier Device Package	64-WFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3223-7u-tr

TABLE 2-2: SCH3223 PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR Power Plane	VCC=0 Operation (Note 2-10)	Buffer Modes (Note 2-1)
MISCELLANEOUS PINS						
	GP42/ nIO_PME	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in either S3 or S5 and below.		GP42/ nIO_PME	NO GATE	(I/O12/OD12) /(O12/OD12)
2-6, 2-7	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output		GP60 /nLED1 /WDT	NO GATE	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
	nFPRST / GP30	Front Panel Reset / General Purpose IO		nFPRST / GP30	NO GATE	ISPU_400 / (I/O4/OD4)
	PWRGD_PS	Power Good Input from Power Supply		PWRGD_PS	NO GATE	ISPU_400
	PWRGD_OUT	Power Good Output – Open Drain		PWRGD_ OUT	NO GATE	OD8
	nRSMRST	Resume Reset Output		nRSMRST	NO GATE	OD24
2-6, 2-7	GP61 /nLED2 / CLKO	General Purpose I/O /nLED2 / Programmable Clock Output		GP61 /nLED2 / CLKO	NO GATE	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-7	GP27 /nIO_SMI	General Purpose I/O /System Mgt. Interrupt	GP27 /nIO_SMI	GP27	/ HI-Z	(I/O12/OD12) /(O12/OD12)
	TEST	Test purposes. Customer should tie this pin to VSS at all times.	TEST	TEST		
HARDWARE MONITORING BLOCK						
2-8	+5V_IN	Analog input for +5V	HVTR			I_{AN}
2-8	+2.5_IN	Analog input for +2.5V	HVTR			I_{AN}
2-8	VCCP_IN	Analog input for +Vccp (processor voltage: 1.5 V nominal).	HVTR			I_{AN}
2-8	+12V_IN	Analog input for +12V	HVTR			I_{AN}
	REMOTE1-	This is the negative input (current sink) from the remote thermal diode 1.	HVTR			I_{AND-}
	REMOTE1+	This is the positive input (current source) from the remote thermal diode 1.	HVTR			I_{AND+}
	PWM1	Fan Speed Control 1 Output.		PWM1		OD8
	FANTACH1	Tachometer Input 1 for monitoring a fan.		FANTACH 1		I_M
RESET OUTPUTS						
	nPCIRST3 / GP47	PCI Reset output 3 GPIO with Schmitt trigger input	nPCIRST3	GP47	NO GATE	(O4/OD4) / (IS/O4/OD4)
	nPCIRST2 / GP46	PCI Reset output 2 GPIO with Schmitt trigger input	nPCIRST2	GP46	NO GATE	(O8/OD8) / (IS/O8/OD8)

4.0 POWER FUNCTIONALITY

The SCH3223 has five power planes: VCC, HVTR, VREF, VTR, and Vbat.

4.1 VCC Power

The SCH3223 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). VCC is the main power supply for the Super I/O Block. See Section 25.2, "DC Electrical Characteristics," on page 170.

4.2 HVTR Power

The HVTR supply is 3.3 Volts (nominal). HVTR is a dedicated power supply for the Hardware Monitoring Block. HVTR is connected to the VTR suspend well. See Section 25.2, "DC Electrical Characteristics," on page 170.

Note:	The hardware monitoring logic is powered by HVTR, but only operational when VCC is on. The hardware monitoring block is connected to the suspend well to retain the programmed configuration through a sleep cycle.

4.3 VTR Support

The SCH3223 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See Section 25.0, "Operational Description," on page 170. The maximum VTR current that is required depends on the functions that are used in the part. See Section 25.0.

If the SCH3223 is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. VTR powers the IR interface, the PME configuration registers, and the PME interface. The VTR pin generates a VTR Power-on-Reset signal to initialize these components. If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 ms before Vcc begins a power-on cycle. Note that under all circumstances, the hardware monitoring HVTR must be driven as the same source as VTR.

4.3.1 TRICKLE POWER FUNCTIONALITY

When the SCH3223 is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP27, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are PME wakeup as a GPIO (or alternate function).

The other GPIOs function as follows:

GP42, GP60 and GP61:

- Buffers powered by VTR. GP42 is the nIO_PME pin which is active under VTR. GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- PME runtime register block (includes all PME, SMI, GPIO, Fan and other miscellaneous registers)
- Digital logic in the Hardware Monitoring block
- LED control logic
- Watchdog Timer

Bit 7

This bit is permanently set to logic “0” in the 450 mode. In the FIFO mode, this bit is set to a logic “1” when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

7.1.9 MODEM STATUS REGISTER (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic “1” whenever a control input from the MODEM changes state. They are reset to logic “0” whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic “0” to logic “1”.

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note:	Whenever bit 0, 1, 2, or 3 is set to a logic “1”, a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to OUT1 in the MCR.

Bit 7

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to OUT2 in the MCR.

7.1.10 SCRATCHPAD REGISTER (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

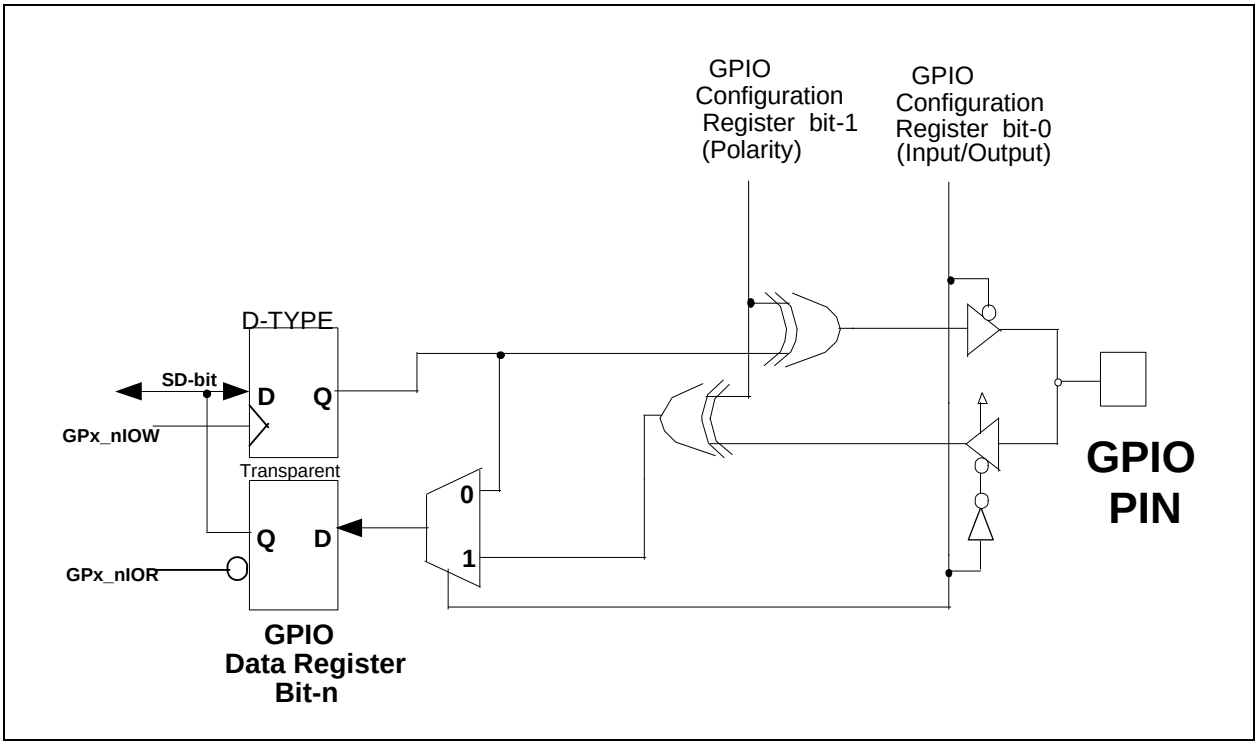
7.1.11 PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3.

TABLE 7-7: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL

Register Address (Note 7-4)	Register Name	Register Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (Note 7-5)
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	0	0	0	0	Enable MODEM Status Interrupt (EMSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Received Data Available Interrupt (ERDAI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	FIFOs Enabled (Note 7-9)	FIFOs Enabled (Note 6)	0	0	Interrupt ID Bit (Note 7-9)	Interrupt ID Bit	Interrupt ID Bit	“0” if Interrupt Pending
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 7-11)	RCVR Trigger MSB	RCVR Trigger LSB	Reserved	Reserved	DMA Mode Select (Note 7-10)	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
ADDR = 3	Line Control Register	LCR	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
ADDR = 4	MODEM Control Register	MCR	0	0	0	Loop	OUT2 (Note 7-7)	OUT1 (Note 7-7)	Request to Send (RTS)	Data Terminal Ready (DTR)
ADDR = 5	Line Status Register	LSR	Error in RCVR FIFO (Note 7-9)	Transmitter Empty (TEMT) (Note 7-6)	Transmitter Holding Register (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
ADDR = 6	MODEM Status Register	MSR	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
ADDR = 7	Scratch Register (Note 7-8)	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

FIGURE 10-1: GPIO FUNCTION ILLUSTRATION



Note: Figure 10-1 is for illustration purposes only and is not intended to suggest specific implementation details.

TABLE 10-4: GPIO READ/WRITE BEHAVIOR

Host Operation	GPIO Input Port	GPIO Output Port
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

10.5 GPIO PME and SMI Functionality

The SCH3223 provides GPIOs that can directly generate a PME. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in a PME Status. For additional description of PME behavior see Section 12.0, "PME Support," on page 46. The default is the low-to-high transition. In addition, the SCH3223 provides GPIOs that can directly generate an SMI.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP27 is controlled by PME_STS3, PME_EN3 registers.

GP50-GP57 are controlled by PME_STS5, PME_EN5 registers.

GP60, GP61 are controlled by PME_STS6, and PME_EN6 registers.

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP54, GP55, GP56, GP57, GP60 are controlled by SMI_STS3, and SMI_EN3 registers.

GP42, GP61 are controlled by SMI_STS4, and SMI_EN4 registers.

The following GPIOs have "either edge triggered interrupt" (EETI) input capability: GP60, GP61. These GPIOs can generate a PME and an SMI on both a high-to-low and a low-to-high edge on the GPIO pin. These GPIOs have a status bit in the PME_STS6 status register that is set on both edges. The corresponding bits in the PME and SMI status registers are also set on both edges.

14.0 PROGRAMMABLE CLOCK OUTPUT

A CLK_OUT pin is available on the SCH3223. This will output a programmable frequency between 0.5 Hz to 16 Hz, and have the following characteristics:

- Must run when Vcc if off - could use 32Khz clock
- Accuracy is not an issue
- CLOCK_OUT register at offset 3Ch in runtime registers with the following programming:
  - Options for 0.25, 0.5, 1, 2, 4, 8, or 16 Hz

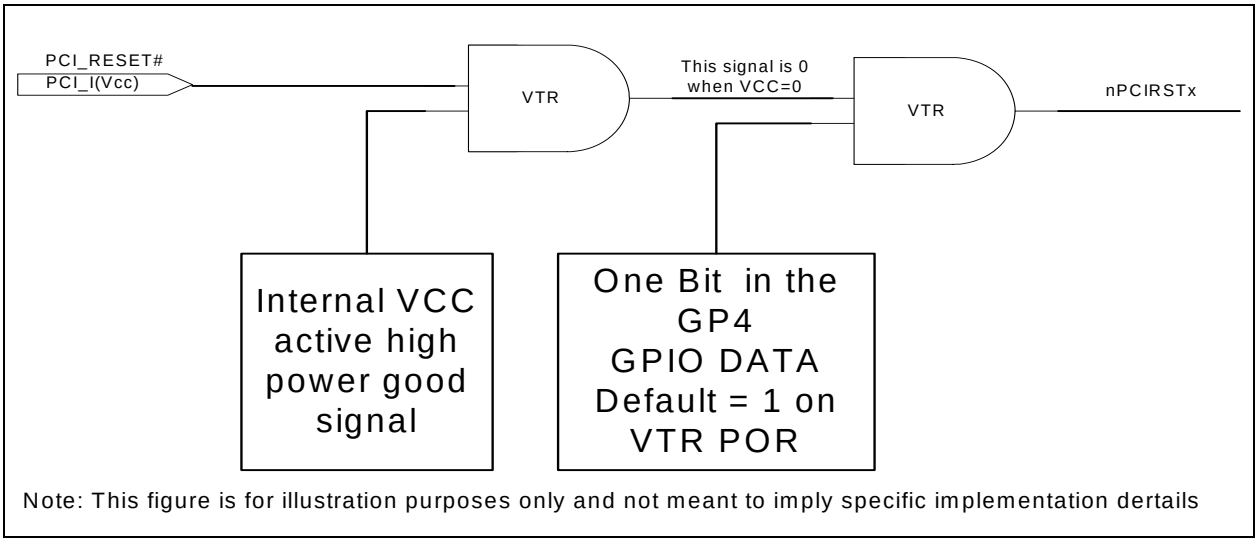
APPLICATION NOTE: No attempt has been made to synchronize the clock. As a result, glitches will occur on the clock output when different frequencies are selected.

CLOCK Output Control Register VTR POR = 0x00	3C (R/W)	Bit[0] Enable 1= Output Enabled 0= Disable Clock output Bit[3:1] Frequency Select 000= 0.25 Hz 001= 0.50 Hz 010= 1.00 Hz 011= 2.00 Hz 100= 4.00 Hz 101= 8.00 Hz 110= 16 hz 111 = reserved Bit[7:4] Reserved

When the VTR power is applied, VCC is powered down, and the GPIO control register's contents are default, the nPCIRSTx pin output is low.

The Figure 16-1 illustrates the nPCIRSTx function. The figure is for illustration purposes only and in not intended to suggest specific implementation details.

FIGURE 16-1: NPCIRSTX LOGIC



Note: This figure is for illustration purposes only and not meant to imply specific implementation dertails

17.0 POWER CONTROL FEATURES

The SCH3223 device is able to turn on the power supply when the power button located on the PC chassis is pressed, or when recovering from a power failure. The signals used to support these features are:

- PB_IN#
- PB_OUT#
- SLP_Sx#
- PS_ON#

Table 17-1 and Figure 17-1 describe the interface and connectivity of the following Power Control Features:

1. Front Panel Reset with Input Debounce, Power Supply Gate, and Powergood Output Signal Generation
2. AC Recovery Circuit
3. SLP_Sx# PME wakeup

TABLE 17-1: POWER CONTROL INTERFACE

Name	Direction	Description
PB_IN#	Input	Power Button Input
PB_OUT#	Output	Power Good Output
PS_ON#	Output	Power Supply On output
SLP_SX#	Input	From south bridge
PWRGD_PS	Input	Power Good Input from Power Supply
nFPRST	Input	Reset Input from Front Panel
PWRGD_OUT	Output	Power Good Output – Open Drain
nIO_PME	Output	Power Management Event Output signal allows this device to request wakeup.

19.0 BATTERY BACKED SECURITY KEY REGISTER

Located at the Secondary Base I/O Address of Logical Device A is a 32 byte CMOS memory register dedicated to security key storage. This security key register is battery powered and has the option to be read protected, write protected, and lockable. The Secondary Base I/O Address is programmable at offsets 0x62 and 0x63. Table 19-1, "Security Key Register Summary" is a complete list of the Security Key registers.

TABLE 19-1: SECURITY KEY REGISTER SUMMARY

Register Offset (HEX)	Vbat POR	Register
00	0x00	Security Key Byte 0
01	0x00	Security Key Byte 1
02	0x00	Security Key Byte 2
03	0x00	Security Key Byte 3
04	0x00	Security Key Byte 4
05	0x00	Security Key Byte 5
06	0x00	Security Key Byte 6
07	0x00	Security Key Byte 7
08	0x00	Security Key Byte 8
09	0x00	Security Key Byte 9
0A	0x00	Security Key Byte 10
0B	0x00	Security Key Byte 11
0C	0x00	Security Key Byte 12
0D	0x00	Security Key Byte 13
0E	0x00	Security Key Byte 14
0F	0x00	Security Key Byte 15
10	0x00	Security Key Byte 16
11	0x00	Security Key Byte 17
12	0x00	Security Key Byte 18
13	0x00	Security Key Byte 19
14	0x00	Security Key Byte 20
15	0x00	Security Key Byte 21
16	0x00	Security Key Byte 22
17	0x00	Security Key Byte 23
18	0x00	Security Key Byte 24
19	0x00	Security Key Byte 25
1A	0x00	Security Key Byte 26
1B	0x00	Security Key Byte 27
1C	0x00	Security Key Byte 28
1D	0x00	Security Key Byte 29
1E	0x00	Security Key Byte 30
1F	0x00	Security Key Byte 31

Access to the Security Key register block is controlled by bits [2:1] of the Security Key Control (SKC) Register located in the Configuration Register block, Logical Device A, at offset 0xF2. The following table summarizes the function of these bits.

occurred and the Tach Reading register will be set to either FFFEh or FFFFh depending on the state of the Slow Tach bits located in the TACHx Options registers at offsets 90h - 93h. Software can easily compute the RPM value using the tachometer reading value if it knows the number of edges per revolution.

Note 1: If the PWM output associated with a tach input is configured for the high frequency option then the tach input must be configured for Mode 1.

2: Some enhanced features added to support Mode 2, are available to Mode 1 also. They are: programmable number of tach edges and force tach reading register to FFFEh to indicate a SLOW fan.

3: Five edges or two tach pulses are generated per revolution.

4: If a tach input is left unconnected it must be configured for Mode 1.

20.14.2.4 Mode 2 – Monitor Tach input When PWM is 'ON'

In this mode, the PWM is used to pulse the Fan motor of a 3-wire fan. 3-wire fans use the same power supply to drive the fan motor and to drive the tachometer output logic. When the PWM is 'ON' the fan generates valid tach pulses. When the PWM is not driving the Fan, the tachometer signal is not generated and the tach signal becomes indeterminate or tristate. Therefore, Mode 2 only makes tachometer measurements when the associated PWM is driving high during an update cycle. As a result, the Fan tachometer measurement is "synchronized" to the PWM output, such that it only looks for tach pulses when the PWM is 'ON'.

Note:	Any fan tachometer input may be associated with any PWM output (see Linking Fan Tachometers to PWMs on page 98.)

During an update cycle, if an insufficient number of tachometer pulses are detected during this time period, the following applies: If at least one edge but less than the programmed number of edges is detected, the fan is considered slow. If no edge is detected, the fan is considered stopped.

Note 1: The interrupt status bits are set, if enabled, to indicate that a slow or stopped fan event has occurred when the tach reading registers are greater than the tach limit registers.

2: At some duty cycles, the programmed number of edges will appear during some PWM High times, but not all. If opportunistic mode is enabled, the tach logic will latch the count value any time it detects the programmed number of edges and reset the update counter. An interrupt will only be generated if no valid readings were made during the programmed update time.

20.14.2.5 Assumptions (refer to Figure 4 - PWM and Tachometer Concept):

The Tachometer pulse generates 5 transitions per fan revolution (i.e., two fan tachometer periods per revolution, edges 2→6). One half of a revolution (one tachometer period) is equivalent to three edges (2→4 or 3→5). One quarter of a revolution (one-half tachometer period) is equivalent to two edges. To obtain the fan speed, count the number of 90Khz pulses that occurs between 2 edges i.e., 2→3, between 3 edges i.e., 2→4, or between 5 edges, i.e. 2→6 (the case of 9 edges is not shown). The time from 1-2 occurs through the guard time and is not to be used. For the discussion below, an edge is a high-to-low or low-to-high transition (edges are numbered – refer to Figure 4 - PWM and Tachometer Concept.

The Tachometer circuit begins monitoring the tach when the associated PWM output transitions high and the guard time has expired. Each tach circuit will continue monitoring until either the "ON" time ends or the programmed number of edges has been detected, whichever comes first.

The Fan Tachometer value may be updated every 300ms, 500ms, or 1000ms.

21.2.7 REGISTER 3EH: COMPANY ID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	5Ch

The company ID register contains a unique value to allow software to identify Microchip devices that been implemented in a given system.

21.2.8 REGISTER 3FH: REVISION

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Fh	R	Revision	7	6	5	4	3	2	1	0	01h

The Revision register contains the current version of this device.

The register is used by application software to identify which version of the device has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping.

This register is read only – a write to this register has no effect.

21.2.9 REGISTER 40H: READY/LOCK/START MONITORING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
40h	R/W	Ready/Lock/Start	RES	RES	RES	RES	OVRID	READY	LOCK Note 21 -15	START	04h

Note 21-15 This LOCK bit is cleared when PWRGD_PS is asserted.

Setting the Lock bit makes the Lock and Start bits read-only.

Bit	Name	R/W	Default	Description
0	START	R/W	0	When software writes a 1 to this bit, the SCH3223 enables monitoring and PWM output control functions based on the limit and parameter registers. Before this bit is set, the part does not update register values. Whenever this bit is set to 0, the monitoring and PWM output control functions are based on the default limits and parameters, regardless of the current values in the limit and parameter registers. The SCH3223 preserves the values currently stored in the limit and parameter registers when this bit is set or cleared. This bit becomes read only when the Lock bit is set. **Note 1:** When this bit is 0, all fans are on full 100% duty cycle, i.e., PWM pins are high for 255 clocks, low for 1 clock. When this bit is 0, the part is not monitoring. **2:** It is suggested that software clear the START bit and exit auto fan control mode before modifying any fan configuration registers. After clearing the START bit, software should wait for a period of one 90kHz-10% clock (~12.5usec) before setting the START bit back to '1' to ensure the fan logic exited auto mode when START was cleared.
1	LOCK	R/W Note 21-16	0	Setting this bit to 1 locks specified limit and parameter registers. Once this bit is set, limit and parameter registers become read only and will remain locked until the device is powered off. This register bit becomes read only once it is set.

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at high speeds (100% duty cycle), so care should be taken in software to ensure that the limit is low enough not to cause sporadic alerts. Note that an interrupt status event will be generated when the tachometer reading is greater than the minimum tachometer limit.

The fan tachometer will not cause a bit to be set in the interrupt status register if the current value in the associated Current PWM Duty registers is 00h or if the PWM is disabled via the PWM Configuration Register.

Interrupts will never be generated for a fan if its tachometer minimum is set to FFFFh.

21.2.15 REGISTERS 5C-5EH: PWM CONFIGURATION

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Ch	R/W	PWM 1 Configuration	ZON2	ZON1	ZON0	INV	SUEN1	SPIN2	SPIN1	SPIN0	62h
5Dh	R/W	PWM 2 Configuration	ZON2	ZON1	ZON0	INV	SUEN2	SPIN2	SPIN1	SPIN0	62h
5Eh	R/W	PWM 3 Configuration	ZON2	ZON1	ZON0	INV	SUEN3	SPIN2	SPIN1	SPIN0	62h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits [7:5] Zone/Mode

Bits [7:5] of the PWM Configuration registers associate each PWM with a temperature zone.

- When in Auto Fan Mode, the PWM will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If 'Hottest' option is selected (101 or 110), the PWM will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. If one of these options is selected, the PWM is controlled by the limits and parameters for the zone that requires the highest PWM duty cycle, as computed by the auto fan algorithm.
- When in manual control mode, the PWMx Current Duty Cycle Registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. See PWMx Current Duty Cycle Registers description.
- When the fan is disabled (100) the corresponding PWM output is driven low (or high, if inverted).
- When the fan is Full On (011) the corresponding PWM output is driven high (or low, if inverted).

Note 1: Zone 1 is controlled by Remote Diode 1 Temp Reading register

2: Zone 2 is controlled by the Ambient Reading Register.

3: Zone 3 is controlled by Remote Diode 2 Temp Reading register

TABLE 21-7: FAN ZONE SETTING

ZON[7:5]	PWM Configuration
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2,3
110	Fan controlled by hottest of zones 1,2,3
111	Fan manually controlled

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 1, 100% duty cycle will yield an output that is low for 255 clocks and high for 1 clock. If set to 0, 100% duty cycle will yield an output that is high for 255 clocks and low for 1 clock.

Bit [3] Forced Spin-up Enable

Bit [3] enables the forced spin up option for a particular PWM. If set to 1, the forced spin-up feature is enabled for the associated PWM. If set to 0, the forced spin-up feature is disabled for the associated PWM.

APPLICATION NOTE: This bit should always be enabled (set) to prevent fan tachometer interrupts during spinup.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to '1' if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

21.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default)

21.2.67 REGISTER CEH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CEh	R/W		RES	RES	RES	RES	RES	RD2 _INT_ EN	RD1 _INT_ EN	AMB_ INT_ EN	00h

21.2.68 REGISTERS D1,D6,DBH: PWM MAX SEGMENT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
0D1h	R/W	PWM1 Max	7	6	5	4	3	2	1	0	FFh
0D6h	R/W	PWM2 Max	7	6	5	4	3	2	1	0	FFh
0DBh	R/W	PWM3 Max	7	6	5	4	3	2	1	0	FFh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Registers 0D1h, 0D6h and 0DBh are used to program the Max PWM duty cycle for the fan function for each PWM.

21.2.69 REGISTER E0H: ENABLE LSBS FOR AUTO FAN

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
E0h	R/W	Enable LSbs for AutoFan	RES	RES	PWM3_ n1	PWM3_ n0	PWM2_ n1	PWM2_ n0	PWM1_ n1	PWM1_ n0	00h

Bits[7:6] Reserved

Bits[5:4] PWM3_n[1:0]

Bits[3:2] PWM2_n[1:0]

Bits[1:0] PWM1_n[1:0]

The PWMx_n[1:0] configuration bits allow the autofan control logic to utilize the extended resolution bits in the temperature reading. Increasing the precision reduces the programmable temperature range that can be used to control the PWM outputs. For a description of the programmable temperature ranges see Registers 5F-61h: Zone Temperature Range, PWM Frequency on page 116.

TABLE 22-6: LOGICAL DEVICE REGISTERS (CONTINUED)

Logical Device Register	Address	Description
DMA Selection	(0x74,0x75)	Reserved - not supported in the SCH3223. Do not attempt to alter these registers in any Logical Device.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see MCHP defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Note 22-4 A logical device will be active and powered up according to the following equation unless otherwise specified:
DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).
The Logical Device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 22-5 If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

TABLE 22-7: BASE I/O RANGE FOR LOGICAL DEVICES

Logical Device Number	Logical Device	Register Index	Base I/O Range (Note 22-6)	Fixed Base Offsets
0x00	Reserved	n/a	n/a	n/a
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Reserved	n/a	n/a	n/a
0x04	Serial Port 1	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x05	Serial Port 2	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x06	Reserved	n/a	n/a	n/a
0x07	Reserved	n/a	n/a	n/a
0x08	Reserved	n/a	n/a	n/a
0x09	Reserved	n/a	n/a	n/a
0x0A	Runtime Register Block	0x60,0x61	[0x0000:0x0F7F] on 128-byte boundaries	See Table 23-1, "Runtime Register Summary," on page 150
	Security Key Register	0x62, 0x63	[0x0000:0x0FDF on 32-byte boundaries	+00 : Security Key Byte 0 . . . +1F: Security Key Byte 31
0x0B	Reserved	n/a	n/a	n/a

TABLE 22-11: LOGICAL DEVICE A [LOGICAL DEVICE NUMBER = 0X0A]

Name	REG Index	Definition
CLOCKI32 Default = 0x00 on VTR POR	0xF0 (R/W)	Bit[0] (CLK32_PRSN) 0 = 32kHz clock is connected to the CLKI32 pin (default) 1 = 32kHz clock is not connected to the CLKI32 pin (pin is grounded) Bit[1] Reserved. Do not alter from reset state. Bit[2] Reserved (read-only bit) Bit[3] Reserved. Do not alter from reset state. Bits[7:4] are reserved
Reserved Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Reserved. Do not alter from default value.
Security Key Control (SKC) Register Default=0x04 on a VTR POR, VCC POR, PCI Reset	0xF2 R/W when bit[0]= 0 Read-Only when bit[0]=1	Bit[0] SKC Register Lock This bit blocks write access to the Security Key Control Register. 0 = Security Key Control Register is a Read/Write register (default) 1 = Security Key Control Register is a Read-Only register Bit[1] Read-Lock This bit prevents reads from the Security Key registers located at an offset from the Secondary Base I/O address in Logical Device A 0 = Permits read operations in the Security Key block (default) 1 = Prevents read operations in the Security Key block (Reads return 00h.) Bit[2] Write-Lock This bit prevents writes to the Security Key registers located at an offset from the Secondary Base I/O address in Logical Device A 0 = Permits write operations in the Security Key block 1 = Prevents write operations in the Security Key block (default) Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved

Note: The registers located in Logical Device A are runtime registers.

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SMI_STS1 Default = 0x02, or 0x03 on VTR POR. The default will be 0x03 if there is a LOW_BAT event under VBAT power only, or 0x02 if this event does not occur. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] Reserved Bit[2] U2INT Bit[3] U1INT Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	Bit[7:0] Reserved
SMI_STS3 Default = 0x00 on VTR POR	16 (R/WC)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] Reserved Bit[2] Reserved Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_STS4 Default = 0x00 on VTR POR (Note 23-14)	17 (R/WC)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] Reserved Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] GP42 Bit[6] Reserved Bit[7] GP61
SMI_EN1 Default = 0x00 on VTR POR	18 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nIO_SMI output. 1=Enable 0=Disable Bit[0] EN_LOW_BAT Bit[1] Reserved Bit[2] EN_U2INT Bit[3] EN_U1INT Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] EN_WDT

TABLE 25-1: BUFFER OPERATIONAL RATINGS (CONTINUED)

SUPER I/O BLOCK (T_A INDUSTRIAL = -40°C – +85°C, V_{CC} = +3.3 V ± 10%) OR (T_A COMMERCIAL = 0°C – +70°C, V_{CC} = +3.3 V ± 10%)						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Comments**
IO12 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IOP14 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
IOD16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OD_PH Type Buffer	VOL			0.3	V	RLOAD is 40ohms to 1.2V Max Output impedance is 10ohms
PCI Type Buffers (PCI_ICLK, PCI_I, PCI_O, PCI_IO)	3.3V PCI 2.1 Compatible.					
Leakage Current (ALL)						(Note 25-1)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Backdrive Protect/ChiProtect (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$ILEAK_{IH}$			10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V

HARDWARE MONITORING BLOCK (T_A = 0°C – +70°C, HVTR = +3.3 V ± 10%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 25-5
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±1		%/V	
Total Monitoring Cycle Time (Cycle Mode, Default Averaging)	$t_{C(Cycle)}$		1.25	1.4	sec	Note 25-6
Conversion Time (Continuous Mode, Default Averaging)	$t_{C(Cts)}$	225	247	275	msec	Note 25-7
Input Resistance			140	200	kΩ	
ADC Resolution						10 bits Note 25-10
Input Buffer (I) (FANTACH1)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
Input Buffer (I) (FANTACH2-FANTACH3)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
I_VID Type Buffer (GP62*, GP63*)						(Note 25-11)
Low Input Level	V_{ILI}			0.4	V	
High Input Level	V_{IHI}	0.8		5.5	V	
IOD Type Buffer (PWM1, PWM2, PWM3/ADDRESS ENABLE, nHWM_INT						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = +4.0 mA (Note 25-9)
Leakage Current (ALL - Digital)						(Note 25-8)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Digital Input Capacitance	C_{IN}			10	pF	

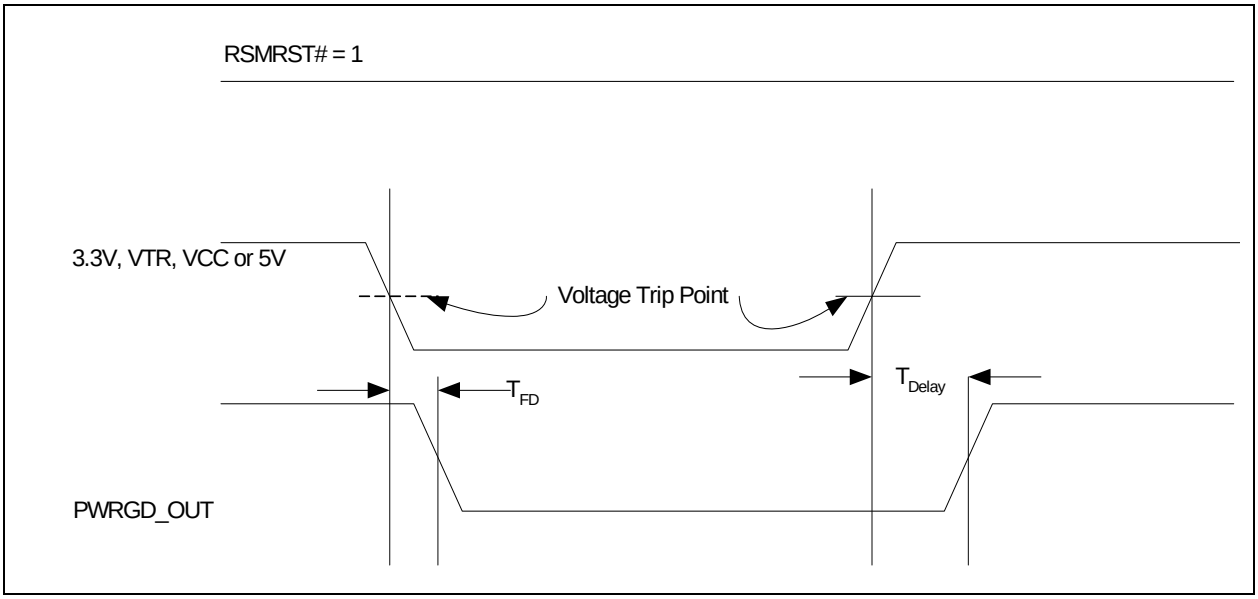
TABLE 26-1: RESUME RESET TIMING

Name	Description	MIN	TYP	MAX	Units	Notes
t1	tRESET_DELAY: VTR active to nRSMRST inactive	140	350	560	msec	
t2	tRESET_FALL: VTR inactive to nRSMRST active (Glitch width allowance)			100	nsec	
t3	tRESET_RISE			100	nsec	
V_{TRIP}	VTR low trip voltage	2.7	2.8	2.9	V	

APPLICATION NOTE: The 5 Volt Standby power supply must power up before or simultaneous with VTR, and must power down simultaneous with or after VTR (from ICH/PCH data sheet.) SCH3223 does not have a 5 Volt Standby power supply input and does not respond to incorrect 5 Volt Standby power - VTR sequencing.

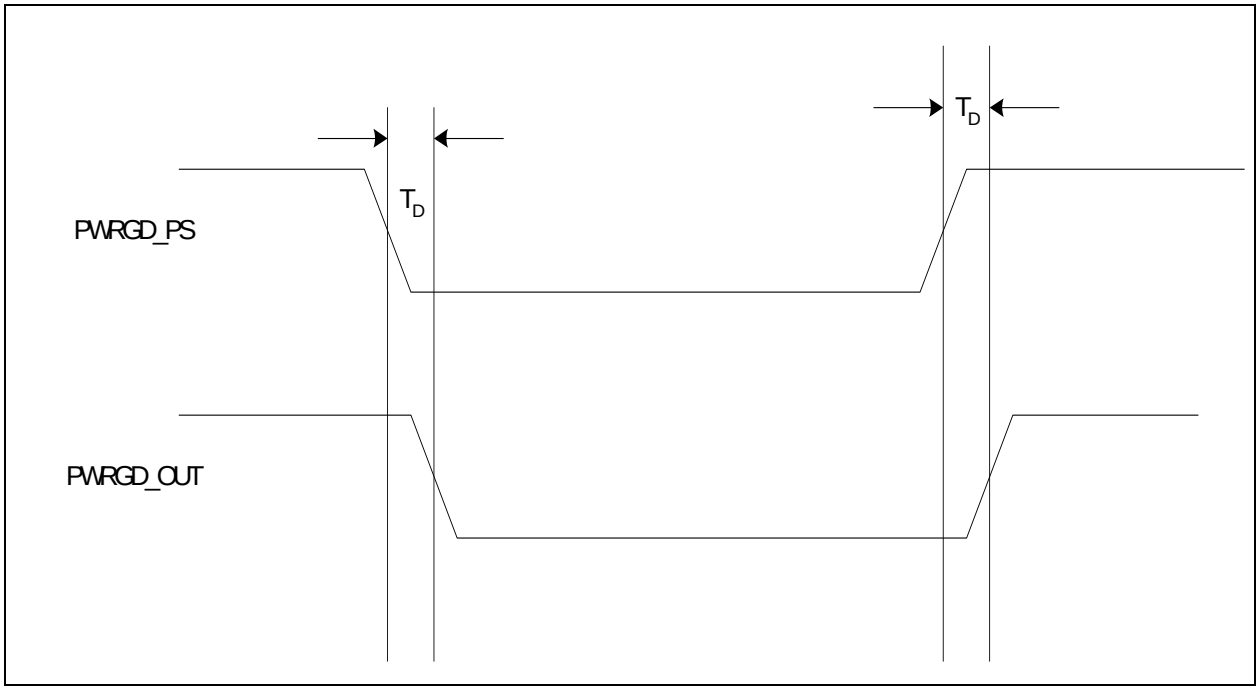
26.7 PWRGD_OUT Signal Generation

FIGURE 26-12: PWRGD_OUT TIMING VS. VOLTAGE 3.3V OR 5V DROP



Symbol	Time			Description
	MIN	TYP	MAX	
T_{Delay}	188ms	200ms	212ms	The delay time is from the rising voltage trip voltage to the rising edge of PWRGD_OUT. This delay is selected via a strapping option. Default value is 200ms.
	470ms	500ms	530ms	
T_{FD}	3ηs		20ηs	

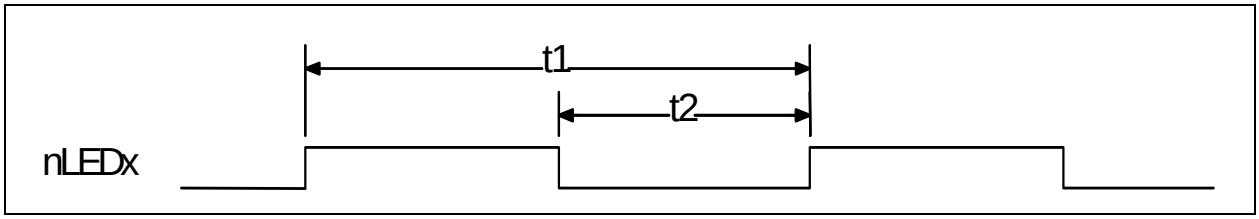
For 3.3V and 5V trip points refer to Table 25-3, “Reset Generators,” on page 177.



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	1ηs	10ηs	20ηs	Gate Delay

26.8 nLEDx Timing

FIGURE 26-14: NLEDX TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period		1 or 2(2)	5.88(1)	sec
t2	Blink ON Time	0	0.5(2)	1.52(1)	sec

Note 1: These Max values are due to internal Ring Oscillator. If 1Hz blink rate is selected for LED1 pin, the range will vary from 0.33Hz to 1.0Hz. If 0.5Hz blink rate is selected for LED1 pin, the range will vary from 0.17Hz to 0.5Hz.

2: The blink rate is programmed through Bits[1:0] in LEDx register. When Bits[1:0]=00, LED is OFF. Bits[1:0]=01 indicates LED blink at 1Hz rate with a 50% duty cycle (0.5 sec ON, 0.5 sec OFF). Bits[1:0]=10 indicates LED blink at ½ Hz rate with a 25% duty cycle (0.5 sec ON, 1.5 sec OFF). When Bits[1:0]=11, LED is ON.