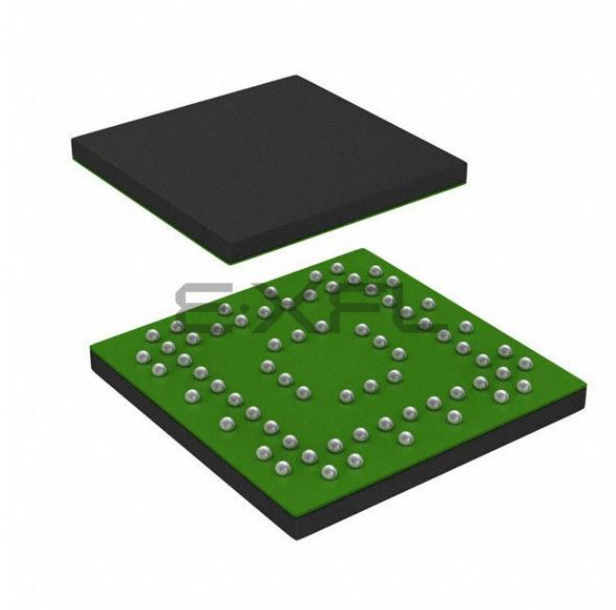

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The SYNC value of 0110 is intended to be used where the number of wait states is large. However, the SCH3223 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

6.3.2 RESET POLICY

The following rules govern the reset policy:

- When PCI_RESET# goes inactive (high), the PCI clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
- When PCI_RESET# goes active (low):

1. The host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
2. The SCH3223 ignores LFRAME#, tristates the LAD[3:0] pins and drives the LDRQ# signal inactive (high).

Table 7-8, summarizes the various IRQ sharing configurations. In this table, the following nomenclature is used:

- NS - port not shared
- S12 - uart 1 and uart 2 share an IRQ

TABLE 7-8: SCH3223 IRQ SHARING SUMMARY

Device	SP1 Mode REG (0xF0) Bit6 All Share Bit Table 22-9 on page 147	SP1 Mode REG (0xF0) Bit7 SP12 Share Bit Table 22-9 on page 147	SP1	SP2
SCH3223	0	0	NS	NS
	0	1	S12	S12
	1	0	NS	NS
	1	1	S12	S12

7.3 RS485 Auto Direction Control

The purpose of this function is to save the effort to deal with direction control in software. A direction control signal (usually nRTS) is used to tristate the transmitter when no other data is available, so that other nodes can use the shared lines. It is preferred to have this function on all six serial ports.

This will affect the nRTS and nDTR signals for each serial port in the device. Each serial port will have the following additional characteristics:

- An option register for the serial port in the runtime registers with following bits:
  - An enable bit to turn on/off the direction control
  - An enable bit to select which bit nRTS or nDTR, of the serial port is affected.
  - A bit to select the polarity - high or low, that the selected signal is driven to when the output buffer of the corresponding serial port is empty or full.
- When automatic direction control is enabled, the device monitors the local output buffer for not empty and empty conditions. If enabled, the direction control will force the nRTS or nDTR signal (selected via programming) to the desired polarity under the empty or not empty condition. Table 7-9 summarizes the possible programming states.
- Automatic Direction Control of the serial ports is only valid when the FIFO is enabled.
- The multi-function GPIO pins do not automatically set the direction when selected as serial port pins.
- The high speed baud rates will only work if the MSB of the MS divisor is set.

TABLE 7-9: NRTS/NDTR AUTOMATIC DIRECTION CONTROL OPTIONS

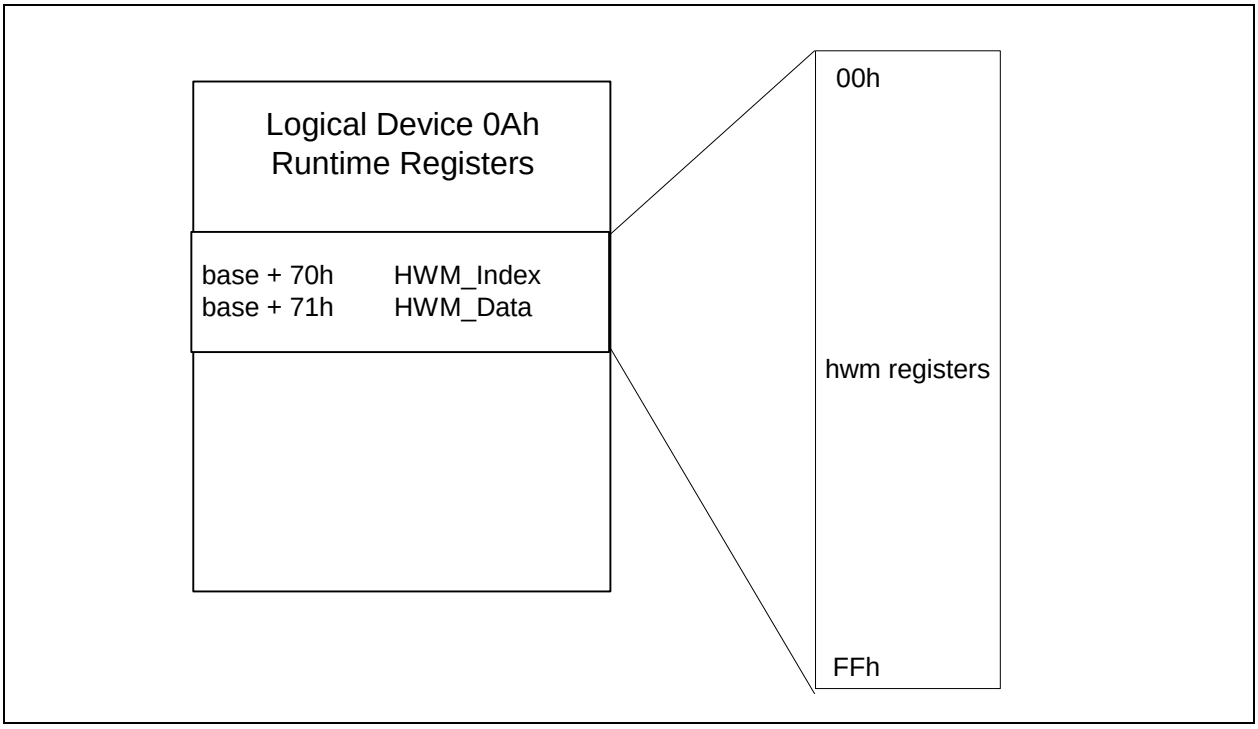
Local TX Buffer State	Flow Count EN Bit	NRTS/NDTR SEL BIT	Polarity SEL Bit	NRTS	NDTR
X	0	X	X	N/A	N/A
empty	1	1	0	0	N/A
empty	1	1	1	1	N/A
not empty	1	1	0	1	N/A
not empty	1	1	1	0	N/A
empty	1	0	0	N/A	0
empty	1	0	1	N/A	1
not empty	1	0	0	N/A	1
not empty	1	0	1	N/A	0

Note: Note that N/A indicates the signal is not affected under these conditions and maintains normal operation.

20.2 HWM Interface

The SCH3223 HWM block registers are accessed through an index and data register located at offset 70h and 71h, respectively, from the address programmed in the Base I/O Address in Logical Device A (also referred to as the Runtime Register set).

FIGURE 20-2: HWM REGISTER ACCESS



20.3 Power Supply

The HWM block is powered by standby power, HVTR, to retain the register settings during a main power (sleep) cycle. The HWM block does not operate when VCC=0 and HVTR is on. In this case, the H/W Monitoring logic will be held in reset and no monitoring or fan control will be provided. Following a VCC POR, the H/W monitoring logic will begin to operate based on programmed parameters and limits.

The fan tachometer input pins are protected against floating inputs and the PWM output pins are held low when VCC=0.

Note:	The PWM pins will be forced to “spinup” (if enabled) when PWRGD_PS goes active. See “PWM Fan Speed Control” on page 77.

20.4 Resetting the SCH3223 Hardware Monitor Block

20.4.1 VTR POWER-ON RESET

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when VTR power is applied to the block. The default state of the register is shown in the Register Summary Table located in Table 21-1 on page 100. The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note:	Usually the first action after power up is to write limits into the Limit Registers.

The nHWM_INT pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if enabled.

The nHWM_INT pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2 (Fan Tachs) register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The nHWM_INT pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the nHWM_INT pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to ‘1’ again.

The nHWM_INT pin may only become active while the monitor block is operational.

20.9.2 INTERRUPT AS A PME EVENT

The hardware monitoring interrupt signal is routed to the SIO PME block. For a description of these bits see the section defining PME events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 20-3: Interrupt Control on page 71.)

The THERM PME status bit is located in the PME_STS1 Runtime Register at offset 04h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM PME status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the PME_EN1 register at offset 08h.

20.9.3 INTERRUPT AS AN SMI EVENT

The hardware monitoring interrupt signal is routed to the SIO SMI block. For a description of these bits see the section defining SMI events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 20-3: Interrupt Control on page 71.)

The THERM SMI status bit is located in the SMI_STS5 Runtime Register at offset 14h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM SMI status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the SMI_EN5 register at offset 1Ah.

The SMI is enabled onto the SERIRQ (IRQ2) via bit 6 of the SMI_EN2 register at 17h.

20.9.4 INTERRUPT EVENT ON SERIAL IRQ

The hardware monitoring interrupt signal is routed to the Serial IRQ logic. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 20-3: Interrupt Control on page 71.)

This operation is configured via the Interrupt Select register (0x70) in Logical Device A. This register allows the selection of any serial IRQ frame to be used for the HWM nHWM_INT interrupt (SERIRQ9 slot will be used). See Interrupt Event on Serial IRQ on page 73.

20.10 Low Power Mode

bit The hardware monitor has two modes of operation: Monitoring and Sleep. When the START bit, located in Bit[0] of the Ready/Lock/Start register (0x40), is set to zero the hardware monitor is in Sleep Mode. When this bit is set to one the hardware monitor is fully functional and monitors the analog inputs to this device.
bit Sleep mode is a low power mode in which bias currents are on and the internal oscillator is on, but the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

Note 1: In Sleep Mode the PWM Pins are held high forcing the PWM pins to 100% duty cycle (256/256).

2: The START a bit cannot be modified when the LOCK bit is set.

duty cycle will be held constant for a minimum of 18 periods (206/11.4 = 18.07) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.

- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than 1/255. For example, if the PWM frequency is 11Hz (1/11Hz = 90.9msec) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., 90.9/5 = 18.18) until it reaches the calculated duty cycle. Note: The step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.

Note:	The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 105.8msec (default) (see Table 20-2, "ADC Conversion Sequence," on page 69). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits. The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every 1/(PWM frequency) seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle>00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

PWM Output Transition from ON to OFF

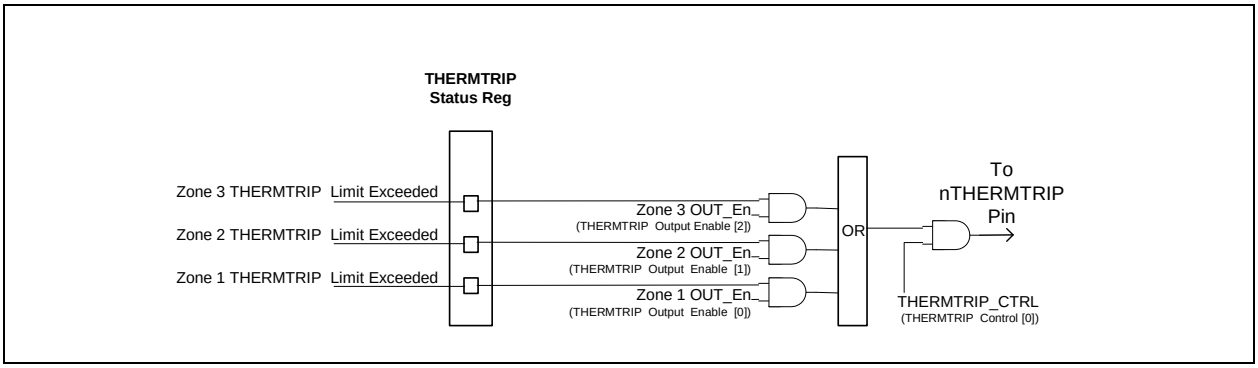
Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

TABLE 20-4: PWM RAMP RATE

RRx-[2:0]	PWM Ramp Time (SEC) (Time from 33% Duty Cycle to 100% Duty Cycle)	PWM Ramp Time (SEC) (Time from 0% Duty Cycle to 100% Duty Cycle)	Time per PWM Step (PWM Step Size = 1/255)	PWM Ramp Rate (Hz)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

The following figures summarize the THERMTRIP operation in relation to the THERMTRIP status bits.

FIGURE 20-15: NTHERMTRIP OUTPUT OPERATION



20.14.2 FAN SPEED MONITORING

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

The tachometers will operate in one of two modes:

- Mode 1: Standard tachometer reading mode. This mode is used when the fan is always powered when the duty cycle is greater than 00h.
- Mode 2: Enhanced tachometer reading mode. This mode is used when the PWM is pulsing the fan.

20.14.2.1 TACH Inputs

The tachometer inputs are implemented as digital input buffers with logic to filter out small glitches on the tach signal.

20.14.2.2 Selecting the Mode of Operation:

The mode is selected through the Mode Select bits located in the Tach Option register. This Mode Select bit is defined as follows:

- 0=Mode 1: Standard tachometer reading mode
- 1=Mode 2: Enhanced tachometer reading mode.

Default Mode of Operation:

- Mode 1
- Slow interrupt disabled (Don't force FFFEh)
- Tach interrupt enabled via enable bit
- Tach Limit = FFFFh
- Tach readings updated once a second

20.14.2.3 Mode 1 – Always Monitoring

Mode 1 is the simple case. In this mode, the Fan is always powered when it is ‘ON’ and the fan tachometer output ALWAYS has a valid output. This mode is typically used if a linear DC Voltage control circuit drives the fan. In this mode, the fan tachometer simply counts the number of 90kHz pulses between the programmed number of edges (default = 5 edges). The fan tachometer reading registers are continuously updated.

The counter is used to determine the period of the Fan Tachometer input pulse. The counter starts counting on the first edge and continues counting until it detects the last edge or until it reaches FFFFh. If the programmed number of edges is detected on or before the counter reaches FFFFh, the reading register is updated with that count value. If the counter reaches FFFFh and no edges were detected a stalled fan event has occurred and the Tach Reading register will be set to FFFFh. If one or more edges are detected, but less than the programmed number of edges, a slow fan event has

TABLE 21-3: TEMPERATURE VS. REGISTER READING (CONTINUED)

Temperature	Reading (DEC)	Reading (HEX)
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh
(SENSOR ERROR)		80h

21.2.4 REGISTERS 28-2DH: FAN TACHOMETER READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
28h	R	FANTACH1 LSB	7	6	5	4	3	2	1	0	FFh
29h	R	FANTACH1 MSB	15	14	13	12	11	10	9	8	FFh
2Ah	R	FANTACH2 LSB	7	6	5	4	3	2	1	0	FFh
2Bh	R	FANTACH2 MSB	15	14	13	12	11	10	9	8	FFh
2Ch	R	FANTACH3 LSB	7	6	5	4	3	2	1	0	FFh
2Dh	R	FANTACH3 MSB	15	14	13	12	11	10	9	8	FFh

This register is reset to its default value when PWRGD_PS is asserted.

The Fan Tachometer Reading registers contain the number of 11.111µs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

21.2.5 REGISTERS 30-32H: CURRENT PWM DUTY

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
30h	R/W (Note 21-14)	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
31h	R/W (Note 21-14)	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
32h	R/W (Note 21-14)	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A

Note 21-14 These registers are only writable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at high speeds (100% duty cycle), so care should be taken in software to ensure that the limit is low enough not to cause sporadic alerts. Note that an interrupt status event will be generated when the tachometer reading is greater than the minimum tachometer limit.

The fan tachometer will not cause a bit to be set in the interrupt status register if the current value in the associated Current PWM Duty registers is 00h or if the PWM is disabled via the PWM Configuration Register.

Interrupts will never be generated for a fan if its tachometer minimum is set to FFFFh.

21.2.15 REGISTERS 5C-5EH: PWM CONFIGURATION

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Ch	R/W	PWM 1 Configuration	ZON2	ZON1	ZON0	INV	SUEN1	SPIN2	SPIN1	SPIN0	62h
5Dh	R/W	PWM 2 Configuration	ZON2	ZON1	ZON0	INV	SUEN2	SPIN2	SPIN1	SPIN0	62h
5Eh	R/W	PWM 3 Configuration	ZON2	ZON1	ZON0	INV	SUEN3	SPIN2	SPIN1	SPIN0	62h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits [7:5] Zone/Mode

Bits [7:5] of the PWM Configuration registers associate each PWM with a temperature zone.

- When in Auto Fan Mode, the PWM will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If 'Hottest' option is selected (101 or 110), the PWM will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. If one of these options is selected, the PWM is controlled by the limits and parameters for the zone that requires the highest PWM duty cycle, as computed by the auto fan algorithm.
- When in manual control mode, the PWMx Current Duty Cycle Registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. See PWMx Current Duty Cycle Registers description.
- When the fan is disabled (100) the corresponding PWM output is driven low (or high, if inverted).
- When the fan is Full On (011) the corresponding PWM output is driven high (or low, if inverted).

Note 1: Zone 1 is controlled by Remote Diode 1 Temp Reading register

2: Zone 2 is controlled by the Ambient Reading Register.

3: Zone 3 is controlled by Remote Diode 2 Temp Reading register

TABLE 21-7: FAN ZONE SETTING

ZON[7:5]	PWM Configuration
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2,3
110	Fan controlled by hottest of zones 1,2,3
111	Fan manually controlled

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 1, 100% duty cycle will yield an output that is low for 255 clocks and high for 1 clock. If set to 0, 100% duty cycle will yield an output that is high for 255 clocks and low for 1 clock.

Bit [3] Forced Spin-up Enable

Bit [3] enables the forced spin up option for a particular PWM. If set to 1, the forced spin-up feature is enabled for the associated PWM. If set to 0, the forced spin-up feature is disabled for the associated PWM.

APPLICATION NOTE: This bit should always be enabled (set) to prevent fan tachometer interrupts during spinup.

21.2.16.2 Range Selection (Default =1100=32°C)

TABLE 21-10: REGISTER SETTING VS. TEMPERATURE RANGE

RAN[3:0]	Range (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32
1101	40
1110	53.33
1111	80

Note: The range numbers will be used to calculate the slope of the PWM ramp up. For the fractional entries, the PWM will go on full when the temp reaches the next integer value e.g., for 3.33, PWM will be full on at (min. temp + 4).

21.2.17 REGISTER 62H, 63H: PWM RAMP RATE CONTROL

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
62h	R/W	PWM 1 Ramp Rate Control	RES1	RES1	RES1	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h
63h	R/W	PWM 2, PWM 3 Ramp Rate Control	RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

RES1 bits are set to ‘1’ and are read only, writes are ignored.

Description of Ramp Rate Control bits:

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the part. The auto fan control logic calculates the PWM duty cycle for all temperature readings. If Ramp Rate Control is disabled, the PWM output will jump or oscillate between different PWM duty cycles causing the fan to suddenly change speeds, which creates unwanted fan noise. If enabled, the PWM Ramp Rate Control logic will prevent the PWM output from jumping, instead the PWM will ramp up/down towards the new duty cycle at a pre-determined ramp rate.

Ramp Rate Control

The Ramp Rate Control logic limits the amount of change to the PWM duty cycle over a period of time. This period of time is programmable via the Ramp Rate Control bits. For a detailed description of the Ramp Rate Control bits see Table 21-11.

Note 1: RR1E, RR2E, and RR3E enable PWM Ramp Rate Control for PWM 1, 2, and 3 respectively.

2: RR1-2, RR1-1, and RR1-0 control ramp rate time for PWM 1

21.2.34 REGISTERS 8AH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

21.2.35 REGISTERS 8BH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Bh	R/W	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

21.2.36 REGISTERS 8CH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ch	R	MCHP Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

21.2.37 REGISTERS 8DH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Dh	R/W	MCHP Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

21.2.38 REGISTERS 8EH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Eh	R	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an MCHP Test register.

21.2.39 REGISTERS 90H-92H: FANTACHX OPTION REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
90h	R/W	FANTACH1 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
91h	R/W	FANTACH2 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
92h	R/W	FANTACH3 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bit[0] SLOW

0= Force tach reading register to FFFFh if number of tach edges detected is greater than 0, but less than programmed number of edges. (default)

21.2.62 REGISTER C0H: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C0h	R/W	MCHP Reserved	RES	RES	RES	RES	RES	RES	RES	RES	00h

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

21.2.63 REGISTER C1H: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C1h	R/W	Thermtrip Control	RES	RES	RES	RES	RES	RES	THERM-TRIP_C-TRL	RES	01h

THERMTRIP_CTRL: Bit 1 in the Thermtrip Control register. May be enabled to assert the Thermtrip# pin if programmed limits are exceeded as indicated by the Thermtrip Status register 1=enable, 0=disable (default).

21.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

21.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h

Note:

- Each bit in this register is cleared on a write of 1 if the event is not active.
- This register is reset to its default value when the PWRGD_PS signal transitions high.

TABLE 22-4: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS (CONTINUED)

Register	Address	Description
Configuration Address Byte 1 Default Sysopt1 = 0 0x16 Sysopt1 = 1 0x00 n VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] Bits[15:21] = 0 (Note 22-3)
Default = 0x00 on VCC POR, SOFT RESET and PCI RESET	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.

Note 22-3 To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note:	The default configuration address is specified in Table 22-1, “SYSOPT Strap Option Configuration Address Select,” on page 137.

22.1.2 TEST REGISTERS

The following test registers are used in the SCH3223 devices.

TABLE 22-5: TEST REGISTER SUMMARY

TEST 8 Default = 0x00, on VCC POR and VTR POR	0x19 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 9 Default = 0x00, on VCC POR and VTR POR	0x25 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST Default = 0x00 Note on VTR_POR BIT0/7 are reset BIT1-6 reset on TST_PORB from resgen block	0x29 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 4 Default = 0x00, on VCC POR and VTR POR	0x2B R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 5 Default = 0x00, on VCC POR and VTR POR	0x2C R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_EN1 Default = 0x00 on VTR POR	08 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_EN bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PME_EN3 Default = 0x00 on VTR POR	09 (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_EN bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] WDT Bit[1] Reserved Bit[2] Reserved Bit[3] DEVINT_EN (Enable bit for group SMI signal for PME) Bit[4] GP27 Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PME_EN5 Default = 0x00 on VTR POR	0A (R/W)	PME Wake Enable Register 5 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_EN bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SMI_STS1 Default = 0x02, or 0x03 on VTR POR. The default will be 0x03 if there is a LOW_BAT event under VBAT power only, or 0x02 if this event does not occur. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] Reserved Bit[2] U2INT Bit[3] U1INT Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	Bit[7:0] Reserved
SMI_STS3 Default = 0x00 on VTR POR	16 (R/WC)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] Reserved Bit[2] Reserved Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_STS4 Default = 0x00 on VTR POR (Note 23-14)	17 (R/WC)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] Reserved Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] GP42 Bit[6] Reserved Bit[7] GP61
SMI_EN1 Default = 0x00 on VTR POR	18 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nIO_SMI output. 1=Enable 0=Disable Bit[0] EN_LOW_BAT Bit[1] Reserved Bit[2] EN_U2INT Bit[3] EN_U1INT Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] EN_WDT

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
Reserved Default = 0x03 on VCC POR, PCI Reset and VTR POR	1E (R/W)	Bit[7:0] Reserved
Reserved	1F (R)	Bit[7:0] Reserved
UART1 FIFO Control Shadow	20 (R)	UART FIFO Control Shadow 1 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select (unused) Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
UART2 FIFO Control Shadow	21 (R)	UART FIFO Control Shadow 2 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select (unused) Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
Reserved	22 (R)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	23 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	24 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	25 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	26 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	27 (R/W)	Bits[7:0] Reserved
Reserved	28 (R)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	29 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	2A (R/W)	Bits[7:0] Reserved

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

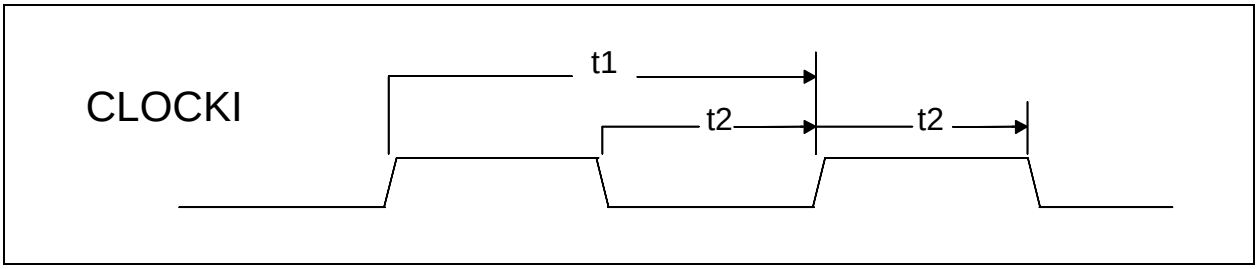
Name	REG Offset (HEX)	Description
Reserved Default = 0x01 on VTR POR	37 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	39 (R/W)	Bits[7:0] Reserved
Reserved Default = 0x01 on VTR POR	3A (R/W)	Bits[7:0] Reserved
Reserved Default =0x01 on VTR POR	3B (R/W)	Bits[7:0] Reserved
CLOCK Output Control Register VTR POR = 0x00	3C (R/W)	Bit[0] Enable 1= Output Enabled 0= Disable Clock output Bit[3:1] Frequency Select 000= 0.25 Hz 001= 0.50 Hz 010= 1.00 Hz 011= 2.00 Hz 100= 4.00 Hz 101= 8.00 Hz 110= 16 hz 111 = reserved Bit[7:4] Reserved
GP42 Default =0x01 on VTR POR	3D (R/W)	General Purpose I/O bit 4.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME Note: configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP50 Default = 0x01 on VTR POR	3F (R/W)	General Purpose I/O bit 5.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRI2 (Note 23-11) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP51 Default = 0x01 on VTR POR	40 (R/W)	General Purpose I/O bit 5.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDCD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP60 Default = 0x01 on VTR POR	47 (R/W)	General Purpose I/O bit 6.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=WDT 10=Either Edge Triggered Interrupt Input 4 (Note 23-12) 01=LED1 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP61 Default = 0x01 on VTR POR	48 (R/W)	General Purpose I/O bit 6.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=CLKO - Programmable clock output as described in 10=Either Edge Triggered Interrupt Input 5 (Note 23-12) 01=LED2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

26.2 Input Clock Timing

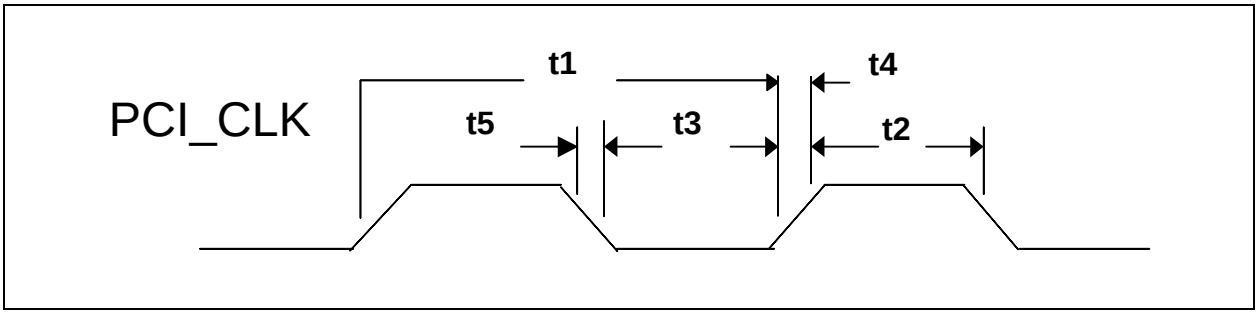
FIGURE 26-2: INPUT CLOCK TIMING



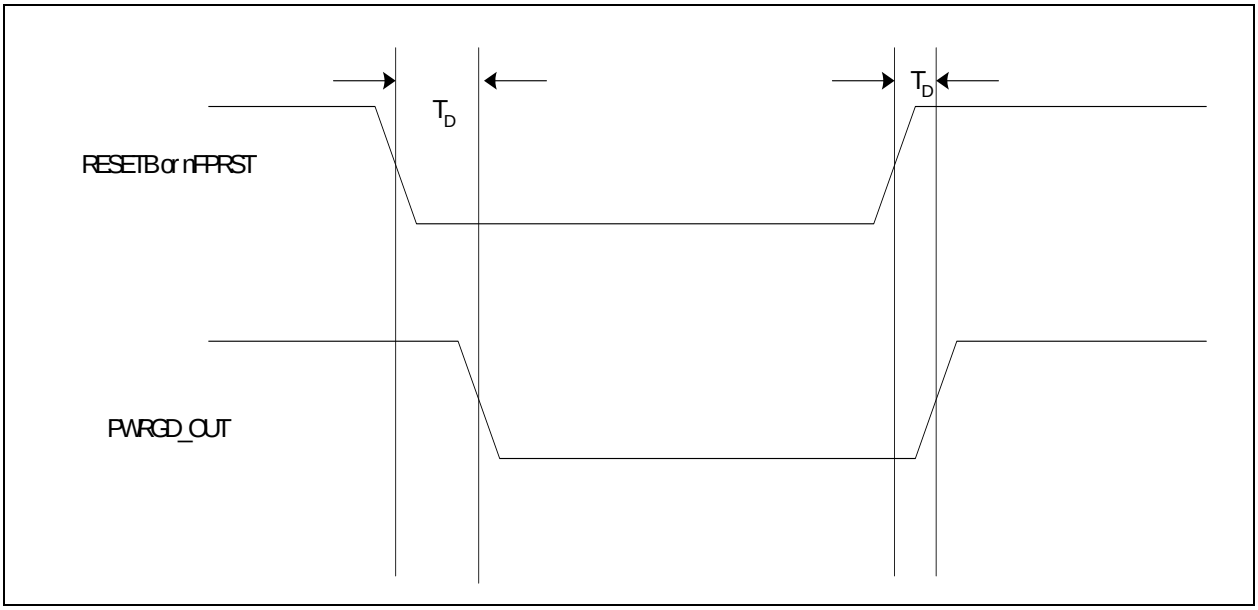
Name	Description	MIN	TYP	MAX	Units
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

26.3 LPC Interface Timing

FIGURE 26-3: PCI CLOCK TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	0	1.6ms	2.0ms	Debounce Delay

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	XX	-	[XX]
Device	Temperature Range		Package		Tape and Reel Option

Device:	SCH3223	
Temperature Range:	Blank =	0°C to +70°C (Commercial)
	I =	-40°C to +85°C (Industrial)
Package:	7U =	64-pin WFBGA
Tape and Reel Option:	Blank =	Standard packaging (tray)
	TR =	Tape and Reel (Note 1)

Examples:

a) SCH3223-7U
Commercial temperature, 64-pin WFBGA, Tray

b) SCH3223I-7U-TR
Industrial temperature, 64-pin WFBGA, Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.