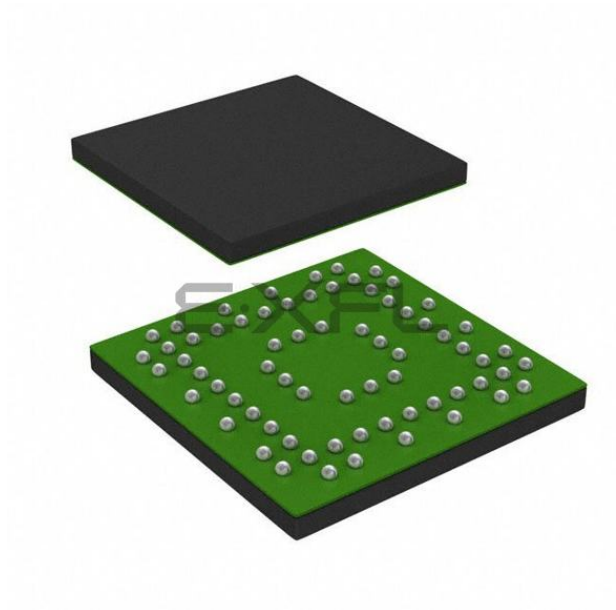

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RAM Size	-
Interface	LPC, Serial, UART
Number of I/O	19
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFBGA
Supplier Device Package	64-WFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3223i-7u-tr

2.1 SCH3223 Pin Layout Summary

TABLE 2-1: SCH3223 SUMMARY

Ball#	Function (Note 1)
B1	+12V_IN
C1	+5V_IN
C2	VTR
D2	TEST=VSS
E2	VSS
E1	CLOCKI
E4	LAD0
F4	LAD1
G4	LAD2
G2	LAD3
G1	LFRAME#
H6	PCI_RESET#
H5	PCI_CLK
H2	SER_IRQ
J2	VSS
K3	VCC
J1	nIDE_RSTDRV / GP44
K2	nPCIRST1 / GP45
K1	nPCIRST2 / GP46
L2	nPCIRST3 / GP47
L3	AVSS
K4	VBAT
K5	GP27 / nIO_SMI
L5	VTR
L9	nRI1
L10	nDCD1
K11	RXD1
K7	TXD1
K8	nDSR1
K9	nRTS1 / SYSOPT0
K10	nCTS1
J10	nDTR1 / SYSOPT1
J11	GP50 / nRI2
H10	VTR
L7	VSS
H7	GP51 / nDCD2
G11	GP52 / RXD2
G10	GP53 / TXD2
G8	GP54 / nDSR2
F8	GP55 / nRTS2 / RESGEN
E8	GP56 / nCTS2
D6	GP57 / nDTR2
D7	PB_OUT#

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7.1.5 INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 7-2 on page 22). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic “0”, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic “1”, no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table (Table 7-2).

Bit 3

In non-FIFO mode, this bit is a logic “0”. In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic “0”.

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

TABLE 7-2: INTERRUPT CONTROL

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.

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Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic “1”, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic “1” and bit 4 is a logic “0”, an odd number of logic “1”’s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic “1” and bit 4 is a logic “1” an even number of bits is transmitted and checked.

Bit 5

This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic “1”, the transmit data output (TXD) is forced to the Spacing or logic “0” state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic “1”) to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic “0”) to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

7.1.7 MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic “1”, the nDTR output is forced to a logic “0”. When bit 0 is a logic “0”, the nDTR output is forced to a logic “1”.

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic “1”, the following occur:

1. The TXD is set to the Marking State (logic “1”).
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

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Table 7-8, summarizes the various IRQ sharing configurations. In this table, the following nomenclature is used:

- NS - port not shared
- S12 - uart 1 and uart 2 share an IRQ

TABLE 7-8: SCH3223 IRQ SHARING SUMMARY

Device	SP1 Mode REG (0xF0) Bit6 All Share Bit Table 22-9 on page 147	SP1 Mode REG (0xF0) Bit7 SP12 Share Bit Table 22-9 on page 147	SP1	SP2
SCH3223	0	0	NS	NS
	0	1	S12	S12
	1	0	NS	NS
	1	1	S12	S12

7.3 RS485 Auto Direction Control

The purpose of this function is to save the effort to deal with direction control in software. A direction control signal (usually nRTS) is used to tristate the transmitter when no other data is available, so that other nodes can use the shared lines. It is preferred to have this function on all six serial ports.

This will affect the nRTS and nDTR signals for each serial port in the device. Each serial port will have the following additional characteristics:

- An option register for the serial port in the runtime registers with following bits:
  - An enable bit to turn on/off the direction control
  - An enable bit to select which bit nRTS or nDTR, of the serial port is affected.
  - A bit to select the polarity - high or low, that the selected signal is driven to when the output buffer of the corresponding serial port is empty or full.
- When automatic direction control is enabled, the device monitors the local output buffer for not empty and empty conditions. If enabled, the direction control will force the nRTS or nDTR signal (selected via programming) to the desired polarity under the empty or not empty condition. Table 7-9 summarizes the possible programming states.
- Automatic Direction Control of the serial ports is only valid when the FIFO is enabled.
- The multi-function GPIO pins do not automatically set the direction when selected as serial port pins.
- The high speed baud rates will only work if the MSB of the MS divisor is set.

TABLE 7-9: NRTS/NDTR AUTOMATIC DIRECTION CONTROL OPTIONS

Local TX Buffer State	Flow Count EN Bit	NRTS/NDTR SEL BIT	Polarity SEL Bit	NRTS	NDTR
X	0	X	X	N/A	N/A
empty	1	1	0	0	N/A
empty	1	1	1	1	N/A
not empty	1	1	0	1	N/A
not empty	1	1	1	0	N/A
empty	1	0	0	N/A	0
empty	1	0	1	N/A	1
not empty	1	0	0	N/A	1
not empty	1	0	1	N/A	0

Note: Note that N/A indicates the signal is not affected under these conditions and maintains normal operation.

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10.0 GENERAL PURPOSE I/O (GPIO)

The SCH3223 provides a set of flexible Input/Output control functions to the system designer through the 19 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

10.1 GPIO Pins

The following pins include GPIO functionality. These pins are defined in the table below. All GPIOs default to the GPIO function except on indicated by Note 10-3.

TABLE 10-1: GPIO PIN FUNCTIONALITY

GPIO Pin				
Pin Name (Default Func/ Alternate Funcs)	**GPIO PWRWELL**	**VTR POR**	**SMI/PME**	**Note**
GP27/nIO_SMI	VCC	0x01	nIO_SMI/PME	10-1
nFPRST / GP30	VTR	0x05		10-3
GP42/nIO_PME	VTR	0x01	SMI	
nIDE_RSTDRV / GP44 GP44 / TXD6	VTR	0x01		10-3
nPCI_RST1 / GP45 GP45 / RXD6	VTR	0x01		10-3
nPCI_RST2 / GP46 GP46 / nSCIN6	VTR	0x01	PME	10-3, 10-4
nPCI_RST3 / GP47 GP47 / nSCOUT6	VTR	0x01		10-3
GP50/nRI2	VCC	0x01	PME	10-1
GP51/nDCD2	VCC	0x01	PME	10-1
GP52/RXD2	VCC	0x01	PME	10-1
GP53/TXD2	VCC	0x01	PME	10-1
GP54/nDSR2	VCC	0x01	SMI/PME	10-1
GP55/nRTS2	VCC	0x01	SMI/PME	10-1
GP56/nCTS2	VCC	0x01	SMI/PME	10-1
GP57/nDTR2	VCC	0x01	SMI/PME	10-1
GP60/nLED1/WDT	VTR	0x01	SMI/PME	10-1
GP61/nLED2/ CLKO	VTR	0x01	SMI/PME	10-1
GP62	VTR	0x01		10-3
GP63	VTR	0x01		10-3

Note 10-1 These pins are inputs to VCC and VTR powered logic.. The logic for the GPIO is on VCC - it is also a wake event which goes to VTR powered logic.

Note 10-2 This pin's primary function (power up default function) is not GPIO function; however, the pin can be configured a GPIO Alternate function.

Note 10-3 Not all alternate functions are available in the SCH3223 device. Refer to Table 10-2, "SCH3223 General Purpose I/O Port Assignments," on page 41 for more details.

Note 10-4 The PME is for the RI signal only. Refer to Table 10-2, "SCH3223 General Purpose I/O Port Assignments," on page 41 for more details.

Note 10-5 This pin is an OD type buffer in output mode. It cannot be configured as a Push-Pull Output buffer

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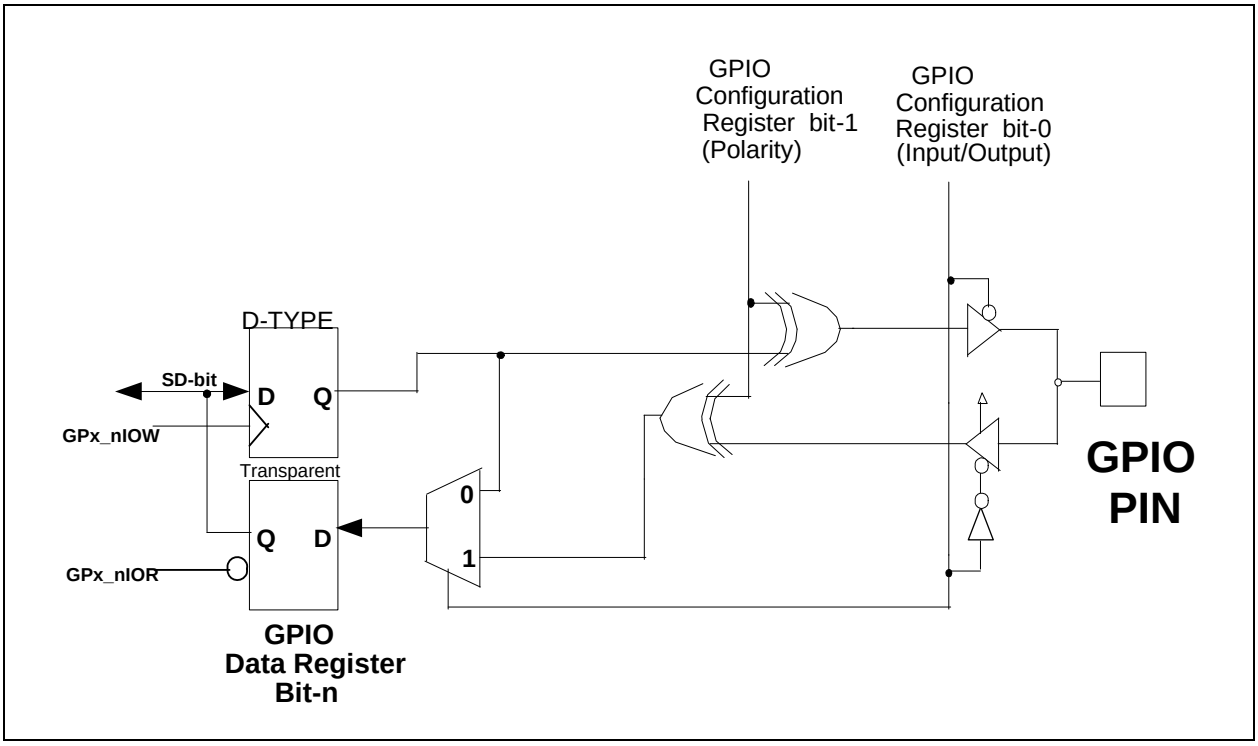
FIGURE 10-1: GPIO FUNCTION ILLUSTRATION



Note: Figure 10-1 is for illustration purposes only and is not intended to suggest specific implementation details.

TABLE 10-4: GPIO READ/WRITE BEHAVIOR

Host Operation	GPIO Input Port	GPIO Output Port
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

10.5 GPIO PME and SMI Functionality

The SCH3223 provides GPIOs that can directly generate a PME. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in a PME Status. For additional description of PME behavior see Section 12.0, "PME Support," on page 46. The default is the low-to-high transition. In addition, the SCH3223 provides GPIOs that can directly generate an SMI.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP27 is controlled by PME_STS3, PME_EN3 registers.

GP50-GP57 are controlled by PME_STS5, PME_EN5 registers.

GP60, GP61 are controlled by PME_STS6, and PME_EN6 registers.

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP54, GP55, GP56, GP57, GP60 are controlled by SMI_STS3, and SMI_EN3 registers.

GP42, GP61 are controlled by SMI_STS4, and SMI_EN4 registers.

The following GPIOs have "either edge triggered interrupt" (EETI) input capability: GP60, GP61. These GPIOs can generate a PME and an SMI on both a high-to-low and a low-to-high edge on the GPIO pin. These GPIOs have a status bit in the PME_STS6 status register that is set on both edges. The corresponding bits in the PME and SMI status registers are also set on both edges.

10.6 Either Edge Triggered Interrupts

Three GPIO pins are implemented such that they allow an interrupt (PME or SMI) to be generated on both a high-to-low and a low-to-high edge transition, instead of one or the other as selected by the polarity bit.

The either edge triggered interrupts (EETI) function as follows: If the EETI function is selected for the GPIO pin, then the bits that control input/output, polarity and open drain/push-pull have no effect on the function of the pin. However, the polarity bit does affect the value of the GP bit.

A PME or SMI interrupt occurs if the PME or SMI enable bit is set for the corresponding GPIO and the EETI function is selected on the GPIO. The PME or SMI status bits are set when the EETI pin transitions (on either edge) and are cleared on a write of '1'. There are also status bits for the EETIs located in the PME_STSX register, which are also cleared on a write of '1'. The MSC_STS register provides the status of all of the EETI interrupts within one register. The PME, SMI or MSC status is valid whether or not the interrupt is enabled and whether or not the EETI function is selected for the pin.

Miscellaneous Status Register (MSC_STS) is for the either edge triggered interrupt status bits. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding MSC status bits. Status bits are cleared on a write of '1'. See Section 23.0, "Runtime Registers," on page 150 for more information.

The configuration register for the either edge triggered interrupt status bits is defined in Section 23.0.

10.7 LED Functionality

The SCH3223 provides LED functionality on two GPIOs, GP60 and GP61. These pins can be configured to turn the LED on and off and blink independent of each other through the LED1 and LED2 runtime registers at offset 0x5D and 0x5E from the base address located in the primary base I/O address in Logical Device A.

The LED pins (GP60 and GP61) are able to control the LED while the part is under VTR power with VCC removed. In order to control a LED while the part is under VTR power, the GPIO pin must be configured for the LED function and either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type, the part will source current. The part is also able to blink the LED under VTR power. The LED will not blink under VTR power (VCC removed) if the external 32KHz clock is not connected.

The LED pins can drive a LED when the buffer type is configured to be push-pull and the part is powered by either VCC or VTR, since the buffers for these pins are powered by VTR. This means they will source their specified current from VTR even when VCC is present.

The LED control registers are defined in Section 23.0.

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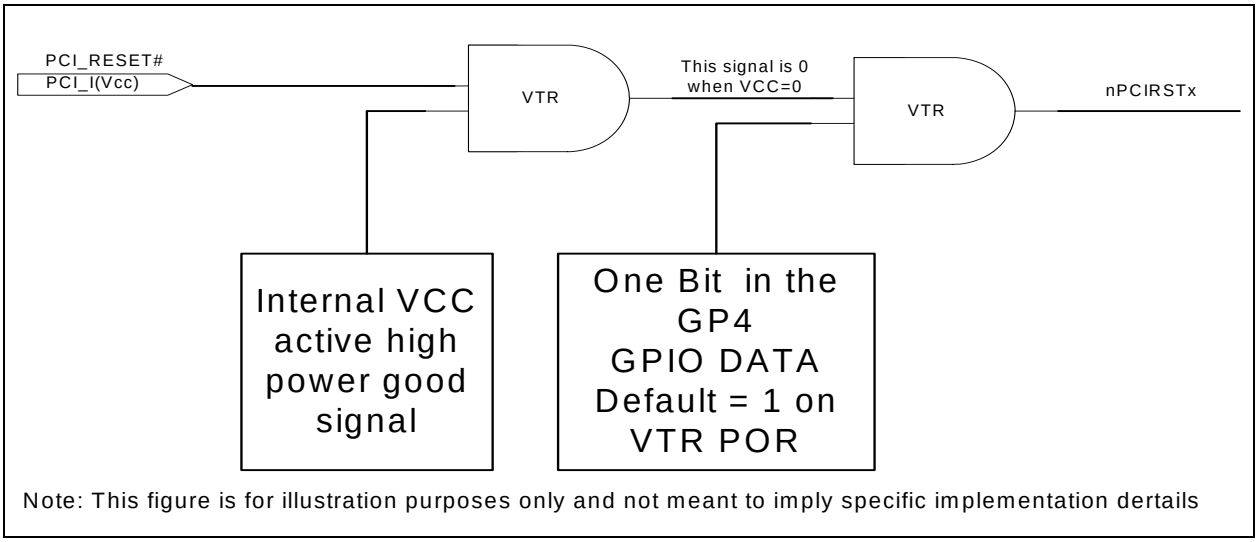
When the VTR power is applied, VCC is powered down, and the GPIO control register's contents are default, the nPCIRSTx pin output is low.

The Figure 16-1 illustrates the nPCIRSTx function. The figure is for illustration purposes only and in not intended to suggest specific implementation details.

FIGURE 16-1: NPCIRSTX LOGIC



Note: This figure is for illustration purposes only and not meant to imply specific implementation dertails

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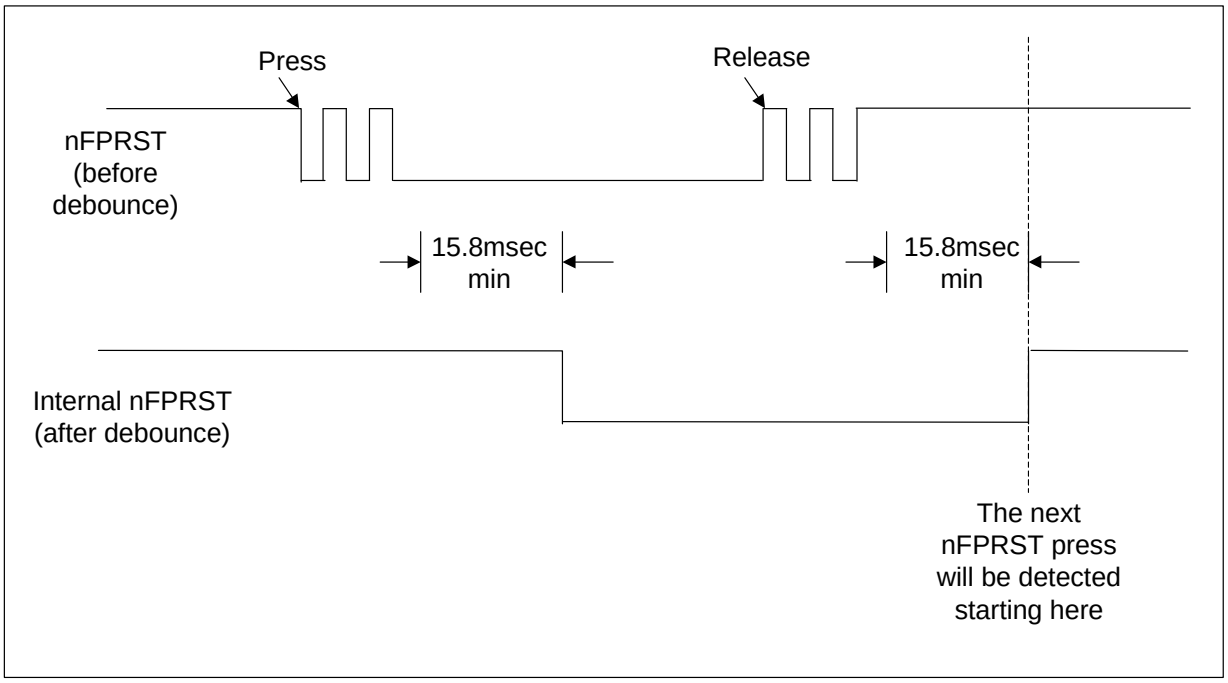
FIGURE 17-2: NFPRST DEBOUNCE TIMING



17.3 A/C Power Failure Recovery Control

The Power Failure Recovery Control logic, which is powered by VTR, is used to return a system to a pre-defined state after a power failure (VTR=0V). The Power Control Register, which is powered by Vbat, contains two bits defined as APF (After Power Failure). These bits are used to determine if the power supply should be powered on, powered off, or set to the previous power state before VTR was removed as shown in Table 17-3.

Power Failure Recovery registers that are required to retain their state through a power failure are powered by Vbat.

Two modes may be used to determine the previous state:

Mode 1: (Suggested if PWR_OK is selected& enabled), which is enabled when Bit[3] PS_ON# sampling is disabled, latches the current value of the PS_ON# pin when VCC, VTR, or PWR_OK (if enabled) transition to the inactive state, whichever comes first. This value is latched into Bit[4] Previous State Bit located in the Power Recovery Register located at offset 49h and is used to determine the state of the PS_ON# pin when VTR becomes active.

Mode 2 is enabled when Bit[3] PS_ON# sampling is enabled. To determine the previous power state, the PS_ON# pin is sampled every 0.5 seconds while VTR is greater than ~2.2Volts. This sample is inserted into a battery powered 8-bit shift register. The hardware will select a bit from the shift register depending on the value of the PS_ON# Previous State Select bits located in the Runtime Register block at offset 53h to determine the state of the PS_ON# pin when VTR becomes active. The value in the 8-bit shift register is latched into the PS_ON Register at offset 4Ah in the Runtime Register block after VTR power is returned to the system, but before the internal shift register is cleared and activated. The PS_ON Register is a battery powered register that is only reset on a Vbat POR.

Note 1: In Mode 2, when VTR falls below ~2.2Volts the current value of the PS_ON# pin will be latched into Bit [4] Previous State Bit located in the Power Recovery Register at offset 49h. This bit will not be used by hardware, but may be read by software to determine the state of the PS_ON# pin when the power failure occurred.

2: The time selected for the PS_ON# Previous State bits should be greater than or equal to the time it takes for Resume Reset to go inactive to the time VTR is less than ~2.2 Volts.

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When in Auto Fan Control Operating Mode the hardware controls the fans directly based on monitoring of temperature and speed.

To control the fans:

1. Set the minimum temperature that will turn the fans on. This value is programmed in Registers 67h-69h: Zone x Low Temp Limit (Auto Fan Mode Only).

The speed of the fan is controlled by the duty cycle set for that device. The duty cycle for the minimum fan speed must be programmed in Registers 64h-66h: PWMx Minimum Duty Cycle. This value corresponds to the speed of the fan when the temperature reading is equal to the minimum temperature LIMIT setting. As the actual temperature increases and is above the Zone LIMIT temperature and below the Absolute Temperature Limit, the PWM will be determined by a linear function based on the Auto Fan Speed Range bits in Registers 5Fh-61h.

The maximum speed of the fan for the linear autofan function is programmed in the PWMx Max registers (0D1h, 0D6h, 0DBh). When the temperature reaches the top of the linear fan function for the sensor (Zone x Low Temp Limit plus Temperature Range) the fan will be at the PWM maximum duty cycle.

Set the absolute temperature for each zone in Registers 6Ah-6Ch: Zone x Temp Absolute Limit (Auto Fan Mode only). If the actual temperature is equal to or exceeds the absolute temperature in one or more of the associated zones, all Fans operating in auto mode will be set to Full on, regardless of which zone they are operating in (except those that are disabled or configured for Manual Mode). Note: fans can be disabled via the PWMx Configuration registers and the absolute temperature safety feature can be disabled by writing 80h into the Zone x Temp Absolute Limit registers.

To set the mode to operate in auto mode, set Bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWM Configuration Bits[7:5]=’000’ for PWM on Zone 1; Bits[7:5]=’001’ for PWM on Zone 2; Bits[7:5]=’010’ for PWM on Zone 3. If the “Hottest” option is chosen (101 or 110), then the PWM output is controlled by the zone that results in the highest PWM duty cycle value.

Note 1: Software can be alerted of an out-of-limit condition by the nHWM_INT pin if an event status bit is set and the event is enabled and the interrupt function is enabled onto the nHWM_INT pin.

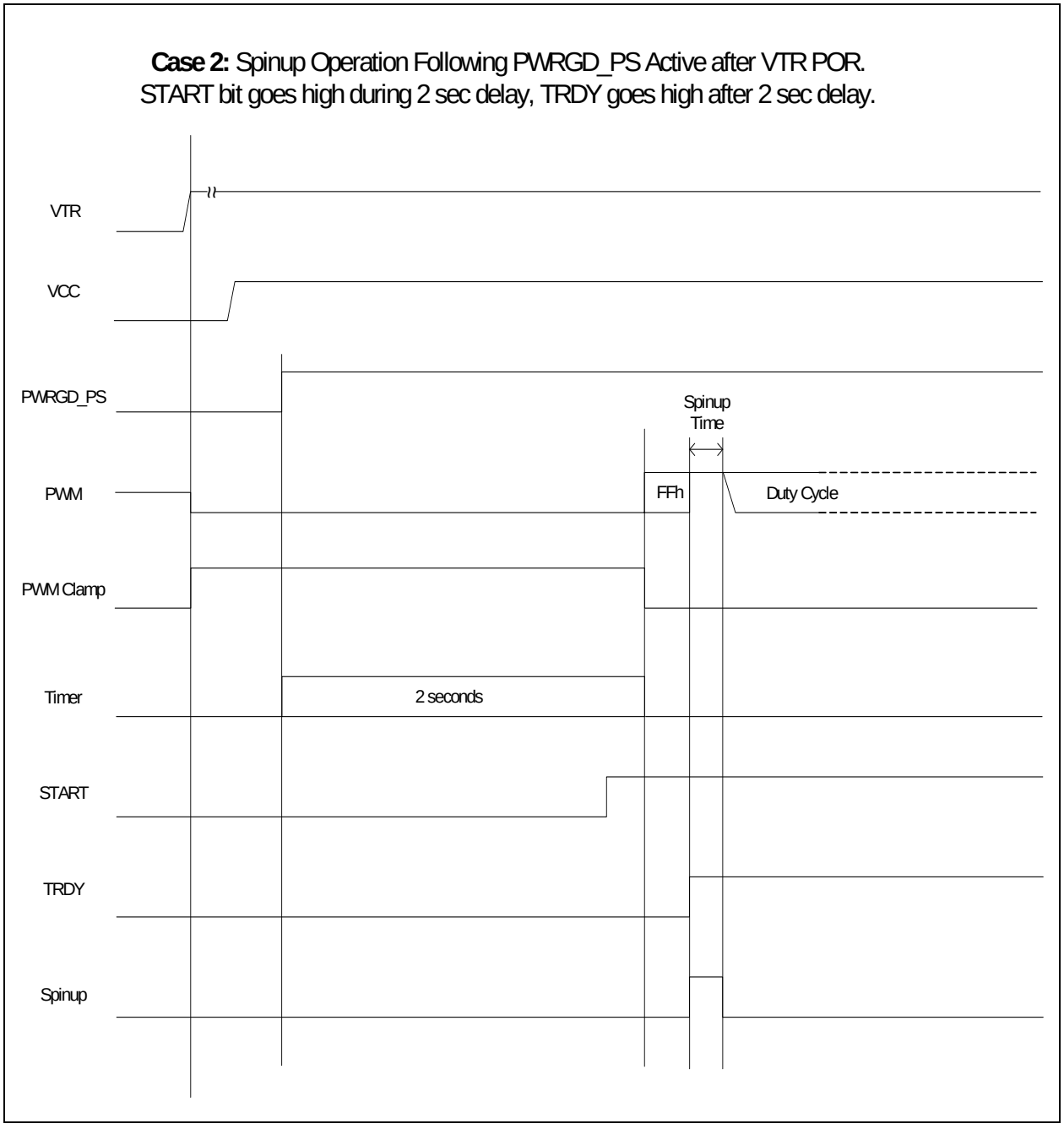
2: Software can monitor the operation of the Fans through the Fan Tachometer Reading registers and by the PWM x Current PWM duty registers. It can also monitor current temperature readings through the Temperature Limit Registers if hardware monitoring is enabled.

3: Fan control in auto mode is implemented without any input from external processor .

In auto “Zone” mode, the speed is adjusted automatically as shown in the figure below. Fans are assigned to a zone(s). It is possible to have more than one fan assigned to a thermal zone or to have multiple zones assigned to one fan.

FIGURE 20-5: on page 80 shows the control for the auto fan algorithm. The part allows a minimum temperature to be set, below which the fan will run at minimum speed. The minimum speed is programmed in the PWMx Minimum Duty cycle registers (64h-66h) and may be zero. A temperature range is specified over which the part will automatically adjust the fan speed. The fan will go to a duty cycle computed by the auto fan algorithm. As the temperature rises, the duty cycle will increase until the fan is running at full-speed when the temperature reaches the minimum plus the range value. The effect of this is a temperature feedback loop, which will cause the temperature to reach equilibrium between the minimum temperature and the minimum temperature plus the range. Provided that the fan has adequate cooling capacity for all environmental and power dissipation conditions, this system will maintain the temperature within acceptable limits, while allowing the fan to run slower (and quieter) when less cooling is required.

FIGURE 20-9: CASE 2 SPINUP OPERATION



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20.15 High Frequency PWM Options

Note:	If a fan with a tachometer output is driven by the high frequency PWM option, the tachometer must be monitored in Mode 1 only.

20.15.1 PWM FREQUENCIES SUPPORTED

The SCH3223 supports low frequency and high frequency PWMs. The low frequency options are 11.0Hz, 14.6Hz, 21.9Hz, 29.3Hz, 35.2Hz, 44.0Hz, 58.6Hz and 87.7Hz. The high frequency options are 15kHz, 20kHz, 25kHz and 30kHz. All PWM frequencies are derived from the 14.318MHz clock input.

The frequency of the PWM output is determined by the Frequency Select bits[3:0]. The default PWM frequency is 25kHz.

The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section and the Ramp Rate Control logic, unless the associated fan is in manual mode – see below.

Note:	When the device is configured for Manual Mode, the Ramp Rate Control logic should be disabled.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note:	If the current PWM duty cycle registers are written while the part is not in manual mode or when the start bit is zero, the data will be stored in internal registers that will only be active and observable when the start bit is set and the fan is configured for manual mode. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

Manual Mode (Test Mode)

In manual mode, when the start bit is set to 1 and the lock bit is 0, the current duty cycle registers are writeable to control the PWMs.

Note:	When the lock bit is set to 1, the current duty cycle registers are Read-Only.

The PWM duty cycle is represented as follows:

TABLE 21-4: PWM DUTY VS REGISTER READING

Current Duty	Value (Decimal)	Value (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

During spin-up, the PWM duty cycle is reported as 0%.

Note 1: The PWMx Current Duty Cycle always reflects the current duty cycle on the associated PWM pin.

2: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

21.2.6 REGISTER 3DH: DEVICE ID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Dh	R	Device ID	7	6	5	4	3	2	1	0	8Ch

The Device ID register contains a unique value to allow software to identify which device has been implemented in a given system.

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Bit[4] SUREN: Spin-up reduction enable. This bit enables the reduction of the spin-up time based on feedback from all fan tachometers associated with each PWM. 0=disable, 1=enable (default)

Bit[5] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[5] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[6] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[7] Initialization

Setting the INIT bit to '1' performs a soft reset. This bit is self-clearing. Soft Reset sets all the registers except the Reading Registers to their default values.

21.2.28 REGISTER 80H: INTERRUPT ENABLE 2 REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
80h	R/W	Interrupt Enable 2 (Fan Tachs)	RES	RES	RES	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	FAN-TACH	1Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual fan tach error events to set the corresponding status bits in the interrupt status registers. This register also contains the group fan tach enable bit (Bit[0] TACH), which is used to enable fan tach events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] FANTACH (Group TACH Enable)

0= Out-of-limit tachometer readings do not affect the state of the nHWM_INT pin (default)

1= Enable out-of-limit tachometer readings to make the nHWM_INT pin active low

Bit[1] Fantach 1 Event Enable

Bit[2] Fantach 2 Event Enable

Bit[3] Fantach 3 Event Enable

Bit[4] Reserved

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual fan tach error event bits are defined as follows:

0= disable

1= enable.

21.2.29 REGISTER 81H: TACH_PWM ASSOCIATION REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
81h	R/W	TACH_PWM Association	RES	RES	T3H	T3L	T2H	T2L	T1H	T1L	24h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

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21.2.54 REGISTER B5H: MIN TEMP ADJUST TEMP AND DELAY AMB (ZONE 2)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B5h	R/W	Min Temp Adjust Temp and Delay (Zone 2)	RES	RES	AMATP 1	AMATP 0	RES	RES	AMAD1	AMAD0	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits[5:4] Min Temp Adjust for Ambient Temp Sensor (Zone 2)

See Register B4h: Min Temp Adjust Temp RD1, RD2 (Zones 1& 3) on page 131 for a definition of the Min Temp Adjust bits.

Bits[1:0] Min Temp Adjust Delay for Ambient Temp Sensor (Zone 2)

See Register B6h: Min Temp Adjust Delay RD1, RD2 (ZONE 1 & 3) Register on page 132 for a definition of the Min Temp Delay bits.

21.2.55 REGISTER B6H: MIN TEMP ADJUST DELAY RD1, RD2 (ZONE 1 & 3) REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B6h	R/W	Min Temp Adjust Temp and Delay RD1, RD2 (Zones 1 & 3)	R1 AD1	R1 AD0	R2 AD1	R2 AD0	RES	RES	RES	RES	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits[7:4] are the bits to program the time delay for subsequently adjusting the low temperature limit value for zones 1&3 once an adjustment is made. These bits are defined as follows: RxAD[1:0]:

- 00= 1min (default)
- 01= 2min
- 10= 3min
- 11= 4min

Note: The Zones are hardwired to the sensors in the following manner:

- R1AD[1:0] = Zone 1 = Remote Diode 1
- AMAD[1:0] = Zone 2 = Ambient
- R2AD[1:0] = Zone 3 = Remote Diode 2

21.2.56 REGISTER B7H: MIN TEMP ADJUST ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B7h	R/W	Tmin Adjust Enable	RES	RES	RES	RES	TMIN_ ADJ_ EN2	TMIN_ ADJ_ EN1	TMIN_ ADJ_ ENA	TOP_ INT_ EN	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register is used to enable the Automatic Minimum Temperature Adjustment (AMTA) feature for each zone. AMTA allows for an adjustment of the low temp limit temperature register for each zone when the current temperature for the zone exceeds the Top Temperature. Bits[3:1] are used to enable an adjustment of the low temp limit for each of zones 1-3.

This register also contains the bit (TOP_INT_EN) to enable an interrupt to be generated anytime the top temp for any zone is exceeded. This interrupt is generated based on a bit in the Top Temp Exceeded status register (0B8h) being set. Note that the INT_EN bit (register 7Ch) must also be set for an interrupt to be generated on the THERM pin.

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This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to '1' if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

21.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default)

21.2.67 REGISTER CEH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CEh	R/W		RES	RES	RES	RES	RES	RD2 _INT_ EN	RD1 _INT_ EN	AMB_ INT_ EN	00h

21.2.68 REGISTERS D1,D6,DBH: PWM MAX SEGMENT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
0D1h	R/W	PWM1 Max	7	6	5	4	3	2	1	0	FFh
0D6h	R/W	PWM2 Max	7	6	5	4	3	2	1	0	FFh
0DBh	R/W	PWM3 Max	7	6	5	4	3	2	1	0	FFh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Registers 0D1h, 0D6h and 0DBh are used to program the Max PWM duty cycle for the fan function for each PWM.

21.2.69 REGISTER E0H: ENABLE LSBS FOR AUTO FAN

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
E0h	R/W	Enable LSbs for AutoFan	RES	RES	PWM3_ n1	PWM3_ n0	PWM2_ n1	PWM2_ n0	PWM1_ n1	PWM1_ n0	00h

Bits[7:6] Reserved

Bits[5:4] PWM3_n[1:0]

Bits[3:2] PWM2_n[1:0]

Bits[1:0] PWM1_n[1:0]

The PWMx_n[1:0] configuration bits allow the autofan control logic to utilize the extended resolution bits in the temperature reading. Increasing the precision reduces the programmable temperature range that can be used to control the PWM outputs. For a description of the programmable temperature ranges see Registers 5F-61h: Zone Temperature Range, PWM Frequency on page 116.

TABLE 23-2: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
LED2 Default = 0x00 on VTR POR	5E (R/W)	LED2 Bit[1:0] LED2 Control 00=off 01=blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and PCI Reset	65 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and PCI Reset	66 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and PCI Reset	67 (R/W)	Watch-dog timer Configuration Bit[2:0] Reserved Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = IRQ2 (Note) 0001 = IRQ1 0000 = Disable **Note:** IRQ2 is used for generating SMI events via the serial IRQ's stream. The WDT should not be configured for IRQ2 if the IRQ2 slot is enabled for generating an SMI event.
WDT_CTRL Default = 0x00 on VCC POR and VTR POR Default = 0000000xb on PCI Reset • Bit[0] is not cleared by PCI Reset	68 (R/W) Bit[2] is Write-Only	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] Reserved Bit[7:4] Reserved. Set to 0
TEST Default=0x00 on Vbat POR	6D (R/W)	Test Register. Test Registers are reserved for MCHP. Users should not write to this register, may produce undesired results.
GP44 Default = 0x80 on VTR POR	6Eh (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=GPIO 0=nIDE_RSTDRV (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

TABLE 25-1: BUFFER OPERATIONAL RATINGS (CONTINUED)

SUPER I/O BLOCK (T_A INDUSTRIAL = -40°C – +85°C, V_{CC} = +3.3 V ± 10%) OR (T_A COMMERCIAL = 0°C – +70°C, V_{CC} = +3.3 V ± 10%)						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Comments**
OD4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}			5.5	V	Open Drain;
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
IO8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
IS/O8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	Schmitt Trigger
High Input Level	V_{IHI}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA

TABLE 25-1: BUFFER OPERATIONAL RATINGS (CONTINUED)

SUPER I/O BLOCK (T_A INDUSTRIAL = -40°C – +85°C, V_{CC} = +3.3 V ± 10%) OR (T_A COMMERCIAL = 0°C – +70°C, V_{CC} = +3.3 V ± 10%)						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Comments**
5V Tolerant Pins (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#) Inputs and Outputs in High Impedance State						
Input High Current	$ILEAK_{IH}$			10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
LPC Bus Pins (LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$ILEAK_{IH}$			10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
V_{CC} Supply Current Active	I_{CC}			1 (Note 25-2)	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Trickle Supply Voltage	V_{TR}	2.97 (Note 25-3)	3.3	3.63	V	
V_{TR} Supply Current Active	I_{TR}			20 (Note 25-2, Note 25-4)	mA	All outputs, all inputs transitioning from/to 0V to/from 3.3V.
Battery Supply Voltage	V_{BAT}	2.2	3.0	3.6	V	
V_{BAT} Average Supply Current Active					µA	All outputs open, all inputs transitioning to/from 0V from/to 3.0V).
V_{BAT} Monitoring Active	$I_{BAT, AVG}$			1.5		
V_{BAT} Monitoring Disabled	$I_{BAT, AVG}$			1.0		
V_{BAT} Peak Supply Current Active **V_{BAT} Monitoring Active**	$I_{BAT, Peak}$			10	µA	All outputs open, all inputs transitioning to/from 0V from/to 3.0V).

HARDWARE MONITORING BLOCK (T_A = 0°C – +70°C, HVTR = +3.3 V ± 10%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3	±0.25	+3	°C	0°C <= T_A <= 70°C
		-2		+2	°C	40°C <= T_A <= 70°C
External Diode Sensor Accuracy					°C	Resolution
		-5	±0.25	+5	°C	-40°C <= T_S <= 125°C
		-3		+3	°C	40°C <= T_S <= 100°C
					°C	Resolution

APPENDIX A: ADC VOLTAGE CONVERSION

TABLE A-1: ANALOG-TO-DIGITAL VOLTAGE CONVERSIONS FOR HARDWARE MONITORING BLOCK

Input Voltage					A/D Output	
+12 V	**+5 V** Note 27-1	**+3.3 V** Note 27-2	**+2.5V**	**1.5V**	**Decimal**	**Binary**
<0.062	<0.026	<0.0172	<0.013	<0.008	0	0000 0000
0.062–0.125	0.026–0.052	0.017–0.034	0.013 - 0.031	0.008 - 0.015	1	0000 0001
0.125–0.188	0.052–0.078	0.034–0.052	0.031 - 0.039	0.015 - 0.024	2	0000 0010
0.188–0.250	0.078–0.104	0.052–0.069	0.039 - 0.052	0.024 - 0.031	3	0000 0011
0.250–0.313	0.104–0.130	0.069–0.086	0.052 - 0.065	0.031 - 0.039	4	0000 0100
0.313–0.375	0.130–0.156	0.086–0.103	0.065 - 0.078	0.039 - 0.047	5	0000 0101
0.375–0.438	0.156–0.182	0.103–0.120	0.078 - 0.091	0.047 - 0.055	6	0000 0110
0.438–0.500	0.182–0.208	0.120–0.138	0.091 - 0.104	0.055 - 0.063	7	0000 0111
0.500–0.563	0.208–0.234	0.138–0.155	0.104 - 0.117	0.063 - 0.071	8	0000 1000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
4.000–4.063	1.666–1.692	1.100–1.117	0.833 - 0.846	0.501 - 0.508	64 (1/4 Scale)	0100 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
8.000–8.063	3.330–3.560	2.200–2.217	1.665- 1.780	1.001 - 1.009	128 (1/2 Scale)	1000 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
12.000–12.063	5.000–5.026	3.300–3.317	2,500 - 2.513	1.502 - 1.509	192 (3/4 Scale)	1100 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
15.312–15.375	6.380–6.406	4.210–4.230	3.190 - 3.200	1.916 - 1.925	245	1111 0101
15.375–15.437	6.406–6.432	4.230–4.245	3.200 - 3.216	1.925 - 1.931	246	1111 0110
15.437–15.500	6.432–6.458	4.245–4.263	3.216 - 3.229	1.931 - 1.948	247	1111 0111
15.500–15.563	6.458–6.484	4.263–4.280	3.229 - 3.242	1.948 - 1.947	248	1111 1000
15.625–15.625	6.484–6.510	4.280–4.300	3.242 - 3.255	1.947 - 1.957	249	1111 1001
15.625–15.688	6.510–6.536	4.300–4.314	3.255 - 3.268	1.957 - 1.963	250	1111 1010
15.688–15.750	6.536–6.562	4.314–4.330	3.268 - 3.281	1.963 - 1.970	251	1111 1011
15.750–15.812	6.562–6.588	4.331–4.348	3.281 - 3.294	1.970 - 1.978	252	1111 1100
15.812–15.875	6.588–6.615	4.348–4.366	3.294 - 3.308	1.978 - 1.987	253	1111 1101
15.875–15.938	6.615–6.640	4.366–4.383	3.308 - 3.320	1.987 - 1.994	254	1111 1110
>15.938	>6.640	>4.383	> 3.320	> 1.994	255	1111 1111

Note 27-1 The 5V input is a +5V nominal inputs. 2.5V input is a 2.5V nominal input.

Note 27-2 The VCC, VTR, and Vbat inputs are +3.3V nominal inputs. VCC and VTR are nominal 3.3V power supplies. Vbat is a nominal 3.0V power supply.