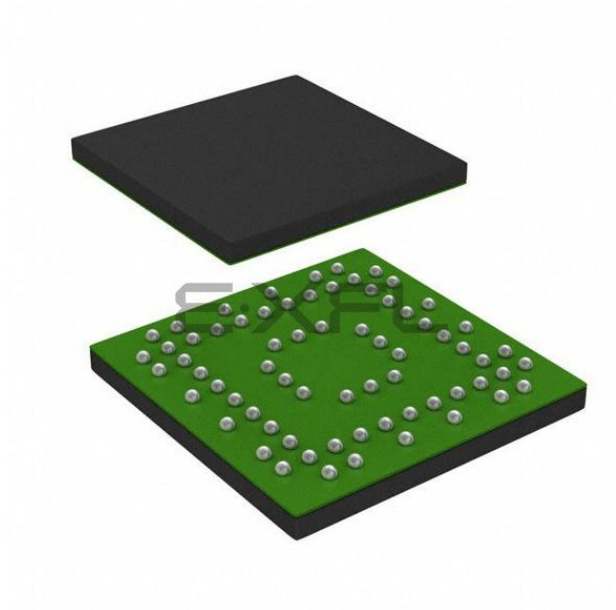


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8024 Keyboard Controller
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	LPC, Serial, UART
Number of I/O	19
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFBGA
Supplier Device Package	64-WFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3223i-7u

The following functions will not work under VTR power (VCC removed) if the external 32KHz clock is not connected. These functions will work under VCC power even if the external 32 KHz clock is not connected.

- LED blink
- Power Recovery Logic
- WDT
- Front Panel Reset with Input Debounce, Power Supply Gate, and CPU Powergood Signal Generation

4.6 Super I/O Functions

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The super I/O pins that are powered by VTR are as follows: GP42/nIO_PME, GP60/LED1, and GP61/LED2. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum Vbat current, I_{bat}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

4.7 Power Management Events (PME/SCI)

The SCH3223 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the Section 12.0, "PME Support," on page 46 section.

5.0 SIO OVERVIEW

The SCH3223 is a Super I/O Device with hardware monitoring. The Super I/O features are implemented as logical devices accessible through the LPC interface. The Super I/O blocks are powered by VCC, VTR, or Vbat. The Hardware Monitoring block is powered by HVTR and is accessible via the LPC interface. The following chapters define each of the functional blocks implemented in the SCH3223, their corresponding registers, and physical characteristics.

This chapter offers an introduction into the Super I/O functional blocks, registers and host interface. Details regarding the hardware monitoring block are defined in later chapters. Note that the Super I/O registers are implemented as typical Plug-and-Play components.

5.1 Super I/O Registers

The address map, shown below in Table 5-1 shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of all the Super I/O Logical Blocks, including the configuration register block, can be moved or relocated via the configuration registers.

Note: Some addresses are used to access more than one register.

5.2 Host Processor Interface (LPC)

The host processor communicates with the Super I/O features in the SCH3223 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 5-1, "Super I/O Block Addresses". Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Note: The SCH3223 does not use or need LPC DMA.

TABLE 5-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name	Logical Device	Notes
na	Reserved	0, 1, 2, 3	
Base+(0-7)	Serial Port Com 1	4	
Base+(0-7)	Serial Port Com 2	5	
na	Reserved	6, 7, 8, 9	
Base1 + (0-7F) Base2 + (0-1F)	Runtime Registers Security Key Registers	A	(Note 5-2)
na	Reserved	B, C, D, E, F	
Base + (0-1)	Configuration		(Note 5-1)

Note 5-1 Refer to the configuration register descriptions for setting the base address.

Note 5-2 Logical Device A is referred to as the Runtime Register block at Base1 or PME Block and may be used interchangeably throughout this document.

Note 5-3 na = not applicable

7.1.3 INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH3223. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic “1”.

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic “1”.

Bit 2

This bit enables the Received Line Status Interrupt when set to logic “1”. The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic “1”. This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic “0”.

7.1.4 FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCRs are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x21).

Bit 0

Setting this bit to a logic “1” enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic “0” disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic “1” clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic “1” clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the Trigger Level For The Rcvr Fifo Interrupt.

SER_IRQ Sampling Periods		
SER_IRQ Period	**Signal Sampled**	**# of Clocks Past Start**
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the nIO_SMI pin via bit 7 of the SMI Enable Register 2.

9.4 Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuous mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

9.5 Latency

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

9.6 EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

9.7 AC/DC Specification Issue

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

9.8 Reset and Initialization

The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to ensure SER_IRQ bus is in IDLE state before the system configuration changes.

13.0 WATCHDOG TIMER

The SCH3223 contains a Watchdog Timer (WDT). The Watchdog Time-out status bit may be mapped to an interrupt through the WDT_CFG Runtime Register.

Note:	Reset conditions from legacy Keyboard or Mouse interrupts cannot occur in the SCH3223.

The SCH3223 WDT has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register. The WDT time-out value is set through the WDT_VAL Runtime register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

Note 13-1 To set the WDT for time X minutes, the value of X+1 minutes must be programmed. To set the WDT for X seconds, the value of X+1 seconds must be programmed.

The Watchdog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. The WDT interrupt is mapped to an interrupt channel through the WDT_CFG Runtime register. When mapped to an interrupt the interrupt request pin reflects the value of the WDT time-out status bit.

The host may force a Watchdog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Runtime register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watchdog Status). Bit 2 of the WDT_CTRL is self-clearing.

See the Section 23.0, "Runtime Registers" for description of these registers.

TABLE 19-2: DESCRIPTION OF SECURITY KEY CONTROL (SKC) REGISTER BITS[2:1]

Bit[2] (Write-Lock)	Bit[1] (Read-Lock)	Description
0	0	Security Key Bytes[31:0] are read/write registers
0	1	Security Key Bytes[31:0] are Write-Only registers
1	0	Security Key Bytes[31:0] are Read-Only registers
1	1	Security Key Bytes[31:0] are not accessible. All reads/write access is denied.

Note: When Bit[1] (Read-Lock) is '1' all reads to this register block will return 00h.

- As an added layer of protection, bit [0] SKC Register Lock bit has been added to the Security Key Control Register. This lock bit is used to block write access to the Write-Lock and Read-Lock bits defined in the table above. Once this bit is set it can only be cleared by a VTR POR, VCC POR, and PCI Reset.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly.

The results of each sampling and conversion can be found in the Reading Registers and are available at any time, however, they are only updated once per conversion cycle.

20.8 Interrupt Status Registers

The Hardware Monitor Block contains two primary interrupt status registers (ISRs):

- Interrupt Status Register 1 (41h)
- Interrupt Status Register 2 (42h)

There is also a secondary set of interrupt status registers:

- Interrupt Status Register 1 - Secondary (A5h)
- Interrupt Status Register 2 - Secondary (A6h)

Note 1: The status events in the primary set of interrupt status registers is mapped to a PME bit, an SMI bit, to Serial IRQ (See Interrupt Event on Serial IRQ on page 73), and to the nHWM_INT pin.

2: The nHWM_INT pin is deasserted when all of the bits in the primary ISRs (41h, 42h) are cleared. The secondary ISRs do not affect the nHWM_INT pin.

3: The primary and secondary ISRs share all of the interrupt enable bits for each of the events.

These registers are used to reflect the state of all temperature and fan violation of limit error conditions and diode fault conditions that the Hardware Monitor Block monitors.

When an error occurs during the conversion cycle, its corresponding bit is set (if enabled) in its respective interrupt status register. The bit remains set until the register bit is written to ‘1’ by software, at which time the bit will be cleared to ‘0’ if the associated error event no longer violates the limit conditions or if the diode fault condition no longer exists. Writing ‘1’ to the register bit will not cause a bit to be cleared if the source of the status bit remains active.

These registers default to 0x00 on a VCC POR, VTR POR, and Initialization. (See Resetting the SCH3223 Hardware Monitor Block on page 67.)

The following section defines the Interrupt Enable Bits that correspond to the Interrupt Status registers listed above. Setting or clearing these bits affects the operation of the Interrupt Status bits.

20.8.1 INTERRUPT ENABLE BITS

Each interrupt event can be enabled into the interrupt status registers. See the figure below for the status and enable bits used to control the interrupt bits and nHWM_INT pin. Note that a status bit will not be set if the individual enable bit is not set.

The following is a list of the Interrupt Enable registers:

- Interrupt Enable Register - Fan Tachs (80h)
- Interrupt Enable Register - Temp (82h)

Note:	Clearing the individual enable bits will clear the corresponding individual status bit.

Clearing the individual enable bits. There are two cases and in both cases it is not possible to change the individual interrupt enable while the start bit is set.

1. The interrupt status bit will never be set when the individual interrupt enable is cleared. Here the interrupt status bit will not get set when the start bit is set, regardless of whether the limits are violated during a measurement.
2. If an interrupt status bit had been set from a previous condition, clearing the start bit and then clearing the individual interrupt enable bit will not clear the associated interrupts status bit immediately. It will be cleared when the start bit is set, when the associated reading register is updated.

20.11 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a 3904 type diode.

20.11.1 INTERNAL TEMPERATURE MEASUREMENT

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the programmed limits in the Internal High Temperature Limit register (51h) and the Internal Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 77.

20.11.2 EXTERNAL TEMPERATURE MEASUREMENT

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then the corresponding Remote Diode 1 (D1) or Remote Diode 2 (D2) status bits will be set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 77.

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-). Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be forced to 80h. Note that this will cause the associated remote diode limit exceeded status bit to be set (i.e. Remote Diode x Limit Error bits (D1 and D2) are located in the Interrupt Status 1 Register at register address 41h).

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

20.11.3 TEMPERATURE DATA FORMAT

Temperature data can be read from the three temperature registers:

- Internal Temp Reading register (26h)
- Remote Diode 1 Temp Reading register (25h)
- Remote Diode 2 Temp Reading register (27h)

The following table shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 ^{0}C.

TABLE 20-3: TEMPERATURE DATA FORMAT

Temperature	Reading (DEC)	Reading (HEX)	Digital Output
-127^{0}C	-127	81h	1000 0001
⋮	⋮	⋮	⋮
-50 ^{0}C	-50	CEh	1100 1110
⋮	⋮	⋮	⋮
-25 ^{0}C	-25	E7h	1110 0111
⋮	⋮	⋮	⋮
-1 ^{0}C	-1	FFh	1111 1111
0 ^{0}C	0	00h	0000 0000

20.13.3 PWM FAN SPEED CONTROL

The following description applies to PWM1, PWM2, and PWM3.

Note: The PWM output pins are held low when VCC=0. The PWM pins will be forced to “spinup” when PWRGD_PS goes active. See “Spin Up” on page 80.

The PWM pin reflects a duty cycle that is determined based on 256 PWM duty cycle intervals. The minimum duty cycle is “off”, when the pin is low, or “full on” when the pin is high for 255 intervals and low for 1 interval. The INVERT bit (bit 4 of the PWMx Configuration registers at 80h-82h) can be used to invert the PWM output, however, the default operation (following a VCC POR) of the part is based on the PWM pin active high to turn the fans “on”. When the INVERT bit is set, as long as power is not removed from the part, the inversion of the pin will apply thereafter.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high for 255 clocks and low for 1 clock (INVERT bit = 0). The exception to this is during fan spin-up when the PWM pin will be forced high for the duration of the spin-up time.

The SCH3223 can control each of the PWM outputs in one of two modes:

- Manual Fan Control Operating Mode: software controls the speed of the fans by directly programming the PWM duty cycle.
- Auto Fan Control Mode: the device automatically adjusts the duty cycle of the PWM outputs based on temperature, according to programmed parameters.

These modes are described in sections that follow.

20.13.3.1 Manual Fan Control Operating Mode (Test Mode)

When operating in Manual Fan Control Operating Mode, software controls the speed of the fans by directly programming the PWM duty cycle. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The SCH3223 offers the option of generating an interrupt indicated by the nHWM_INT signal.

To control the PWM outputs in manual mode:

- To set the mode to operate in manual mode, write ‘111’ to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWMx Configuration.
- The speed of the fan is controlled by the duty cycle set for that PWM output. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

Fans equipped with Tachometer outputs can be monitored via the FANTACHx input pins. See Section 20.14.2, "Fan Speed Monitoring," on page 93.

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the nHWM_INT pin (if enabled). Software must handle the interrupt condition and modify the operation of the device accordingly. Software can evaluate the operation of the Fan Control device through the Temperature and Fan Tachometer Reading registers.

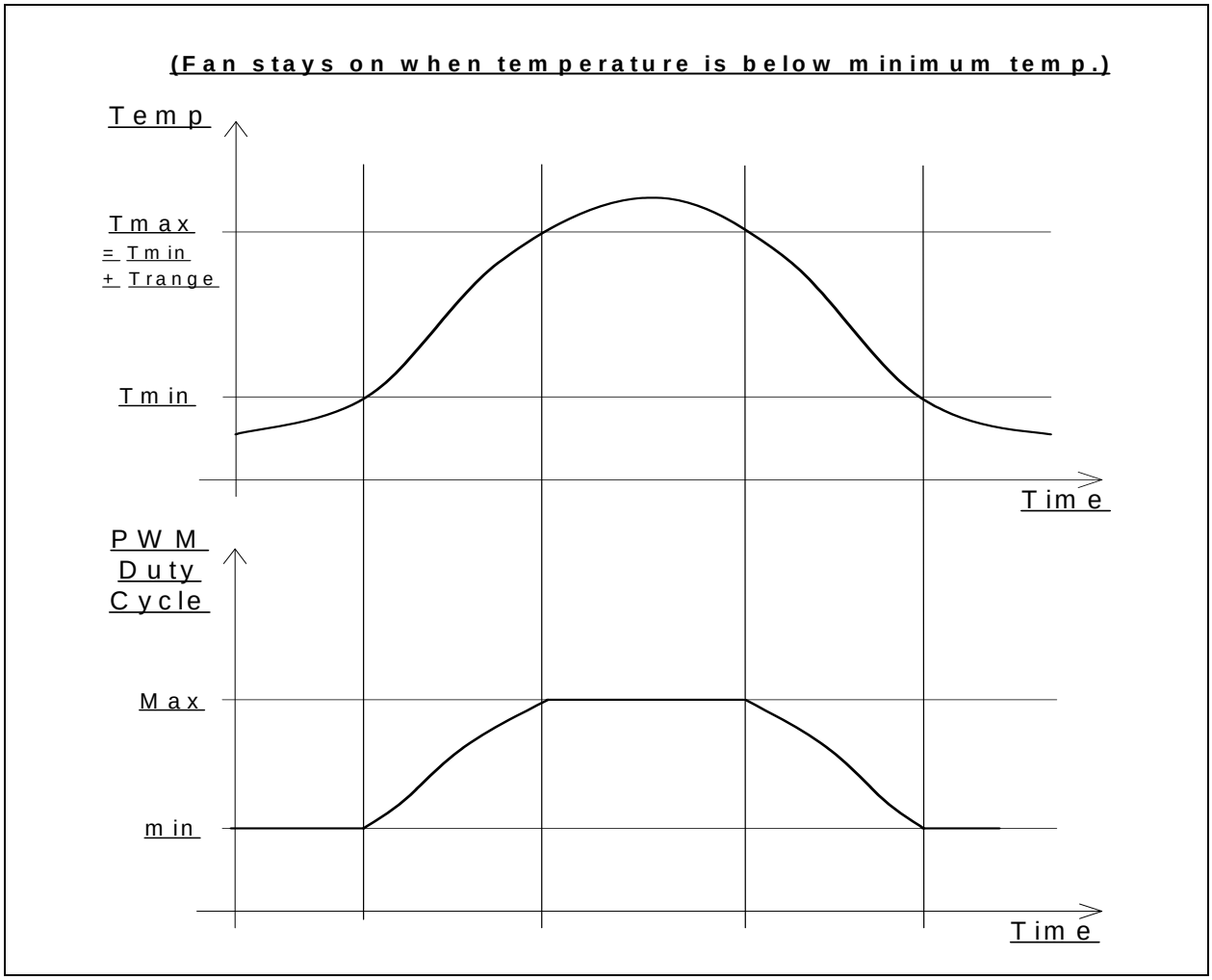
When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writable when the lock bit is set.

Note: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

20.13.3.2 Auto Fan Control Operating Mode

The SCH3223 implements automatic fan control. In Auto Fan Mode, this device automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart on the following page (see FIGURE 20-4: Automatic Fan Control Flow Diagram on page 78).

FIGURE 20-5: AUTOMATIC FAN CONTROL



20.13.3.3 Spin Up

When a fan is being started from a stationary state (PWM duty cycle =00h), the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan (i.e., to get the fan turning). Following this spin up time, the fan will go to the duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

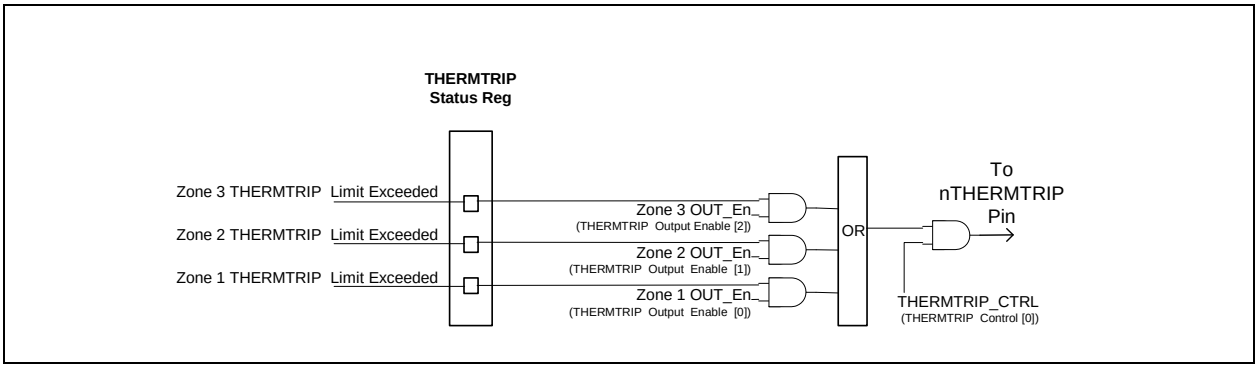
To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up.

Auto Fan operation during Spin Up:

The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit (see Figure 20-6), or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.

The following figures summarize the THERMTRIP operation in relation to the THERMTRIP status bits.

FIGURE 20-15: NTHERMTRIP OUTPUT OPERATION



20.14.2 FAN SPEED MONITORING

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

The tachometers will operate in one of two modes:

- Mode 1: Standard tachometer reading mode. This mode is used when the fan is always powered when the duty cycle is greater than 00h.
- Mode 2: Enhanced tachometer reading mode. This mode is used when the PWM is pulsing the fan.

20.14.2.1 TACH Inputs

The tachometer inputs are implemented as digital input buffers with logic to filter out small glitches on the tach signal.

20.14.2.2 Selecting the Mode of Operation:

The mode is selected through the Mode Select bits located in the Tach Option register. This Mode Select bit is defined as follows:

- 0=Mode 1: Standard tachometer reading mode
- 1=Mode 2: Enhanced tachometer reading mode.

Default Mode of Operation:

- Mode 1
- Slow interrupt disabled (Don't force FFFEh)
- Tach interrupt enabled via enable bit
- Tach Limit = FFFFh
- Tach readings updated once a second

20.14.2.3 Mode 1 – Always Monitoring

Mode 1 is the simple case. In this mode, the Fan is always powered when it is ‘ON’ and the fan tachometer output ALWAYS has a valid output. This mode is typically used if a linear DC Voltage control circuit drives the fan. In this mode, the fan tachometer simply counts the number of 90kHz pulses between the programmed number of edges (default = 5 edges). The fan tachometer reading registers are continuously updated.

The counter is used to determine the period of the Fan Tachometer input pulse. The counter starts counting on the first edge and continues counting until it detects the last edge or until it reaches FFFFh. If the programmed number of edges is detected on or before the counter reaches FFFFh, the reading register is updated with that count value. If the counter reaches FFFFh and no edges were detected a stalled fan event has occurred and the Tach Reading register will be set to FFFFh. If one or more edges are detected, but less than the programmed number of edges, a slow fan event has

TABLE 21-1: REGISTER SUMMARY (CONTINUED)

Reg Addr	Read/ Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	
9Bh	R	VTR Limit Low		7	6	5	4	3	2	1	0	00h	No	
9Ch	R/W	VTR Limit Hi		7	6	5	4	3	2	1	0	FFh	No	
9Dh	R/W	VBAT Limit Low										00h	No	
9Eh	R/W	VBAT Limit Hi		7	6	5	4	3	2	1	0	FFh	No	
9Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A0h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A1h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A2h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A3h	R/W	MCHP Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h N/A	Yes	
A4h	R	MCHP Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	02h	No	
A5h	R/WC	Interrupt Status 1 Secondary		INT23	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h Note 21-10	No	
A6h	R/WC	Interrupt Status 2 Secondary		ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h Note 21-10	No	
A7h	RWC	Interrupt Status 3 Secondary	INS3	RES	RES	RES	RES	RES	RES	VBAT	VTR	00h	No	
A8h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A9h	R/W	MCHP Test Register		7	6	5	4	3	2	1	0	00h	Yes	
AAh	R/W	MCHP Test Register		7	6	5	4	3	2	1	0	00h	Yes	
ABh	R/W	Tach 1-3 Mode		T1M1	T1M0	T2M1	T2M0	T3M1	T3M0	RES	RES	00h	No	
ACh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
ADh	R	MCHP Test Register		7	6	5	4	3	2	1	0	00h	No	
AEh	R/W	Top Temperature Remote Diode 1 (Zone 1)		7	6	5	4	3	2	1	0	2Dh Note 21-10	Yes	
AFh	R/W	Top Temperature Remote Diode 2 (Zone 3)		7	6	5	4	3	2	1	0	2Dh Note 21-10	Yes	
B0h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B1h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B2h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B3h	R/W	Top Temperature Ambient (Zone 2)		7	6	5	4	3	2	1	0	2Dh Note 21-10	Yes	
B4h	R/W	Min Temp Adjust Temp RD1, RD2		R1ATP1	R1ATP0	R2ATP1	R2ATP0	RES	RES	RES	RES	00h	Yes	
B5h	R/W	Min Temp Adjust Temp and Delay Amb		RES	RES	AMATP1	AMATP0	RES	RES	AMAD1	AMAD0	00h	Yes	
B6h	R/W	Min Temp Adjust Delay 1-2		R1AD1	R1AD0	R2AD1	R2AD0	RES	RES	RES	RES	00h	Yes	
B7h	R/W	Tmin Adjust Enable		RES	RES	RES	RES	TMIN_ADJ_EN2	TMIN_ADJ_EN1	TMIN_ADJ_ENA	TOP_INT_EN	00h	Yes	
B8h	R/WC	Top Temp Exceeded Status		RES	RES	RES	RES	RES	STS2	STS1	STSA	00h Note 21-10	No	
B9h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BAh	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	04h	Yes	
BBh	R	MCHP Reserved		7	6	5	4	3	2	1	0	00h	No	
BCh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BDh	R	MCHP Reserved		7	6	5	4	3	2	1	0	00h	No	
BEh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BFh	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	Yes	
C0h	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	Yes	
C1h	R/W	Thermtrip Control		RES	RES	RES	RES	RES	RES	RES	THER-MTRIP_CTRL	01h	Yes	
C2h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
C3h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	

Note 21-19 Vbat is a nominal 3.0V input source that has been implemented on a 3.3V analog voltage monitoring input.

21.2.13 REGISTERS 4E-53H: TEMPERATURE LIMIT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
4Eh	R/W	Remote Diode 1 Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Remote Diode 1 High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Ambient Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Ambient High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Remote Diode 2 Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Remote Diode 2 High Temp	7	6	5	4	3	2	1	0	7Fh

Setting the Lock bit has no effect on these registers.

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or is less than or equal to the value set in the low limit register, the corresponding bit will be set automatically by the SCH3223 in the Interrupt Status Register 1 (41h). For example, if the temperature reading from the Remote1- and Remote1+ inputs exceeds the Remote Diode 1 High Temp register limit setting, Bit[4] D1 of the Interrupt Status Register 1 will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 21-6.

TABLE 21-6: TEMPERATURE LIMITS VS. REGISTER SETTINGS

Temperature	Limit (DEC)	Limit (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

21.2.14 REGISTERS 54-59H: FAN TACHOMETER LOW LIMIT

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
54h	R/W	FANTACH1 Minimum LSB	7	6	5	4	3	2	1	0	FFh
55h	R/W	FANTACH1 Minimum MSB	15	14	13	12	11	10	9	8	FFh
56h	R/W	FANTACH2 Minimum LSB	7	6	5	4	3	2	1	0	FFh
57h	R/W	FANTACH2 Minimum MSB	15	14	13	12	11	10	9	8	FFh
58h	R/W	FANTACH3 Minimum LSB	7	6	5	4	3	2	1	0	FFh
59h	R/W	FANTACH3 Minimum MSB	15	14	13	12	11	10	9	8	FFh

Setting the Lock bit has no effect on these registers.

If an absolute limit register set to 80h (-128°c), the safety feature is disabled for the associated zone. That is, if 80h is written into the Zone x Temp Absolute Limit Register, then regardless of the reading register for the zone, the fans will not turn on-full based on the absolute temp condition.

Default =100°c=64h.

When any fan is in auto fan mode, then if the temperature in any zone exceeds absolute limit, all fans go to full, including any in manual mode, except those that are disabled. Therefore, even if a zone is not associated with a fan, if that zone exceeds absolute, then all fans go to full. In this case, the absolute limit can be chosen to be 7Fh for those zones that are not associated with a fan, so that the fans won't turn on unless the temperature hits 127 degrees.

TABLE 21-14: ABSOLUTE LIMIT VS. REGISTER SETTING

Absolute Limit	ABS Limit (Dec)	ABS Limit (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

21.2.21 REGISTERS 6D-6EH: MCHP TEST REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Dh	R/W	MCHP Test Register	7	6	5	4	3	2	1	0	44h
6Eh	R/W	MCHP Test register	7	6	5	4	RES	RES	RES	RES	40h

21.2.22 REGISTER 70-72H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
70h	R	MCHP Test Register	7	6	5	4	3	2	1	0	N/A
71h	R	MCHP Test Register	7	6	5	4	3	2	1	0	N/A
72h	R	MCHP Test Register	7	6	5	4	3	2	1	0	N/A

This is a read-only MCHP test register. Writing to this register has no effect.

21.2.23 REGISTER 73-78H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
73h	R	MCHP Test Register	RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h
74h	R/W	MCHP Test Register	RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h
75h	R	MCHP Test Register	RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h
76h	R/W	MCHP Test Register	RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h

21.2.51 REGISTER ADH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
ADh	R	MCHP Test Register	7	6	5	4	3	2	1	0	00h

This is a read-only MCHP test register. Writing to this register has no effect.

21.2.52 REGISTERS AE-AFH, B3H: TOP TEMPERATURE LIMIT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
AEh	R/W	Top Temperature Remote Diode 1 (Zone 1)	7	6	5	4	3	2	1	0	2Dh
AFh	R/W	Top Temperature Remote Diode 2 (Zone 3)	7	6	5	4	3	2	1	0	2Dh
B3h	R/W	Top Temperature Ambient (Zone 2)	7	6	5	4	3	2	1	0	2Dh

Note: These registers are reset to their default values when the powergood_ps signal transitions high.

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

The Top Temperature Registers define the upper bound of the operating temperature for each zone. If the temperature of the zone exceeds this value, the minimum temperature for the zone can be configured to be adjusted down.

The Top Temperature registers are used as a comparison point for the AMTA feature, to determine if the Low Temp Limit register for a zone should be adjusted down. The Top temp register for a zone is not used if the AMTA feature is not enabled for the zone. The AMTA feature is enabled via the Tmin Adjust Enable register at 0B7h.

21.2.53 REGISTER B4H: MIN TEMP ADJUST TEMP RD1, RD2 (ZONES 1& 3)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B4h	R/W	Min Temp Adjust Temp RD1, RD2 (Zones 1&3)	R1ATP1	R1ATP 0	R2ATP 1	R2ATP 0	RES	RES	RES	RES	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits[7:4] are used to select the temperature adjustment values that are subtracted from the Zone Low temp limit for zones 1& 3. There is a 2-bit value for each of the remote zones that is used to program the value that is subtracted from the low temp limit temperature register when the temperature reading for the zone reaches the Top Temperature for the AMTA feature. The AMTA feature is enabled via the Tmin Adjust Enable register at B7h.

These bits are defined as follows: ZxATP[1:0]:

- 00= 2oC (default)
- 01= 4oC
- 10= 6oC
- 11= 8oC

Note: The Zones are hardwired to the sensors in the following manner:

- R1ATP[1:0] = Zone 1 = Remote Diode 1
- AMATP[1:0] = Zone 2 = Ambient
- R2ATP[1:0] = Zone 3 = Remote Diode 2

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to '1' if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

21.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default)

21.2.67 REGISTER CEH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CEh	R/W		RES	RES	RES	RES	RES	RD2 _INT_ EN	RD1 _INT_ EN	AMB_ INT_ EN	00h

21.2.68 REGISTERS D1,D6,DBH: PWM MAX SEGMENT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
0D1h	R/W	PWM1 Max	7	6	5	4	3	2	1	0	FFh
0D6h	R/W	PWM2 Max	7	6	5	4	3	2	1	0	FFh
0DBh	R/W	PWM3 Max	7	6	5	4	3	2	1	0	FFh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Registers 0D1h, 0D6h and 0DBh are used to program the Max PWM duty cycle for the fan function for each PWM.

21.2.69 REGISTER E0H: ENABLE LSBS FOR AUTO FAN

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
E0h	R/W	Enable LSbs for AutoFan	RES	RES	PWM3_ n1	PWM3_ n0	PWM2_ n1	PWM2_ n0	PWM1_ n1	PWM1_ n0	00h

Bits[7:6] Reserved

Bits[5:4] PWM3_n[1:0]

Bits[3:2] PWM2_n[1:0]

Bits[1:0] PWM1_n[1:0]

The PWMx_n[1:0] configuration bits allow the autofan control logic to utilize the extended resolution bits in the temperature reading. Increasing the precision reduces the programmable temperature range that can be used to control the PWM outputs. For a description of the programmable temperature ranges see Registers 5F-61h: Zone Temperature Range, PWM Frequency on page 116.

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode.

Enter Configuration Mode

To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State. (The auto Config ports are enabled).

Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (a) is not required.

Exit Configuration Mode

To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note:	Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

Programming Example

The following is an example of a configuration program in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION MODE    |
;-----------------------------'
MOV DX,02EH
MOV AX,055H
OUT DX,AL
;-----------------------------.
; CONFIGURE REGISTER CRE0,    |
; LOGICAL DEVICE 8            |
;-----------------------------'
MOV DX,02EH
MOV AL,07H
OUT DX,AL ;Point to LD# Config Reg
MOV DX,02FH
MOV AL, 08H
OUT DX,AL;Point to Logical Device 8
;
MOV DX,02EH
MOV AL,E0H
OUT DX,AL; Point to CRE0
MOV DX,02fH
MOV AL,02H
OUT DX,AL; Update CRE0
;-----------------------------.
; EXIT CONFIGURATION MODE     |
;-----------------------------'
MOV DX,02EH
MOV AX,0AAH
OUT DX,AL
```

TABLE 25-1: BUFFER OPERATIONAL RATINGS (CONTINUED)

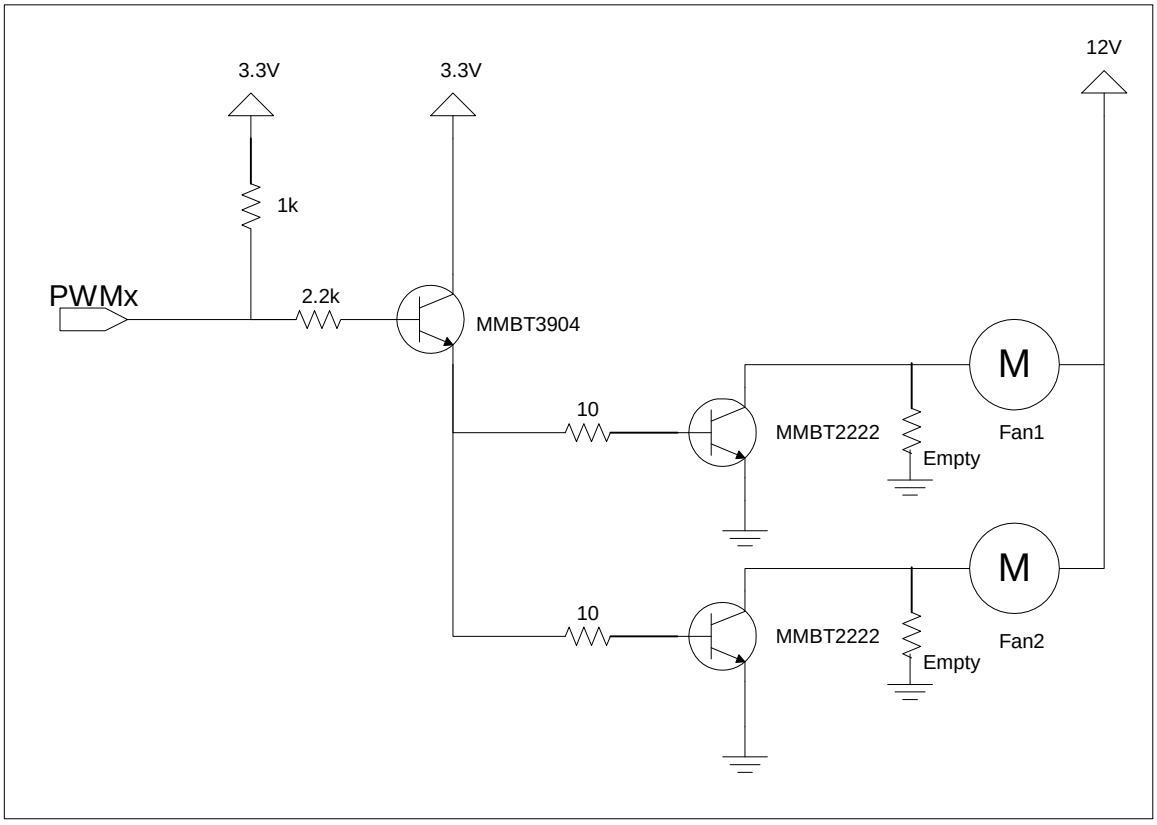
SUPER I/O BLOCK (T_A INDUSTRIAL = -40°C – +85°C, V_{CC} = +3.3 V ± 10%) OR (T_A COMMERCIAL = 0°C – +70°C, V_{CC} = +3.3 V ± 10%)						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Comments**
IO12 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IOP14 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
IOD16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OD_PH Type Buffer	VOL			0.3	V	RLOAD is 40ohms to 1.2V Max Output impedance is 10ohms
PCI Type Buffers (PCI_ICLK, PCI_I, PCI_O, PCI_IO)	3.3V PCI 2.1 Compatible.					
Leakage Current (ALL)						(Note 25-1)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Backdrive Protect/ChiProtect (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$ILEAK_{IH}$			10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V

APPENDIX B: EXAMPLE FAN CIRCUITS

The following figures show examples of circuitry on the board for the PWM outputs, tachometer inputs, and remote diodes. Figure B-1 shows how the part can be used to control four fans by connecting two fans to one PWM output.

Note:	These examples represent the minimum required components. Some designs may require additional components.

FIGURE B-1: FAN DRIVE CIRCUITRY FOR LOW FREQUENCY OPTION (APPLY TO PWM DRIVING TWO FANS)



APPENDIX C: REVISION HISTORY

TABLE C-1: SCH3223 DATA SHEET REVISION HISTORY

REVISION	SECTION/FIGURE/ENTRY	CORRECTION
DS00002028B (03-16-16)	Product Identification System on page 194	Part Ordering Codes updated
	Section 1.0, "General Description" and Section 21.1, "Undefined Registers"	Removal of the word “legacy” in describing unsupported features
DS00002028A (11-12-15)	Initial Release	