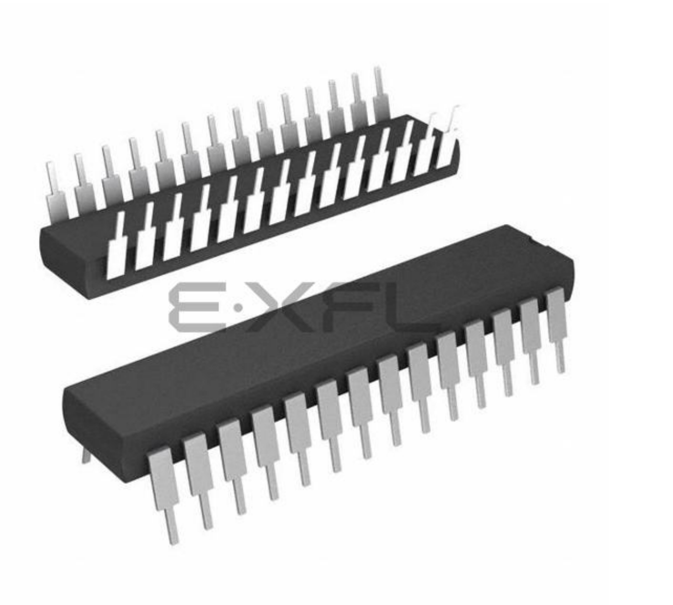


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	20
Program Memory Size	24KB (8K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3010-30i-sp

Special Microcontroller Features:

- Enhanced Flash Program Memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100K (typical)
- Data EEPROM Memory:
  - 100,000 erase/write cycle (min.) for industrial temperature range, 1M (typical)
- Self-Reprogrammable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with On-Chip Low-Power RC Oscillator for Reliable Operation
- Fail-Safe Clock Monitor Operation Detects Clock Failure and Switches to On-Chip Low-Power RC Oscillator
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes:
  - Sleep, Idle and Alternate Clock modes

CMOS Technology:

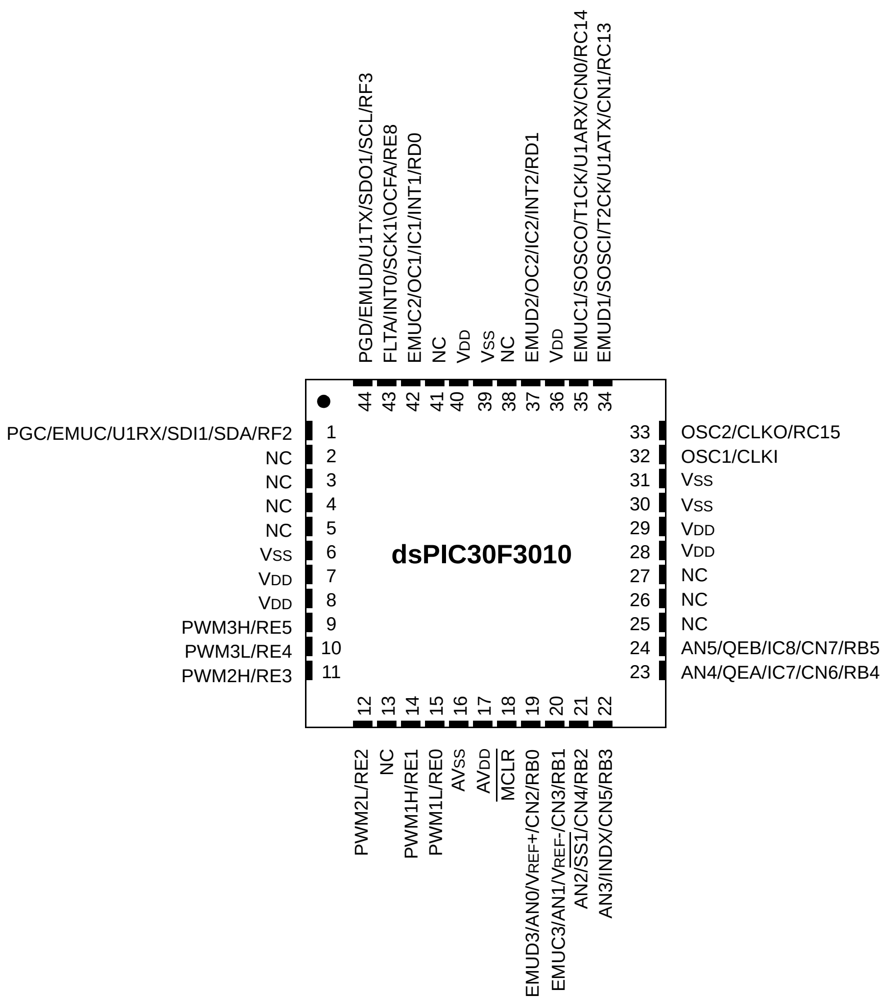
- Low-Power, High-Speed Flash Technology
- Wide Operating Voltage Range (2.5V to 5.5V)
- Industrial and Extended Temperature Ranges
- Low Power Consumption

dsPIC30F Motor Control and Power Conversion Family

Device	Pins	Program Mem. Bytes/ Instructions	SRAM Bytes	EEPROM Bytes	Timer 16-Bit	Input Cap	Output Comp/Std PWM	Motor Control PWM	A/D 10-Bit 1 Msps	Quad Enc	UART	SPI	I^2C^{TM}
dsPIC30F3010	28	24K/8K	1024	1024	5	4	2	6 ch	6 ch	Yes	1	1	1
dsPIC30F3011	40/44	24K/8K	1024	1024	5	4	4	6 ch	9 ch	Yes	2	1	1

Pin Diagrams (Continued)

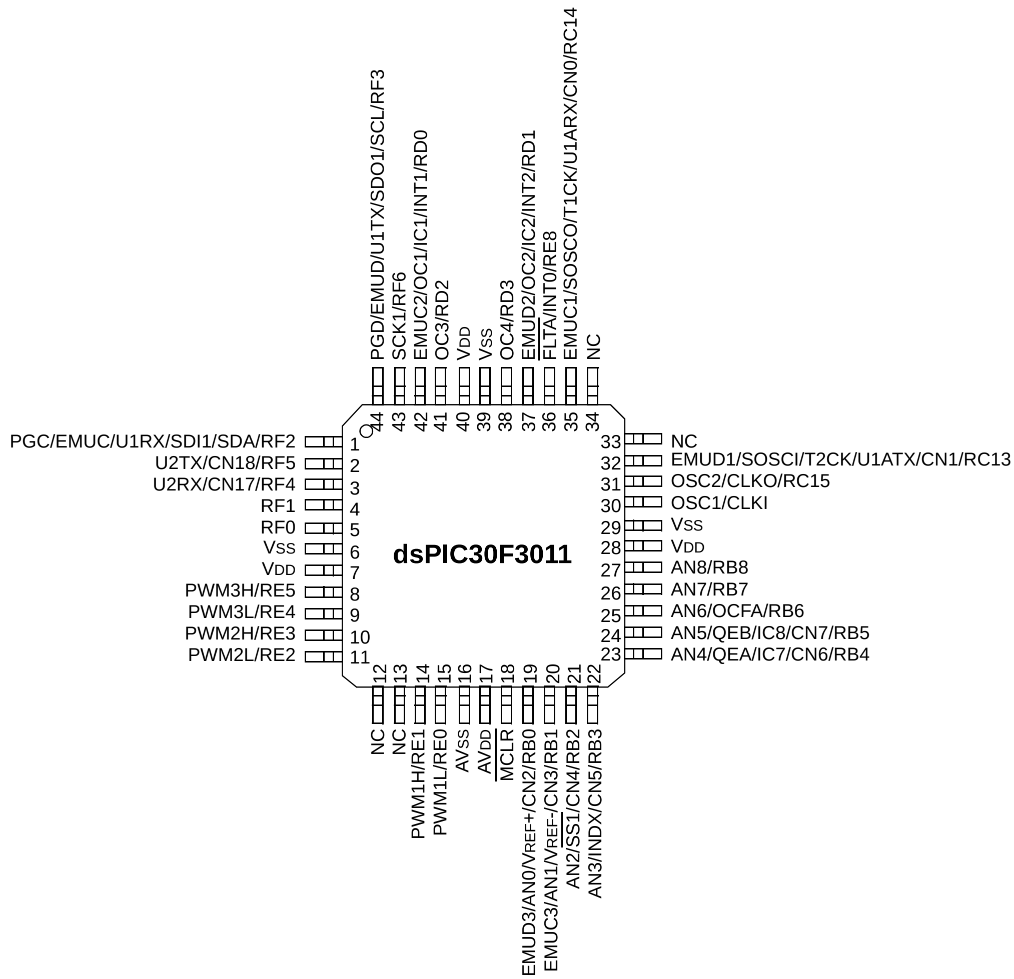
44-Pin QFN(1)



Note 1: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin TQFP



NOTES:

3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see **Section 3.1.2 “Data Access From Program Memory Using Program Space Visibility”**). The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lsw of any address within program space, without going through data space. The `TBLRDH` and `TBLWTH` instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

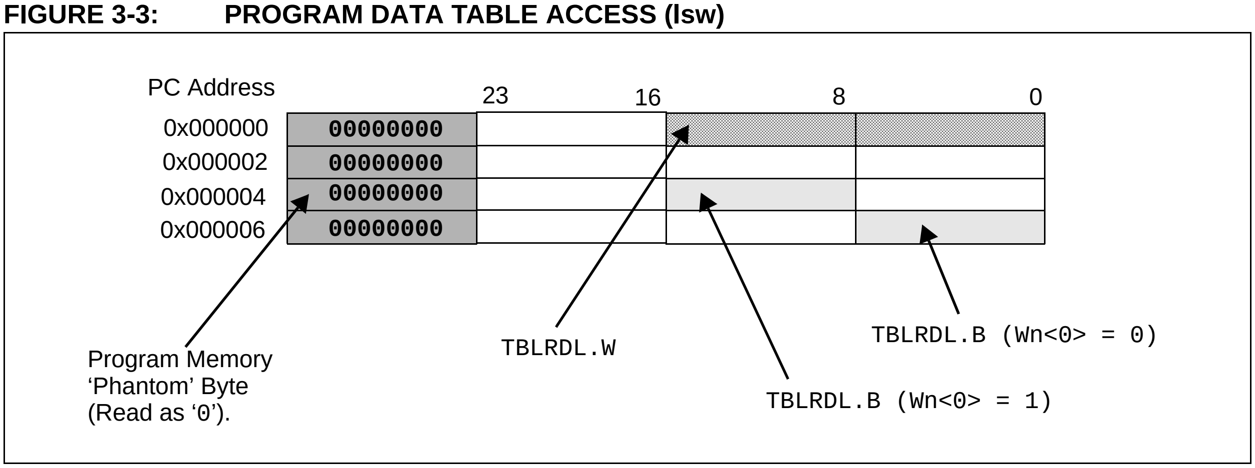
The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word-wide address spaces, residing side by side, each with the same address range. `TBLRDL` and `TBLWTL` access the space which contains the lsw, and `TBLRDH` and `TBLWTH` access the space which contains the MSB.

Figure 3-2 illustrates how the EA is created for table operations and data space accesses (PSV = `1`). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space.

1. **`TBLRDL:`** Table Read Low
   Word: Read the lsw of the program address;
   P<15:0> maps to D<15:0>.
   Byte: Read one of the LSBs of the program address;
   P<7:0> maps to the destination byte when byte select = `0`;
   P<15:8> maps to the destination byte when byte select = `1`.
2. **`TBLWTL:`** Table Write Low (refer to **Section 6.0 “Flash Program Memory”** for details on Flash programming).
3. **`TBLRDH:`** Table Read High
   Word: Read the msw of the program address;
   P<23:16> maps to D<7:0>; D<15:8> will always be = `0`.
   Byte: Read one of the MSBs of the program address;
   P<23:16> maps to the destination byte when byte select = `0`;
   The destination byte will always be = `0` when byte select = `1`.
4. **`TBLWTH:`** Table Write High (refer to **Section 6.0 “Flash Program Memory”** for details on Flash programming).

FIGURE 3-3: PROGRAM DATA TABLE ACCESS (lsw)



5.0 INTERRUPTS

> **Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*16-bit MCU and DSC Programmer's Reference Manual*" (DS70157).

The dsPIC30F3010/3011 has 29 interrupt sources and 4 processor exceptions (traps), which must be arbitrated based on a priority scheme.

The CPU is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the program counter. The interrupt vector is transferred from the program data bus into the program counter through a 24-bit wide multiplexer on the input of the program counter.

The Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004). The IVT and AIVT are shown in Figure 5-1.

The interrupt controller is responsible for pre-processing the interrupts and processor exceptions, prior to their being presented to the processor core. The peripheral interrupts and traps are enabled, prioritized and controlled using centralized Special Function Registers (SFR):

- IFS0<15:0>, IFS1<15:0>, IFS2<15:0>
  All interrupt request flags are maintained in these three registers. The flags are set by their respective peripherals or external signals, and they are cleared via software.
- IEC0<15:0>, IEC1<15:0>, IEC2<15:0>
  All interrupt enable control bits are maintained in these three registers. These control bits are used to individually enable interrupts from the peripherals or external signals.
- IPC0<15:0>... IPC11<7:0>
  The user-assignable priority level associated with each of these interrupts is held centrally in these twelve registers.
- IPL<3:0> The current CPU priority level is explicitly stored in the IPL bits. IPL<3> is present in the CORCON register, whereas IPL<2:0> are present in the STATUS Register (SR) in the processor core.
- INTCON1<15:0>, INTCON2<15:0>
  Global interrupt control functions are derived from these two registers. INTCON1 contains the control and status flags for the processor exceptions. The INTCON2 register controls the external interrupt request signal behavior and the use of the alternate vector table.

> **Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit. User software should ensure the appropriate Interrupt flag bits are clear prior to enabling an interrupt.

All interrupt sources can be user-assigned to one of 7 priority levels, 1 through 7, through the IPCx registers. Each interrupt source is associated with an interrupt vector, as shown in Table 5-1. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively.

> **Note:** Assigning a priority level of 0 to an interrupt source is equivalent to disabling that interrupt.

If the NSTDIS bit (INTCON1<15>) is set, nesting of interrupts is prevented. Thus, if an interrupt is currently being serviced, processing of a new interrupt is prevented, even if the new interrupt is of higher priority than the one currently being serviced.

> **Note:** The IPL bits become read-only whenever the NSTDIS bit has been set to '1'.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the peripheral module which generates the interrupt.

The `DISI` instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instructions, during which the DISI bit (INTCON2<14>) remains set.

When an interrupt is serviced, the PC is loaded with the address stored in the vector location in program memory that corresponds to the interrupt. There are 63 different vectors within the IVT (refer to Figure 5-2). These vectors are contained in locations 0x000004 through 0x0000FE of program memory (refer to Figure 5-2). These locations contain 24-bit addresses, and in order to preserve robustness, an address error trap will take place should the PC attempt to fetch any of these words during normal execution. This prevents execution of random data as a result of accidentally decrementing a PC into vector space, accidentally mapping a data space address into vector space or the PC rolling over to 0x000000 after reaching the end of implemented program memory space. Execution of a `GOTO` instruction to this vector space will also generate an address error trap.

5.2 Reset Sequence

A Reset is not a true exception, because the interrupt controller is not involved in the Reset process. The processor initializes its registers in response to a Reset, which forces the PC to zero. The processor then begins program execution at location 0x000000. A `GOTO` instruction is stored in the first program memory location, immediately followed by the address target for the `GOTO` instruction. The processor executes the `GOTO` to the specified address and then begins operation at the specified target (start) address.

5.2.1 RESET SOURCES

There are 6 sources of error which will cause a device reset.

- Watchdog Time-out:
  The watchdog has timed out, indicating that the processor is no longer executing the correct flow of code.
- Uninitialized W Register Trap:
  An attempt to use an uninitialized W register as an Address Pointer will cause a Reset.
- Illegal Instruction Trap:
  Attempted execution of any unused opcodes will result in an illegal instruction trap. Note that a fetch of an illegal instruction does not result in an illegal instruction trap if that instruction is flushed prior to execution due to a flow change.
- Brown-out Reset (BOR):
  A momentary dip in the power supply to the device has been detected, which may result in malfunction.
- Trap Lockout:
  Occurrence of multiple trap conditions simultaneously will cause a Reset.

5.3 Traps

Traps can be considered as non-maskable interrupts, indicating a software or hardware error, which adhere to a predefined priority as shown in Figure 5-1. They are intended to provide the user a means to correct erroneous operation during debug and when operating within the application.

Note:	If the user does not intend to take corrective action in the event of a trap error condition, these vectors must be loaded with the address of a default handler that simply contains the `RESET` instruction. If, on the other hand, one of the vectors containing an invalid address is called, an address error trap is generated.

Note that many of these trap conditions can only be detected when they occur. Consequently, the questionable instruction is allowed to complete prior to trap exception processing. If the user chooses to recover from the error, the result of the erroneous action that caused the trap may have to be corrected.

There are 8 fixed priority levels for traps: Level 8 through Level 15, which implies that the IPL3 is always set during processing of a trap.

If the user is not currently executing a trap, and he sets the IPL<3:0> bits to a value of ‘`0111`’ (Level 7), then all interrupts are disabled, but traps can still be processed.

5.3.1 TRAP SOURCES

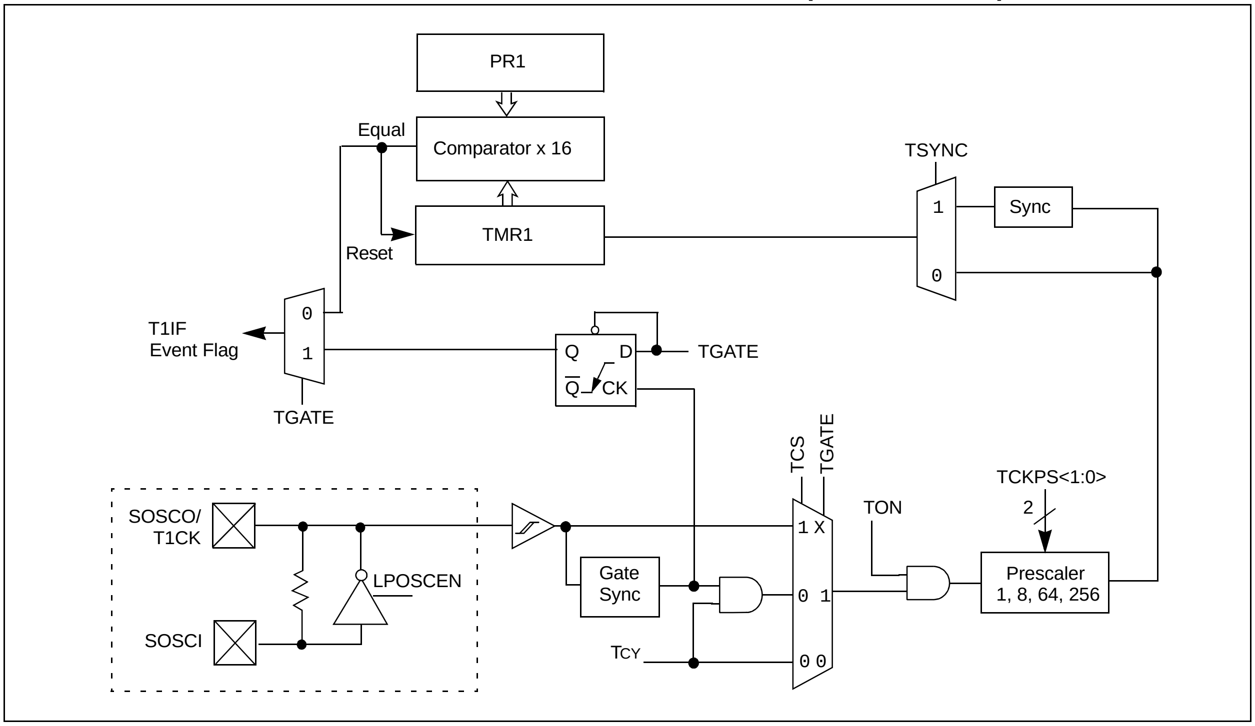
The following traps are provided with increasing priority. However, since all traps can be nested, priority has little effect.

Math Error Trap:

The math error trap executes under the following four circumstances:

1. Should an attempt be made to divide by zero, the divide operation will be aborted on a cycle boundary and the trap taken.
2. If enabled, a math error trap will be taken when an arithmetic operation on either accumulator A or B causes an overflow from bit 31 and the accumulator guard bits are not utilized.
3. If enabled, a math error trap will be taken when an arithmetic operation on either accumulator A or B causes a catastrophic overflow from bit 39 and all saturation is disabled.
4. If the shift amount specified in a shift instruction is greater than the maximum allowed shift amount, a trap will occur.

FIGURE 9-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM (TYPE A TIMER)



9.1 Timer Gate Operation

The 16-bit timer can be placed in the Gated Time Accumulation mode. This mode allows the internal TCY to increment the respective timer when the gate input signal (T1CK pin) is asserted high. Control bit, TGATE (T1CON<6>), must be set to enable this mode. The timer must be enabled (TON = 1) and the timer clock source set to internal (TCS = 0).

When the CPU goes into the Idle mode, the timer will stop incrementing unless TSIDL = 0. If TSIDL = 1, the timer will resume the incrementing sequence upon termination of the CPU Idle mode.

9.2 Timer Prescaler

The input clock (FOSC/4 or external clock) to the 16-bit Timer has a prescale option of 1:1, 1:8, 1:64 and 1:256, selected by control bits, TCKPS<1:0> (T1CON<5:4>). The prescaler counter is cleared when any of the following occurs:

- A write to the TMR1 register
- Clearing of the TON bit (T1CON<15>)
- A device Reset such as a POR and BOR

However, if the timer is disabled (TON = 0), then the timer prescaler cannot be reset since the prescaler clock is halted.

The TMR1 register is not cleared when the T1CON register is written. It is cleared by writing to the TMR1 register.

9.3 Timer Operation During Sleep Mode

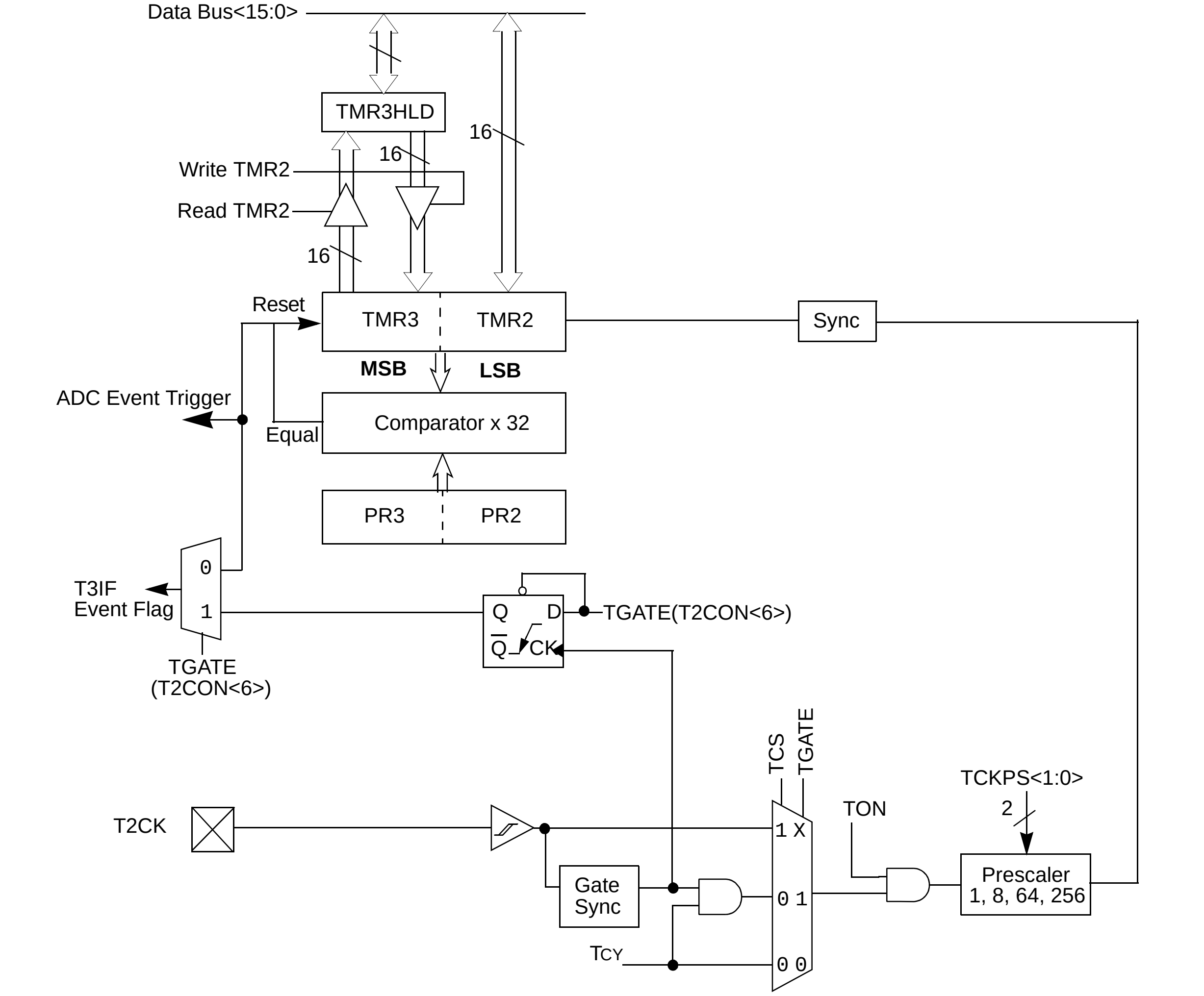
During CPU Sleep mode, the timer will operate if:

- The timer module is enabled (TON = 1) and
- The timer clock source is selected as external (TCS = 1) and
- The TSYNC bit (T1CON<2>) is asserted to a logic ‘0’, which defines the external clock source as asynchronous

When all three conditions are true, the timer will continue to count up to the Period register and be reset to 0x0000.

When a match between the timer and the Period register occurs, an interrupt can be generated, if the respective timer interrupt enable bit is asserted.

FIGURE 10-1: 32-BIT TIMER2/3 BLOCK DIAGRAM



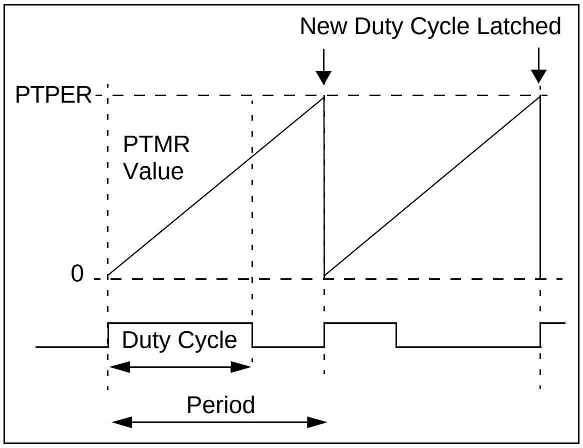
Note: Timer Configuration bit, T32 T2CON(<3>), must be set to ‘1’ for a 32-bit timer/counter operation. All control bits are respective to the T2CON register.

15.3 Edge-Aligned PWM

Edge-aligned PWM signals are produced by the module when the PWM time base is in the Free-Running or Single-Shot mode. For edge-aligned PWM outputs, the output has a period specified by the value in PTPER and a duty cycle specified by the appropriate Duty Cycle register, as shown in Figure 15-2. The PWM output is driven active at the beginning of the period (PTMR = 0) and is driven inactive when the value in the Duty Cycle register matches PTMR.

If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is greater than the value held in the PTPER register.

FIGURE 15-2: EDGE-ALIGNED PWM



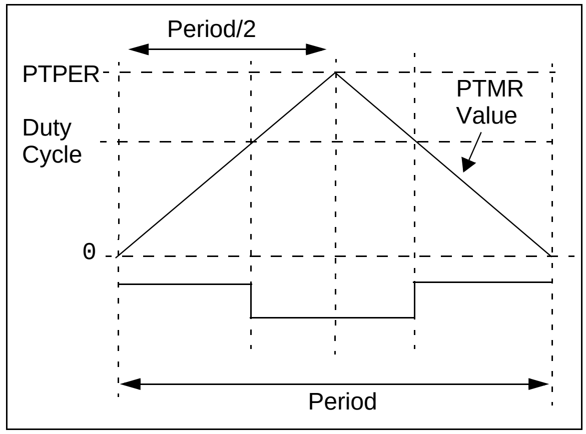
15.4 Center-Aligned PWM

Center-aligned PWM signals are produced by the module when the PWM time base is configured in a Continuous Up/Down Count mode, as shown in Figure 15-3.

The PWM compare output is driven to the active state when the value of the Duty Cycle register matches the value of PTMR and the PWM time base is counting downwards (PTDIR = 1). The PWM compare output is driven to the inactive state when the PWM time base is counting upwards (PTDIR = 0) and the value in the PTMR register matches the duty cycle value.

If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is equal to the value held in the PTPER register.

FIGURE 15-3: CENTER-ALIGNED PWM



15.5 PWM Duty Cycle Comparison Units

There are three 16-bit Special Function Registers (PDC1, PDC2 and PDC3) used to specify duty cycle values for the PWM module.

The value in each Duty Cycle register determines the amount of time that the PWM output is in the active state. The Duty Cycle registers are 16 bits wide. The LSb of a Duty Cycle register determines whether the PWM edge occurs in the beginning. Thus, the PWM resolution is effectively doubled.

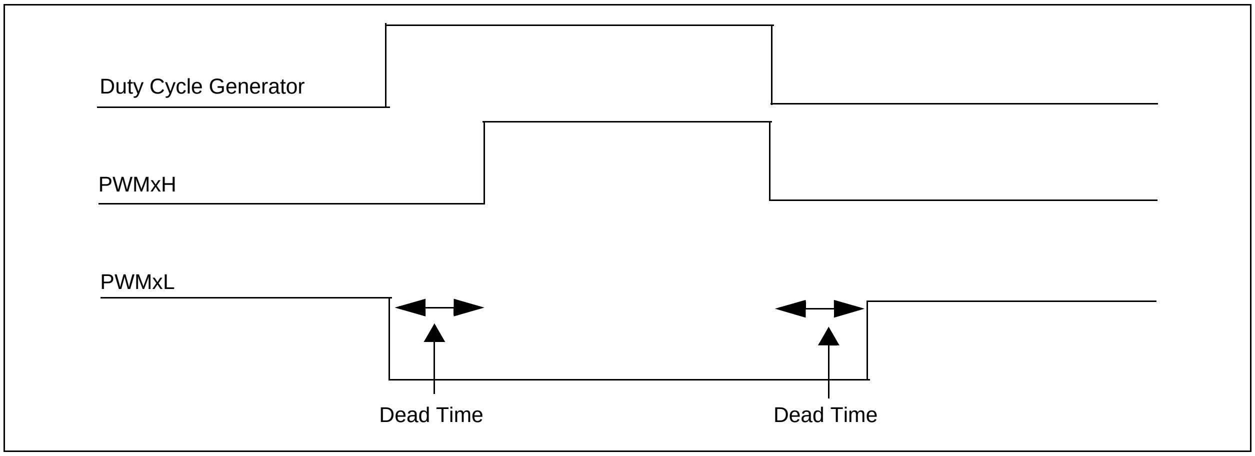
15.5.1 DUTY CYCLE REGISTER BUFFERS

The three PWM Duty Cycle registers are double-buffered to allow glitchless updates of the PWM outputs. For each duty cycle, there is a Duty Cycle register that is accessible by the user and a second Duty Cycle register that holds the actual compare value used in the present PWM period.

For edge-aligned PWM output, a new duty cycle value will be updated whenever a match with the PTPER register occurs and PTMR is reset. The contents of the duty cycle buffers are automatically loaded into the Duty Cycle registers when the PWM time base is disabled (PTEN = 0) and the UDIS bit is cleared in PWMCON2.

When the PWM time base is in the Continuous Up/Down Count mode, new duty cycle values are updated when the value of the PTMR register is zero and the PWM time base begins to count upwards. The contents of the duty cycle buffers are automatically loaded into the Duty Cycle registers when the PWM time base is disabled (PTEN = 0).

FIGURE 15-4: DEAD-TIME TIMING DIAGRAM



15.8 Independent PWM Output

An Independent PWM Output mode is required for driving certain types of loads. A particular PWM output pair is in the Independent Output mode when the corresponding PMOD bit in the PWMCON1 register is set. No dead-time control is implemented between adjacent PWM I/O pins when the module is operating in the Independent mode and both I/O pins are allowed to be active simultaneously.

In the Independent mode, each duty cycle generator is connected to both of the PWM I/O pins in an output pair. By using the associated Duty Cycle register and the appropriate bits in the OVDCON register, the user may select the following signal output options for each PWM I/O pin operating in the Independent mode:

- I/O pin outputs PWM signal
- I/O pin inactive
- I/O pin active

15.9 Single Pulse PWM Operation

The PWM module produces single pulse outputs when the PTCON control bits, PTMOD<1:0> = `10`. Only edge-aligned outputs may be produced in the Single Pulse mode. In Single Pulse mode, the PWM I/O pin(s) are driven to the active state when the PTEN bit is set. When a match with a Duty Cycle register occurs, the PWM I/O pin is driven to the inactive state. When a match with the PTPER register occurs, the PTMR register is cleared, all active PWM I/O pins are driven to the inactive state, the PTEN bit is cleared and an interrupt is generated.

15.10 PWM Output Override

The PWM output override bits allow the user to manually drive the PWM I/O pins to specified logic states, independent of the duty cycle comparison units.

All control bits associated with the PWM output override function are contained in the OVDCON register. The upper half of the OVDCON register contains six bits, POVDxH<3:1> and POVDxL<3:1>, that determine which PWM I/O pins will be overridden. The lower half of the OVDCON register contains six bits, POUTxH<3:1> and POUTxL<3:1>, that determine the state of the PWM I/O pins when a particular output is overridden via the POVD bits.

15.10.1 COMPLEMENTARY OUTPUT MODE

When a PWMxL pin is driven active via the OVDCON register, the output signal is forced to be the complement of the corresponding PWMxH pin in the pair. Dead-time insertion is still performed when PWM channels are overridden manually.

15.10.2 OVERRIDE SYNCHRONIZATION

If the OSYNC bit in the PWMCON2 register is set, all output overrides performed via the OVDCON register are synchronized to the PWM time base. Synchronous output overrides occur at the following times:

- Edge-Aligned mode, when PTMR is zero.
- Center-Aligned modes, when PTMR is zero and when the value of PTMR matches PTPER.

16.0 SPI MODULE

> **Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

The Serial Peripheral Interface (SPI) module is a synchronous serial interface. It is useful for communicating with other peripheral devices, such as EEPROMs, shift registers, display drivers and A/D converters or other microcontrollers. It is compatible with SPI and SIOP interfaces available on some other microcontrollers.

16.1 Operating Function Description

The SPI module consists of a 16-bit shift register, SPI1SR, used for shifting data in and out, and a buffer register, SPI1BUF. A Control register, SPI1CON, configures the module. Additionally, a status register, SPI1STAT, indicates various status conditions.

The serial interface consists of 4 pins: SDI1 (Serial Data Input), SDO1 (Serial Data Output), SCK1 (Shift Clock Input or Output) and $\overline{\text{SS1}}$ (Active-Low Slave Select).

In Master mode operation, SCK1 is a clock output, but in Slave mode, it is a clock input.

A series of eight (8) or sixteen (16) clock pulses shifts out bits from the SPI1SR to the SDO1 pin and simultaneously shifts in data from the SDI1 pin. An interrupt is generated when the transfer is complete and the corresponding interrupt flag bit (SPI1IF) is set. This interrupt can be disabled through an interrupt enable bit (SPI1IE).

The receive operation is double-buffered. When a complete byte is received, it is transferred from SPI1SR to SPI1BUF.

If the receive buffer is full when new data is being transferred from SPI1SR to SPI1BUF, the module will set the SPIROV bit, indicating an overflow condition. The transfer of the data from SPI1SR to SPI1BUF will not be completed and the new data will be lost. The module will not respond to SCL transitions while SPIROV is '1', effectively disabling the module until SPI1BUF is read by user software.

Transmit writes are also double-buffered. The user writes to SPI1BUF. When the master or slave transfer is completed, the contents of the shift register (SPI1SR) are moved to the receive buffer. If any transmit data has been written to the buffer register, the contents of the transmit buffer are moved to SPI1SR. The received data is thus placed in SPI1BUF and the transmit data in SPI1SR is ready for the next transfer.

> **Note:** Both the transmit buffer (SPI1TXB) and the receive buffer (SPI1RXB) are mapped to the same register address, SPI1BUF.

In Master mode, the clock is generated by prescaling the system clock. Data is transmitted as soon as a value is written to SPI1BUF. The interrupt is generated at the middle of the transfer of the last bit.

In Slave mode, data is transmitted and received as external clock pulses appear on SCKx. Again, the interrupt is generated when the last bit is latched. If $\overline{\text{SSx}}$ control is enabled, then transmission and reception are enabled only when $\overline{\text{SSx}}$ = low. The SDOx output will be disabled in $\overline{\text{SSx}}$ mode with $\overline{\text{SSx}}$ high.

The clock provided to the module is (FOSC/4). This clock is then prescaled by the primary (PPRE<1:0>) and the secondary (SPRE<2:0>) prescale factors. The CKE bit determines whether transmit occurs on transition from active clock state to Idle clock state, or vice versa. The CKP bit selects the Idle state (high or low) for the clock.

16.1.1 WORD AND BYTE COMMUNICATION

A control bit, MODE16 (SPI1CON<10>), allows the module to communicate in either 16-bit or 8-bit mode. 16-bit operation is identical to 8-bit operation, except that the number of bits transmitted is 16 instead of 8.

The user software must disable the module prior to changing the MODE16 bit. The SPI module is reset when the MODE16 bit is changed by the user.

A basic difference between 8-bit and 16-bit operation is that the data is transmitted out of bit 7 of the SPIxSR for 8-bit operation, and data is transmitted out of bit 15 of the SPIxSR for 16-bit operation. In both modes, data is shifted into bit 0 of the SPIxSR.

16.1.2 SDO1 DISABLE

A control bit, DISSDO, is provided to the SPI1CON register to allow the SDO1 output to be disabled. This will allow the SPI module to be connected in an input only configuration. SDOx can also be used for general purpose I/O.

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) MODULE

Note:	This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

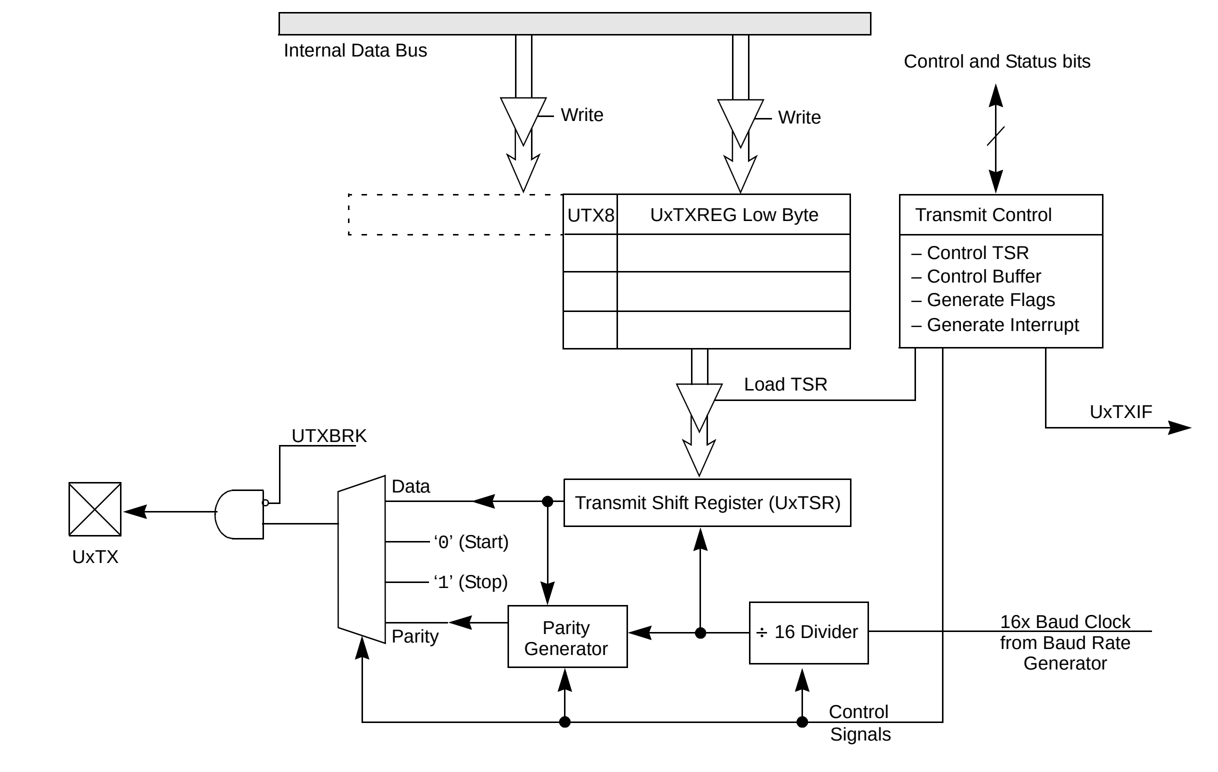
This section describes the Universal Asynchronous Receiver/Transmitter Communications module.

18.1 UART Module Overview

The key features of the UART module are:

- Full-duplex, 8 or 9-bit data communication
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Fully integrated Baud Rate Generator with 16-bit prescaler
- Baud rates range from 38 bps to 1.875 Mbps at a 30 MHz instruction rate
- 4-word deep transmit data buffer
- 4-word deep receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support

FIGURE 18-1: UART TRANSMITTER BLOCK DIAGRAM



Note: x = 1 or 2
dsPIC30F3010 only has UART1.

18.9 Auto Baud Support

To allow the system to determine baud rates of received characters, the input can be optionally linked to a selected capture input. To enable this mode, the user must program the input capture module to detect the falling and rising edges of the Start bit.

18.10 UART Operation During CPU Sleep and Idle Modes

18.10.1 UART OPERATION DURING CPU SLEEP MODE

When the device enters Sleep mode, all clock sources to the module are shut down and stay at logic '0'. If entry into Sleep mode occurs while a transmission is in progress, then the transmission is aborted. The UxTX pin is driven to logic '1'. Similarly, if entry into Sleep mode occurs while a reception is in progress, then the reception is aborted. The UxSTA, UxMODE, Transmit and Receive registers and buffers, and the UxBRG register are not affected by Sleep mode.

If the WAKE bit (UxMODE<7>) is set before the device enters Sleep mode, then a falling edge on the UxRX pin will generate a receive interrupt. The Receive Interrupt Select Mode bit (URXISEL) has no effect for this function. If the receive interrupt is enabled, then this will wake-up the device from Sleep. The UARTEN bit must be set in order to generate a wake-up interrupt.

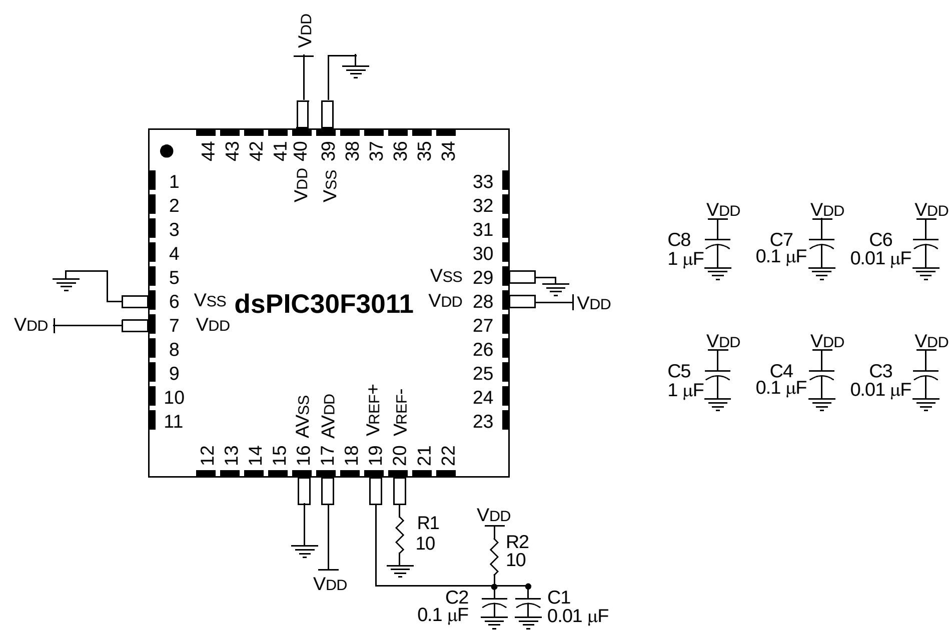
18.10.2 UART OPERATION DURING CPU IDLE MODE

For the UART, the USIDL bit selects if the module will stop operation when the device enters Idle mode, or whether the module will continue on Idle. If USIDL = 0, the module will continue operation during Idle mode. If USIDL = 1, the module will stop on Idle.

The configuration guidelines give the required setup values for the conversion speeds above 500 ksps, since they require external VREF pins usage and there are some differences in the configuration procedure. Configuration details that are not critical to the conversion speed have been omitted.

Figure 19-2 depicts the recommended circuit for the conversion rates above 500 ksps.

FIGURE 19-2: ADC VOLTAGE REFERENCE SCHEMATIC



19.7.1 1 Msps CONFIGURATION GUIDELINE

The configuration for 1 Msps operation is dependent on whether a single input pin is to be sampled or whether multiple pins will be sampled.

19.7.1.1 Single Analog Input

For conversions at 1 Msps for a single analog input, at least two sample and hold channels must be enabled. The analog input multiplexer must be configured so that the same input pin is connected to both sample and hold channels. The ADC converts the value held on one S/H channel, while the second S/H channel acquires a new input sample.

19.7.1.2 Multiple Analog Inputs

The ADC can also be used to sample multiple analog inputs using multiple sample and hold channels. In this case, the total 1 Msps conversion rate is divided among the different input signals. For example, four inputs can be sampled at a rate of 250 ksps for each signal or two inputs could be sampled at a rate of 500 ksps for each signal. Sequential sampling must be used in this configuration to allow adequate sampling time on each input.

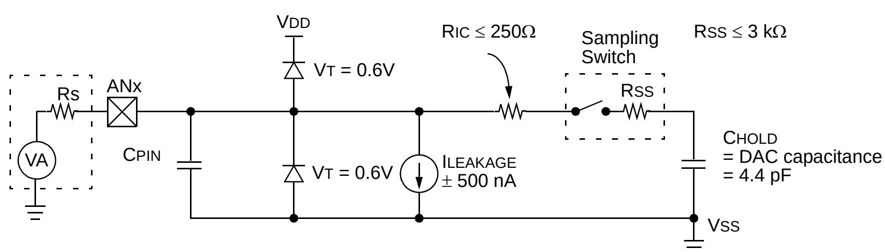
19.8 A/D Acquisition Requirements

The analog input model of the 10-bit ADC is shown in Figure 19-3. The total sampling time for the ADC is a function of the internal amplifier settling time, device V_{DD} and the holding capacitor charge time.

For the ADC to meet its specified accuracy, the Charge Holding Capacitor (C_{HOLD}) must be allowed to fully charge to the voltage level on the analog input pin. The Source Impedance (R_S), the Interconnect Impedance (R_{IC}) and the Internal Sampling Switch (R_{SS}) Impedance combine to directly affect the time required to charge the capacitor, C_{HOLD}. The combined impedance of the analog sources must therefore be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the A/D converter, the maximum recommended source impedance, R_S, is 5 kΩ. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

The user must allow at least 1 T_{AD} period of sampling time, T_{SAMP}, between conversions to allow each sample to be acquired. This sample time may be controlled manually in software by setting/clearing the SAMP bit, or it may be automatically controlled by the ADC. In an automatic configuration, the user must allow enough time between conversion triggers so that the minimum sample time can be satisfied. Refer to the **Section 23.0 "Electrical Characteristics"** for T_{AD} and sample time requirements.

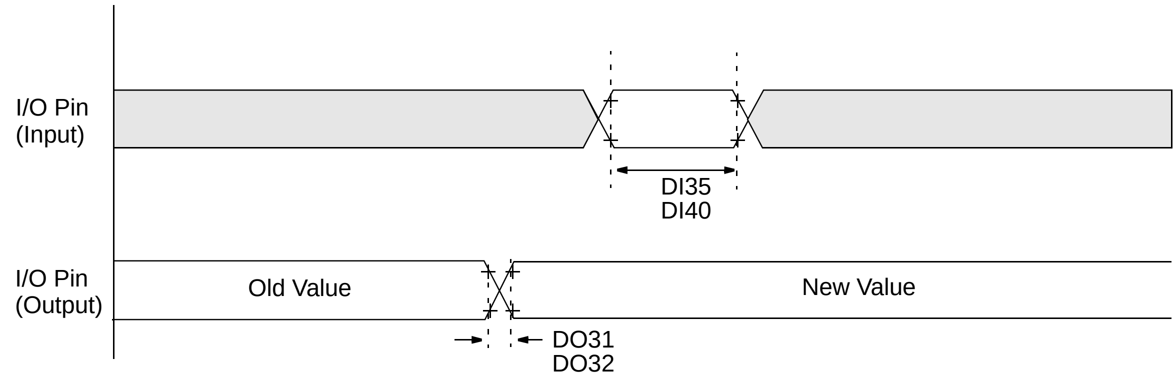
FIGURE 19-3: ADC ANALOG INPUT MODEL



Legend:		
	C_{PIN}	= Input Capacitance
	V_T	= Threshold Voltage
	$I_{LEAKAGE}$	= Leakage Current at the pin due to various junctions
	R_{IC}	= Interconnect Resistance
	R_{SS}	= Sampling Switch Resistance
	C_{HOLD}	= Sample/Hold Capacitance (from DAC)

Note: C_{PIN} value depends on device package and is not tested. Effect of C_{PIN} negligible if Rs ≤ 5 kΩ.

FIGURE 23-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 23-2 for load conditions.

TABLE 23-19: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1,2,3)**	**Min**	**Typ(4)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	7	20	ns	
DO32	TIOF	Port Output Fall Time	—	7	20	ns	
DI35	TINP	INTx Pin High or Low Time (output)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2 TCY	—	—	ns	

Note 1: These parameters are asynchronous events not related to any internal clock edges.
2: Measurements are taken in RC mode and EC mode where CLKO output is 4 x TOSC.
3: These parameters are characterized but not tested in manufacturing.
4: Data in “Typ” column is at 5V, 25°C unless otherwise stated.

FIGURE 23-14: QEA/QEB INPUT CHARACTERISTICS

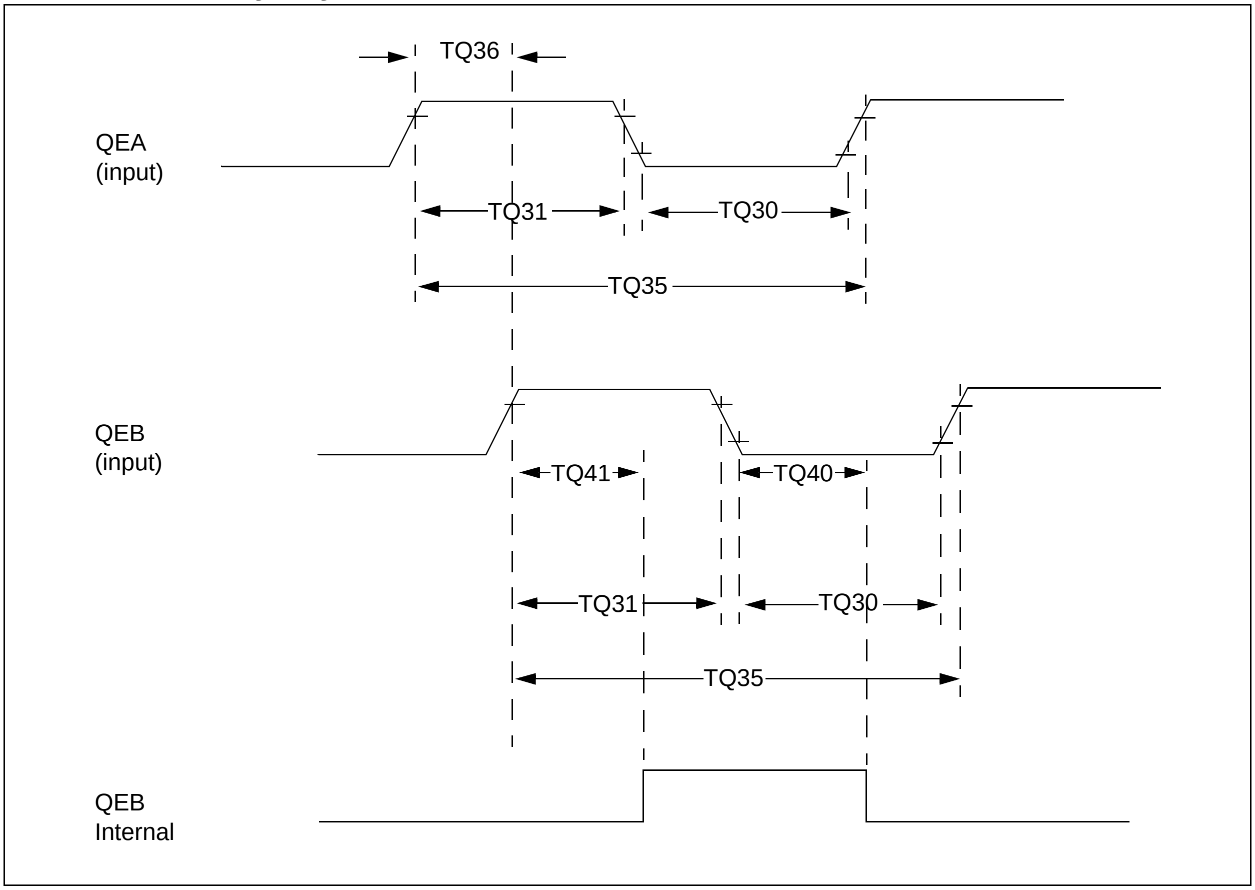


TABLE 23-30: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(1)**	**Typ(2)**	**Max**	**Units**	**Conditions**
TQ30	TQUL	Quadrature Input Low Time	6 TCY	—	ns	
TQ31	TQUH	Quadrature Input High Time	6 TCY	—	ns	
TQ35	TQUIN	Quadrature Input Period	12 TCY	—	ns	
TQ36	TQUP	Quadrature Phase Period	3 TCY	—	ns	
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**

Note 1: These parameters are characterized but not tested in manufacturing.
2: N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 16. “Quadrature Encoder Interface (QEI)”** in the”*dsPIC30F Family Reference Manual*” (DS70046).

TABLE 23-35: SPI MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**	**Min**	**Typ[2]**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time[3]	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time[3]	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time[3]	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time[3]	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}}$↓ to SCKx↓ or SCKx↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SSx}}$↑ to SDOx Output High-Impedance[4]	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{\text{SSx}}$↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid after $\overline{\text{SSx}}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.