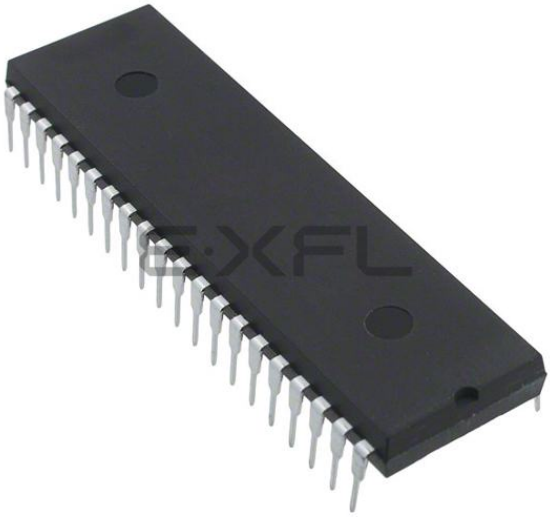

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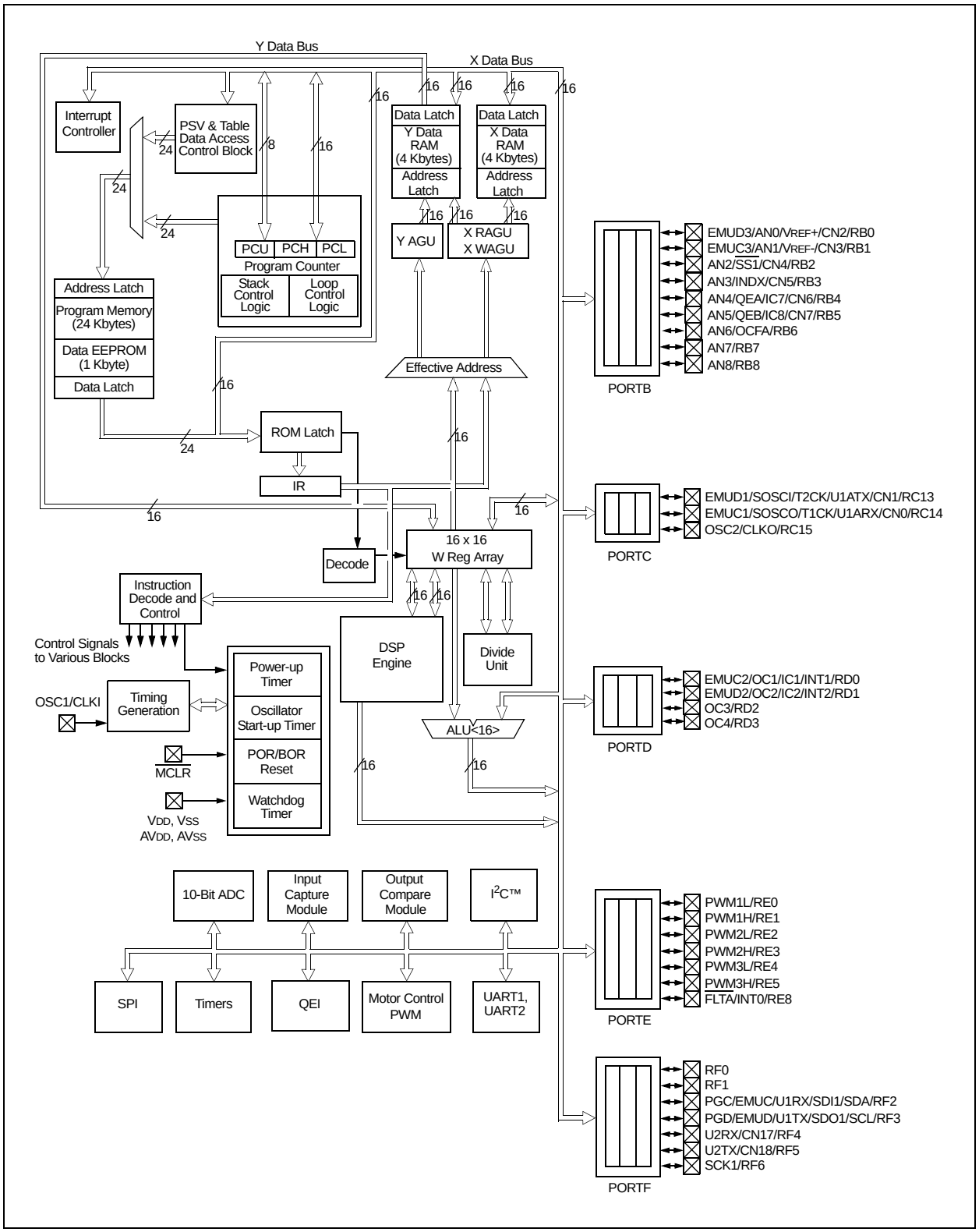
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 20 MIPS |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 24KB (8K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3011-20e-p |

**NOTES:**

**FIGURE 1-1: dsPIC30F3011 BLOCK DIAGRAM**



**NOTES:**

### 3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see **Section 3.1.2 "Data Access From Program Memory Using Program Space Visibility"**). The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lsw of any address within program space, without going through data space. The TBLRDH and TBLWTH instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

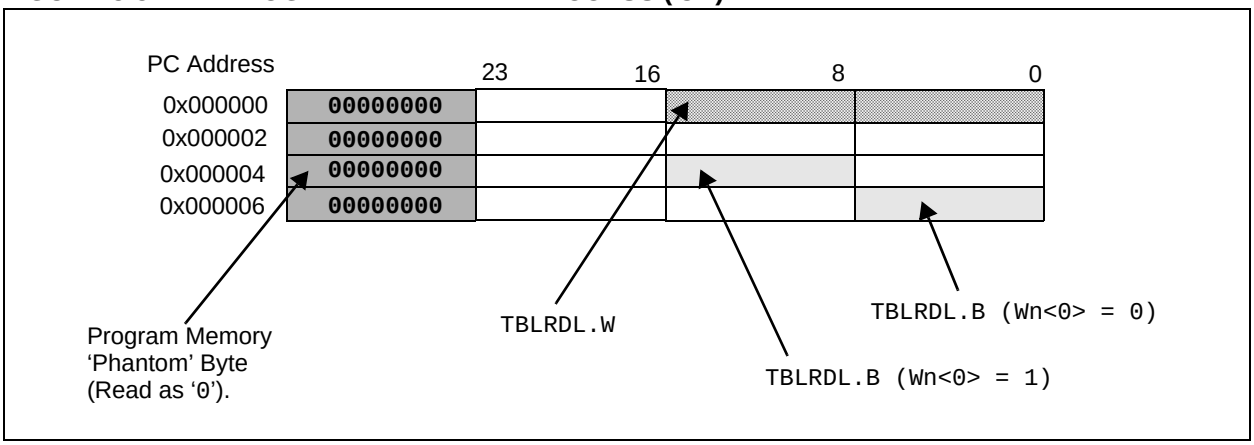
The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the lsw, and TBLRDH and TBLWTH access the space which contains the MSB.

Figure 3-2 illustrates how the EA is created for table operations and data space accesses (PSV = 1). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space.

1. **TBLRDL:** Table Read Low
   *Word:* Read the lsw of the program address;
   P<15:0> maps to D<15:0>.
   *Byte:* Read one of the LSBs of the program address;
   P<7:0> maps to the destination byte when byte select = 0;
   P<15:8> maps to the destination byte when byte select = 1.
2. **TBLWTL:** Table Write Low (refer to **Section 6.0 "Flash Program Memory"** for details on Flash programming).
3. **TBLRDH:** Table Read High
   *Word:* Read the msw of the program address;
   P<23:16> maps to D<7:0>; D<15:8> will always be = 0.
   *Byte:* Read one of the MSBs of the program address;
   P<23:16> maps to the destination byte when byte select = 0;
   The destination byte will always be = 0 when byte select = 1.
4. **TBLWTH:** Table Write High (refer to **Section 6.0 "Flash Program Memory"** for details on Flash programming).

**FIGURE 3-3: PROGRAM DATA TABLE ACCESS (lsw)**



## 6.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*16-bit MCU and DSC Programmer's Reference Manual*" (DS70157).

The dsPIC30F family of devices contains internal program Flash memory for executing user code. There are two methods by which the user can program this memory:

1. In-Circuit Serial Programming™ (ICSP™) capabilities
2. Run-Time Self-Programming (RTSP)

### 6.1 In-Circuit Serial Programming (ICSP)

dsPIC30F devices can be serially programmed while in the end application circuit. This is simply done with two lines for Programming Clock and Programming Data (which are named PGC and PGD, respectively), and three other lines for Power ($V_{DD}$), Ground ($V_{SS}$) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

### 6.2 Run-Time Self-Programming (RTSP)

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions.

With RTSP, the user may erase program memory, 32 instructions (96 bytes) at a time and can write program memory data, 32 instructions (96 bytes) at a time.

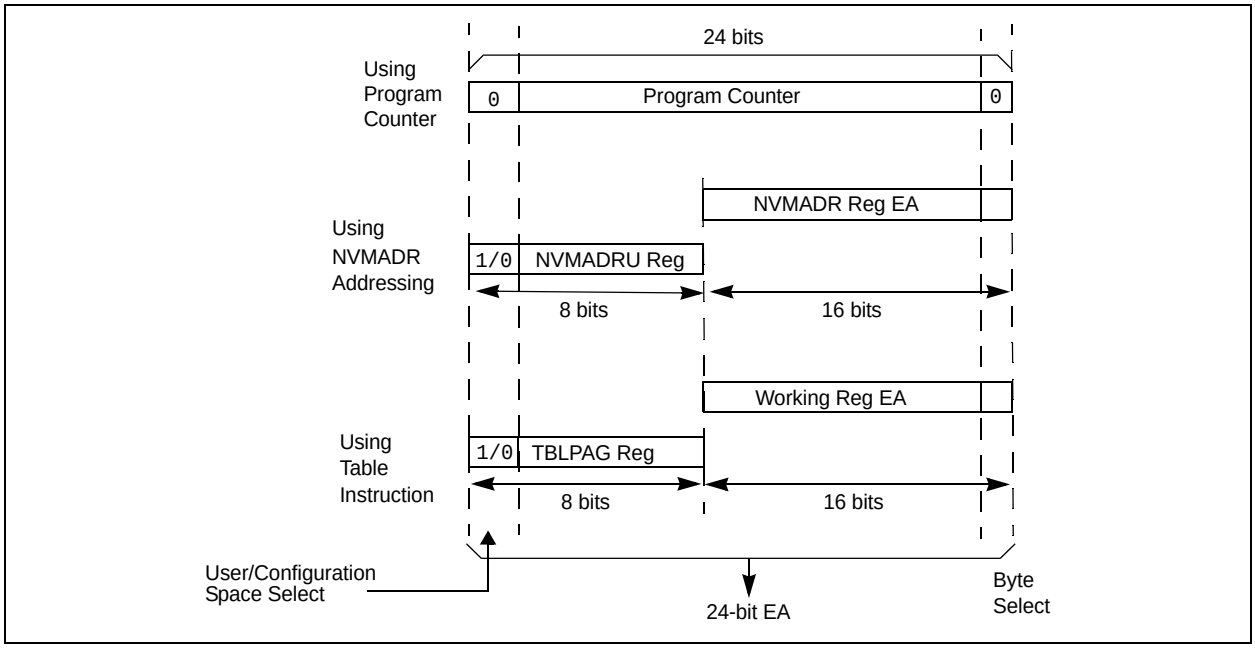
### 6.3 Table Instruction Operation Summary

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in Word or Byte mode.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can access program memory in Word or Byte mode.

A 24-bit program memory address is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 6-1.

**FIGURE 6-1: ADDRESSING FOR TABLE AND NVM REGISTERS**



## 8.0 I/O PORTS

| | |
|---|---|
| **Note:** | This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). |

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSC1/CLKI) are shared between the peripherals and the parallel I/O ports.

All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 8.1 Parallel I/O (PIO) Ports

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with the operation of the port pin. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch (LATx). Reads from the port (PORTx), read the port pins, and writes to the port pins, write the latch (LATx).

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs. An example is the INT4 pin.

The format of the registers for PORTx is shown in Table 8-1.

The TRISx register controls the direction of the pins. The LATx register supplies data to the outputs and is readable/writable. Reading the PORTx register yields the state of the input pins, while writing the PORTx register modifies the contents of the LATx register.

A Parallel I/O (PIO) port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pad cell. Figure 8-2 illustrates how ports are shared with other peripherals, and the associated I/O cell (pad) to which they are connected. Table 8-1 shows the formats of the registers for the shared ports, PORTB through PORTF.

**FIGURE 8-1: BLOCK DIAGRAM OF A DEDICATED PORT STRUCTURE**

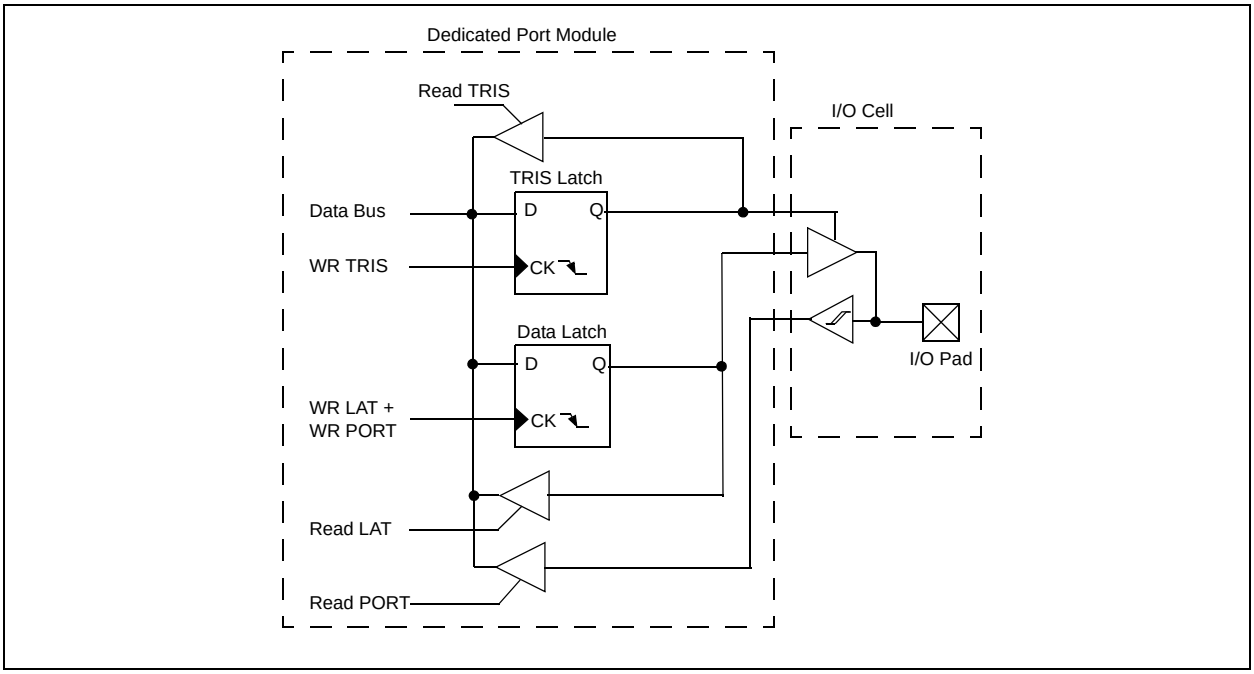
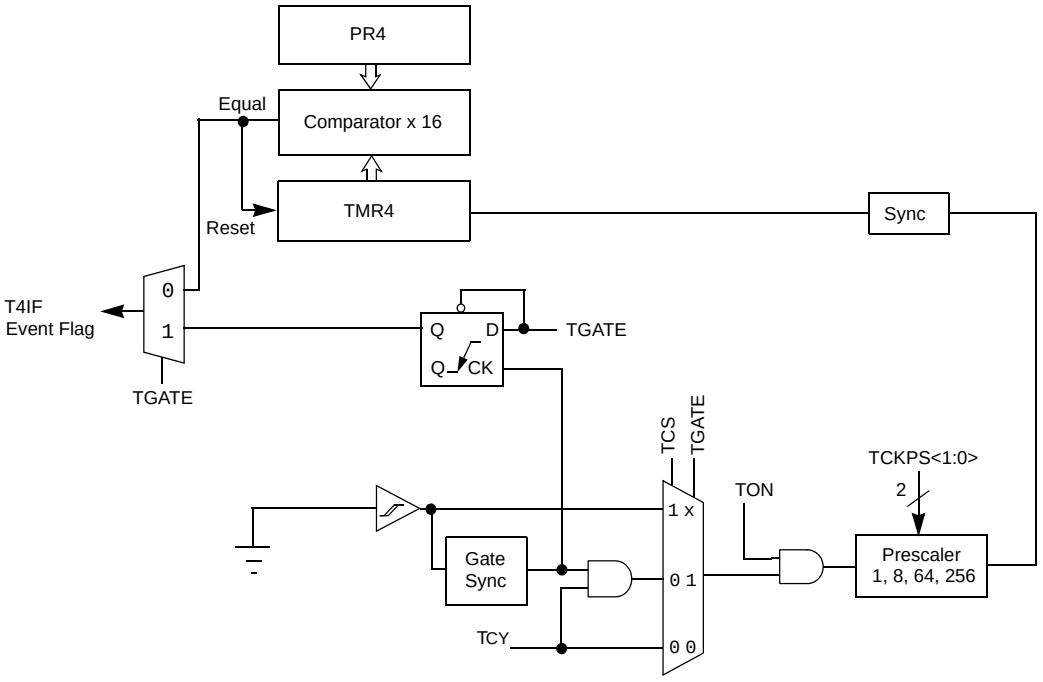


**FIGURE 11-2: 16-BIT TIMER4 BLOCK DIAGRAM (TYPE B TIMER)**




**Note:** The dsPIC30F3010/3011 devices do not have external pin inputs to Timer4 or Timer5. In these devices, the following modes should not be used:
1. TCS = 1
2. TCS = 0 and TGATE = 1 (Gated Time Accumulation)

**NOTES:**

## 15.1 PWM Time Base

The PWM time base is provided by a 15-bit timer with a prescaler and postscaler. The time base is accessible via the PTMR SFR. The PTDIR bit (PTMR<15>) is a read-only status bit that indicates the present count direction of the PWM time base. If the PTDIR bit is cleared, PTMR is counting upward. If the PTDIR bit is set, PTMR is counting downward. The PWM time base is configured via the PTCON SFR. The time base is enabled/disabled by setting/clearing the PTEN bit in the PTCON SFR. PTMR is not cleared when the PTEN bit is cleared in software.

The PTPER SFR sets the counting period for PTMR. The user must write a 15-bit value to PTPER<14:0>. When the value in PTMR<14:0> matches the value in PTPER<14:0>, the time base will either reset to 0, or reverse the count direction on the next occurring clock cycle. The action taken depends on the operating mode of the time base.

| | |
|---|---|
| **Note:** | If the Period register is set to 0x0000, the timer will stop counting, and the interrupt and the Special Event Trigger will not be generated, even if the special event value is also 0x0000. The module will not update the Period register if it is already at 0x0000; therefore, the user must disable the module in order to update the Period register. |

The PWM time base can be configured for four different modes of operation:

- Free-Running mode
- Single-Shot mode
- Continuous Up/Down Count mode
- Continuous Up/Down Count mode with interrupts for double updates

These four modes are selected by the PTMOD<1:0> bits in the PTCON SFR. The Continuous Up/Down Count modes support center-aligned PWM generation. The Single-Shot mode allows the PWM module to support pulse control of certain Electronically Commutative Motors (ECMs).

The interrupt signals generated by the PWM time base depend on the mode selection bits (PTMOD<1:0>) and the postscaler bits (PTOPS<3:0>) in the PTCON SFR.

### 15.1.1 FREE-RUNNING MODE

In the Free-Running mode, the PWM time base counts upwards until the value in the Time Base Period register (PTPER) is matched. The PTMR register is reset on the following input clock edge and the time base will continue to count upwards as long as the PTEN bit remains set.

When the PWM time base is in the Free-Running mode (PTMOD<1:0> = 00), an interrupt event is generated each time a match with the PTPER register occurs and the PTMR register is reset to zero. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

### 15.1.2 SINGLE-SHOT MODE

In the Single-Shot mode, the PWM time base begins counting upwards when the PTEN bit is set. When the value in the PTMR register matches the PTPER register, the PTMR register will be reset on the following input clock edge and the PTEN bit will be cleared by the hardware to halt the time base.

When the PWM time base is in the Single-Shot mode (PTMOD<1:0> = 01), an interrupt event is generated when a match with the PTPER register occurs, the PTMR register is reset to zero on the following input clock edge, and the PTEN bit is cleared. The postscaler selection bits have no effect in this mode of the timer**.**

### 15.1.3 CONTINUOUS UP/DOWN COUNT MODES

In the Continuous Up/Down Count modes, the PWM time base counts upwards until the value in the PTPER register is matched. The timer will begin counting downwards on the following input clock edge. The PTDIR bit in the PTCON SFR is read-only and indicates the counting direction. The PTDIR bit is set when the timer counts downwards.

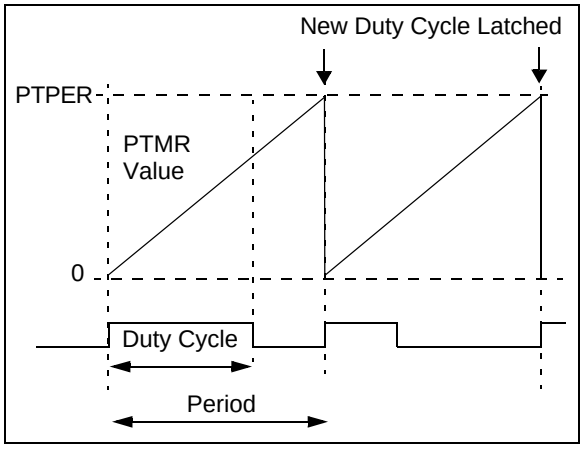
In the Continuous Up/Down Count mode (PTMOD<1:0> = 10), an interrupt event is generated each time the value of the PTMR register becomes zero and the PWM time base begins to count upwards. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

## 15.3 Edge-Aligned PWM

Edge-aligned PWM signals are produced by the module when the PWM time base is in the Free-Running or Single-Shot mode. For edge-aligned PWM outputs, the output has a period specified by the value in PTPER and a duty cycle specified by the appropriate Duty Cycle register, as shown in Figure 15-2. The PWM output is driven active at the beginning of the period (PTMR = 0) and is driven inactive when the value in the Duty Cycle register matches PTMR.

If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is greater than the value held in the PTPER register.

**FIGURE 15-2: EDGE-ALIGNED PWM**



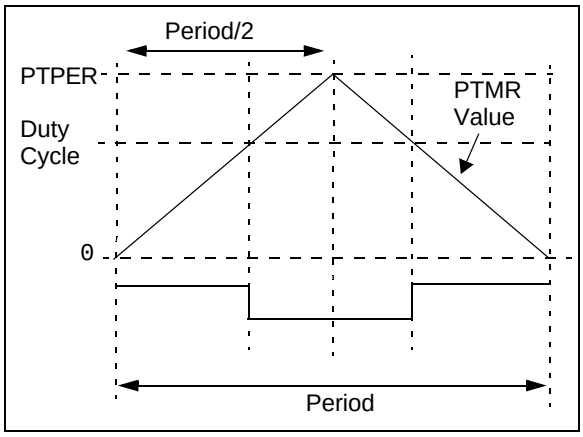

## 15.4 Center-Aligned PWM

Center-aligned PWM signals are produced by the module when the PWM time base is configured in a Continuous Up/Down Count mode, as shown in Figure 15-3.

The PWM compare output is driven to the active state when the value of the Duty Cycle register matches the value of PTMR and the PWM time base is counting downwards (PTDIR = 1). The PWM compare output is driven to the inactive state when the PWM time base is counting upwards (PTDIR = 0) and the value in the PTMR register matches the duty cycle value.

If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is equal to the value held in the PTPER register.

**FIGURE 15-3: CENTER-ALIGNED PWM**




## 15.5 PWM Duty Cycle Comparison Units

There are three 16-bit Special Function Registers (PDC1, PDC2 and PDC3) used to specify duty cycle values for the PWM module.

The value in each Duty Cycle register determines the amount of time that the PWM output is in the active state. The Duty Cycle registers are 16 bits wide. The LSb of a Duty Cycle register determines whether the PWM edge occurs in the beginning. Thus, the PWM resolution is effectively doubled.

### 15.5.1 DUTY CYCLE REGISTER BUFFERS

The three PWM Duty Cycle registers are double-buffered to allow glitchless updates of the PWM outputs. For each duty cycle, there is a Duty Cycle register that is accessible by the user and a second Duty Cycle register that holds the actual compare value used in the present PWM period.

For edge-aligned PWM output, a new duty cycle value will be updated whenever a match with the PTPER register occurs and PTMR is reset. The contents of the duty cycle buffers are automatically loaded into the Duty Cycle registers when the PWM time base is disabled (PTEN = 0) and the UDIS bit is cleared in PWMCON2.

When the PWM time base is in the Continuous Up/Down Count mode, new duty cycle values are updated when the value of the PTMR register is zero and the PWM time base begins to count upwards. The contents of the duty cycle buffers are automatically loaded into the Duty Cycle registers when the PWM time base is disabled (PTEN = 0).

## 16.0 SPI MODULE

| | |
|---|---|
| **Note:** | This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). |

The Serial Peripheral Interface (SPI) module is a synchronous serial interface. It is useful for communicating with other peripheral devices, such as EEPROMs, shift registers, display drivers and A/D converters or other microcontrollers. It is compatible with SPI and SIOP interfaces available on some other microcontrollers.

### 16.1 Operating Function Description

The SPI module consists of a 16-bit shift register, SPI1SR, used for shifting data in and out, and a buffer register, SPI1BUF. A Control register, SPI1CON, configures the module. Additionally, a status register, SPI1STAT, indicates various status conditions.

The serial interface consists of 4 pins: SDI1 (Serial Data Input), SDO1 (Serial Data Output), SCK1 (Shift Clock Input or Output) and $\overline{SS1}$ (Active-Low Slave Select).

In Master mode operation, SCK1 is a clock output, but in Slave mode, it is a clock input.

A series of eight (8) or sixteen (16) clock pulses shifts out bits from the SPI1SR to the SDO1 pin and simultaneously shifts in data from the SDI1 pin. An interrupt is generated when the transfer is complete and the corresponding interrupt flag bit (SPI1IF) is set. This interrupt can be disabled through an interrupt enable bit (SPI1IE).

The receive operation is double-buffered. When a complete byte is received, it is transferred from SPI1SR to SPI1BUF.

If the receive buffer is full when new data is being transferred from SPI1SR to SPI1BUF, the module will set the SPIROV bit, indicating an overflow condition. The transfer of the data from SPI1SR to SPI1BUF will not be completed and the new data will be lost. The module will not respond to SCL transitions while SPIROV is '1', effectively disabling the module until SPI1BUF is read by user software.

Transmit writes are also double-buffered. The user writes to SPI1BUF. When the master or slave transfer is completed, the contents of the shift register (SPI1SR) are moved to the receive buffer. If any transmit data has been written to the buffer register, the contents of the transmit buffer are moved to SPI1SR. The received data is thus placed in SPI1BUF and the transmit data in SPI1SR is ready for the next transfer.

| | |
|---|---|
| **Note:** | Both the transmit buffer (SPI1TXB) and the receive buffer (SPI1RXB) are mapped to the same register address, SPI1BUF. |

In Master mode, the clock is generated by prescaling the system clock. Data is transmitted as soon as a value is written to SPI1BUF. The interrupt is generated at the middle of the transfer of the last bit.

In Slave mode, data is transmitted and received as external clock pulses appear on SCKx. Again, the interrupt is generated when the last bit is latched. If $\overline{SSx}$ control is enabled, then transmission and reception are enabled only when $\overline{SSx}$ = low. The SDOx output will be disabled in $\overline{SSx}$ mode with $\overline{SSx}$ high.

The clock provided to the module is (FOSC/4). This clock is then prescaled by the primary (PPRE<1:0>) and the secondary (SPRE<2:0>) prescale factors. The CKE bit determines whether transmit occurs on transition from active clock state to Idle clock state, or vice versa. The CKP bit selects the Idle state (high or low) for the clock.

#### 16.1.1 WORD AND BYTE COMMUNICATION

A control bit, MODE16 (SPI1CON<10>), allows the module to communicate in either 16-bit or 8-bit mode. 16-bit operation is identical to 8-bit operation, except that the number of bits transmitted is 16 instead of 8.

The user software must disable the module prior to changing the MODE16 bit. The SPI module is reset when the MODE16 bit is changed by the user.

A basic difference between 8-bit and 16-bit operation is that the data is transmitted out of bit 7 of the SPIxSR for 8-bit operation, and data is transmitted out of bit 15 of the SPIxSR for 16-bit operation. In both modes, data is shifted into bit 0 of the SPIxSR.

#### 16.1.2 SDO1 DISABLE

A control bit, DISSDO, is provided to the SPI1CON register to allow the SDO1 output to be disabled. This will allow the SPI module to be connected in an input only configuration. SDOx can also be used for general purpose I/O.

**TABLE 17-2: I²C™ REGISTER MAP(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I2CRCV | 0200 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 0000 0000 0000 |
| I2CTRN | 0202 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 0000 1111 1111 |
| I2CBRG | 0204 | — | — | — | — | — | — | — | Baud Rate Generator | | | | | | | | | 0000 0000 0000 0000 |
| I2CCON | 0206 | I2CEN | — | I2CSIDL | SCLREL | IPMIEN | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 0001 0000 0000 0000 |
| I2CSTAT | 0208 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 0000 0000 0000 |
| I2CADD | 020A | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 0000 0000 0000 |

**Legend:** — = unimplemented bit, read as '0'

**Note 1:** Refer to the *"dsPIC30F Family Reference Manual"* (DS70046) for descriptions of register bit fields.

### 18.5.2 FRAMING ERROR (FERR)

The FERR bit (UxSTA<2>) is set if a '0' is detected instead of a Stop bit. If two Stop bits are selected, both Stop bits must be '1'; otherwise, FERR will be set. The read-only FERR bit is buffered along with the received data; it is cleared on any Reset.

### 18.5.3 PARITY ERROR (PERR)

The PERR bit (UxSTA<3>) is set if the parity of the received word is incorrect. This error bit is applicable only if a Parity mode (odd or even) is selected. The read-only PERR bit is buffered along with the received data bytes; it is cleared on any Reset.

### 18.5.4 IDLE STATUS

When the receiver is active (i.e., between the initial detection of the Start bit and the completion of the Stop bit), the RIDLE bit (UxSTA<4>) is '0'. Between the completion of the Stop bit and detection of the next Start bit, the RIDLE bit is '1', indicating that the UART is Idle.

### 18.5.5 RECEIVE BREAK

The receiver will count and expect a certain number of bit times based on the values programmed in the PDSEL (UxMODE<2:1>) and STSEL (UxMODE<0>) bits.

If the break is longer than 13 bit times, the reception is considered complete after the number of bit times specified by PDSEL and STSEL. The URXDA bit is set, FERR is set, zeros are loaded into the receive FIFO, interrupts are generated, if appropriate and the RIDLE bit is set.

When the module receives a long Break signal and the receiver has detected the Start bit, the data bits and the invalid Stop bit (which sets the FERR), the receiver must wait for a valid Stop bit before looking for the next Start bit. It cannot assume that the Break condition on the line is the next Start bit.

Break is regarded as a character containing all 0's, with the FERR bit set. The Break character is loaded into the buffer. No further reception can occur until a Stop bit is received. Note that RIDLE goes high when the Stop bit has not been received yet.

## 18.6 Address Detect Mode

Setting the ADDEN bit (UxSTA<5>) enables the Address Detect mode, in which a 9th bit (URX8) value of '1' identifies the received word as an address rather than data. This mode is only applicable for 9-bit data communication. The URXISEL control bit does not have any impact on interrupt generation in this mode, since an interrupt (if enabled) will be generated every time the received word has the 9th bit set.

## 18.7 Loopback Mode

Setting the LPBACK bit enables this special mode in which the UxTX pin is internally connected to the UxRX pin. When configured for the Loopback mode, the UxRX pin is disconnected from the internal UART receive logic. However, the UxTX pin still functions as in a normal operation.

To select this mode:

a) Configure UART for desired mode of operation.
b) Set LPBACK = 1 to enable Loopback mode.
c) Enable transmission as defined in **Section 18.3 "Transmitting Data"**.

## 18.8 Baud Rate Generator

The UART has a 16-bit Baud Rate Generator to allow maximum flexibility in baud rate generation. The Baud Rate Generator register (UxBRG) is readable and writable. The baud rate is computed as follows:

BRG = 16-bit value held in UxBRG register (0 through 65535)

$F_{CY}$ = Instruction Clock Rate ($1/T_{CY}$)

The baud rate is given by Equation 18-1.

**EQUATION 18-1: BAUD RATE**

$$Baud\ Rate = F_{CY} / (16 * (BRG + 1))$$

Therefore, maximum baud rate possible is

$F_{CY}$ / 16 (if BRG = 0),

and the minimum baud rate possible is

$F_{CY}$ / (16 * 65536).

With a full 16-bit Baud Rate Generator, at 30 MIPs operation, the minimum baud rate achievable is 28.5 bps.

## 19.4 Programming the Start of Conversion Trigger

The conversion trigger will terminate acquisition and start the requested conversions.

The SSRC<2:0> bits select the source of the conversion trigger.

The SSRC bits provide for up to five alternate sources of conversion trigger.

When SSRC<2:0> = 000, the conversion trigger is under software control. Clearing the SAMP bit will cause the conversion trigger.

When SSRC<2:0> = 111 (Auto-Start mode), the conversion trigger is under A/D clock control. The SAMC bits select the number of A/D clocks between the start of acquisition and the start of conversion. This provides the fastest conversion rates on multiple channels. The SAMC bits must always be at least one clock cycle.

Other trigger sources can come from timer modules, motor control PWM module or external interrupts.

**Note:** To operate the A/D at the maximum specified conversion speed, the auto-convert trigger option should be selected (SSRC = 111) and the auto-sample time bits should be set to 1 TAD (SAMC = 00001). This configuration will give a total conversion period (sample + convert) of 13 TAD.

The use of any other conversion trigger will result in additional TAD cycles to synchronize the external event to the A/D.

## 19.5 Aborting a Conversion

Clearing the ADON bit during a conversion will abort the current conversion and stop the sampling sequencing. The ADCBUF will not be updated with the partially completed A/D conversion sample. That is, the ADCBUF will continue to contain the value of the last completed conversion (or the last value written to the ADCBUF register).

If the clearing of the ADON bit coincides with an auto-start, the clearing has a higher priority.

After the A/D conversion is aborted, a 2 TAD wait is required before the next sampling may be started by setting the SAMP bit.

If sequential sampling is specified, the A/D will continue at the next sample pulse which corresponds with the next channel converted. If simultaneous sampling is specified, the A/D will continue with the next multi-channel group conversion sequence.

## 19.6 Selecting the A/D Conversion Clock

The A/D conversion requires 12 TAD. The source of the A/D conversion clock is software selected using a 6-bit counter. There are 64 possible options for TAD.

**EQUATION 19-1: A/D CONVERSION CLOCK**

$$TAD = TCY \bullet (0.5 \bullet (ADCS<5:0> + 1))$$

$$ADCS<5:0> = 2 \frac{TAD}{TCY} - 1$$

The internal RC oscillator is selected by setting the ADRC bit.

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 83.33 nsec (for VDD = 5V). Refer to **Section 23.0 "Electrical Characteristics"** for minimum TAD under other operating conditions.

Example 19-1 shows a sample calculation for the ADCS<5:0> bits, assuming a device operating speed of 30 MIPS.

**EXAMPLE 19-1: A/D CONVERSION CLOCK CALCULATION**

TAD = 154 nsec
TCY = 33 nsec (30 MIPS)

$$ADCS<5:0> = 2 \frac{TAD}{TCY} - 1$$
$$= 2 \bullet \frac{154 \text{ nsec}}{33 \text{ nsec}} - 1$$
$$= 8.33$$

Therefore,
Set ADCS<5:0> = 9

$$\text{Actual } TAD = \frac{TCY}{2} (ADCS<5:0> + 1)$$
$$= \frac{33 \text{ nsec}}{2} (9 + 1)$$
$$= 165 \text{ nsec}$$

**TABLE 20-7: SYSTEM INTEGRATION REGISTER MAP(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | 0740 | TRAPR | IOPUWR | BGST | — | — | — | — | — | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | Depends on type of Reset. |
| OSCCON | 0742 | — | — | COSC<1:0> | | — | — | NOSC<1:0> | | POST<1:0> | | LOCK | — | CF | — | LPOSCEN | OSWEN | Depends on Configuration bits. |
| OSCTUN | 0744 | — | — | — | — | — | — | — | — | — | — | — | — | TUN<3:0> | | | | |

**Legend:** — = unimplemented bit, read as '0'

**Note 1:** Refer to the *"dsPIC30F Family Reference Manual* "(DS70046) for descriptions of register bit fields.

**TABLE 20-8: DEVICE CONFIGURATION REGISTER MAP(1)**

| Name | Address | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FOSC | F80000 | FCKSM<1:0> | | — | — | — | FOS<2:0> | | | — | — | — | FPR<4:0> | | | | |
| FWDT | F80002 | FWDTEN | — | — | — | — | — | — | — | — | — | FWPSA<1:0> | | FWPSB<3:0> | | | |
| FBORPOR | F80004 | MCLREN | — | — | — | — | PWMPIN | HPOL | LPOL | BOREN | — | BORV<1:0> | | — | — | FPWRT<1:0> | |
| FBS | F80006 | — | — | Reserved(2) | | — | — | — | Reserved(2) | — | — | — | — | Reserved(2) | | | |
| FSS | F80008 | — | — | Reserved(2) | | — | — | Reserved(2) | | — | — | — | — | Reserved(2) | | | |
| FGS | F8000A | — | — | — | — | — | — | — | — | — | — | — | — | — | Reserved(3) | GCP | GWRP |
| FICD | F8000C | BKBUG | COE | — | — | — | — | — | — | — | — | — | — | — | — | ICS<1:0> | |

**Legend:** — = unimplemented bit, read as '0'

**Note 1:** Refer to the *"dsPIC30F Family Reference Manual* "(DS70046) for descriptions of register bit fields.

**2:** Reserved bits read as '1' and must be programmed as '1'.

**3:** The FGS<2> bit is a read-only copy of the GCP bit (FGS<1>).

**TABLE 21-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of words | # of cycles | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 63 | RLC | RLC | f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC | f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC | Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 64 | RLNC | RLNC | f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC | f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC | Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 65 | RRC | RRC | f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC | f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC | Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 66 | RRNC | RRNC | f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 67 | SAC | SAC | Acc,#Slit4,Wdo | Store Accumulator | 1 | 1 | None |
| | | SAC.R | Acc,#Slit4,Wdo | Store Rounded Accumulator | 1 | 1 | None |
| 68 | SE | SE | Ws,Wnd | Wnd = Sign-Extended Ws | 1 | 1 | C,N,Z |
| 69 | SETM | SETM | f | f = 0xFFFF | 1 | 1 | None |
| | | SETM | WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM | Ws | Ws = 0xFFFF | 1 | 1 | None |
| 70 | SFTAC | SFTAC | Acc,Wn | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC | Acc,#Slit6 | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 71 | SL | SL | f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL | Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL | Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 72 | SUB | SUB | Acc | Subtract Accumulators | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SUB | f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | f,WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | #lit10,Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,Ws,Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,#lit5,Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 73 | SUBB | SUBB | f | f = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | f,WREG | WREG = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | #lit10,Wn | Wn = Wn – lit10 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,Ws,Wd | Wd = Wb – Ws – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,#lit5,Wd | Wd = Wb – lit5 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 74 | SUBR | SUBR | f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | f,WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,Ws,Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,#lit5,Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 75 | SUBBR | SUBBR | f | f = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | f,WREG | WREG = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,Ws,Wd | Wd = Ws – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,#lit5,Wd | Wd = lit5 – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 76 | SWAP | SWAP.b | Wn | Wn = Nibble Swap Wn | 1 | 1 | None |
| | | SWAP | Wn | Wn = Byte Swap Wn | 1 | 1 | None |
| 77 | TBLRDH | TBLRDH | Ws,Wd | Read Prog<23:16> to Wd<7:0> | 1 | 2 | None |
| 78 | TBLRDL | TBLRDL | Ws,Wd | Read Prog<15:0> to Wd | 1 | 2 | None |
| 79 | TBLWTH | TBLWTH | Ws,Wd | Write Ws<7:0> to Prog<23:16> | 1 | 2 | None |

**TABLE 23-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Conditions** | | |
| **Power-Down Current ($I_{PD}$)(2)** | | | | | | |
| DC60a | 0.3 | 14.0 | µA | 25°C | 3.3V | Base Power-Down Current |
| DC60b | 1.0 | 27.0 | µA | 85°C | | |
| DC60c | 12.0 | 55.0 | µA | 125°C | | |
| DC60e | 0.5 | 20.0 | µA | 25°C | 5V | |
| DC60f | 2.0 | 40.0 | µA | 85°C | | |
| DC60g | 17.0 | 90.0 | µA | 125°C | | |
| DC61a | 8.0 | 12.0 | µA | 25°C | 3.3V | Watchdog Timer Current: $\Delta I_{WDT}$(3) |
| DC61b | 8.0 | 12.0 | µA | 85°C | | |
| DC61c | 8.0 | 12.0 | µA | 125°C | | |
| DC61e | 14.0 | 21.0 | µA | 25°C | 5V | |
| DC61f | 14.0 | 21.0 | µA | 85°C | | |
| DC61g | 14.0 | 21.0 | µA | 125°C | | |
| DC62a | 4.0 | 10.0 | µA | 25°C | 3.3V | Timer 1 w/32 kHz Crystal: $\Delta I_{TI32}$(3) |
| DC62b | 5.0 | 10.0 | µA | 85°C | | |
| DC62c | 4.0 | 10.0 | µA | 125°C | | |
| DC62e | 4.0 | 15.0 | µA | 25°C | 5V | |
| DC62f | 6.0 | 15.0 | µA | 85°C | | |
| DC62g | 5.0 | 15.0 | µA | 125°C | | |
| DC63a | 33.0 | 57.0 | µA | 25°C | 3.3V | BOR on: $\Delta I_{BOR}$(3) |
| DC63b | 37.0 | 57.0 | µA | 85°C | | |
| DC63c | 38.0 | 57.0 | µA | 125°C | | |
| DC63e | 38.0 | 65.0 | µA | 25°C | 5V | |
| DC63f | 41.0 | 65.0 | µA | 85°C | | |
| DC63g | 43.0 | 65.0 | µA | 125°C | | |

**Note 1:** Parameters are for design guidance only and are not tested.

**2:** These parameters are characterized but not tested in manufacturing.

**3:** These values represent the difference between the base power-down current and the power-down current with the specified peripheral enabled during Sleep.

## 23.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC30F AC characteristics and timing parameters.

**TABLE 23-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 23.1 "DC Characteristics"**. |

**FIGURE 23-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

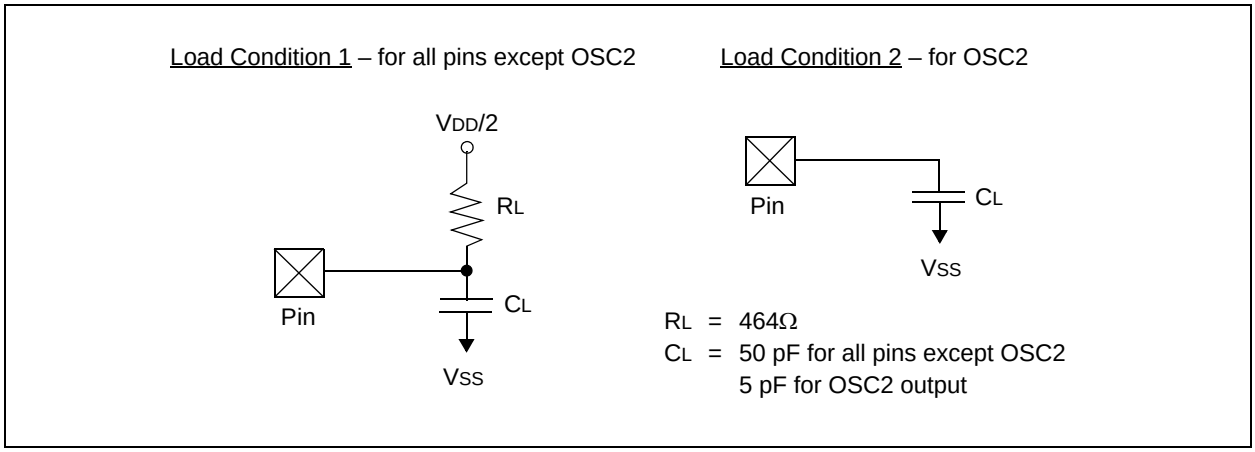



**FIGURE 23-3: EXTERNAL CLOCK TIMING**

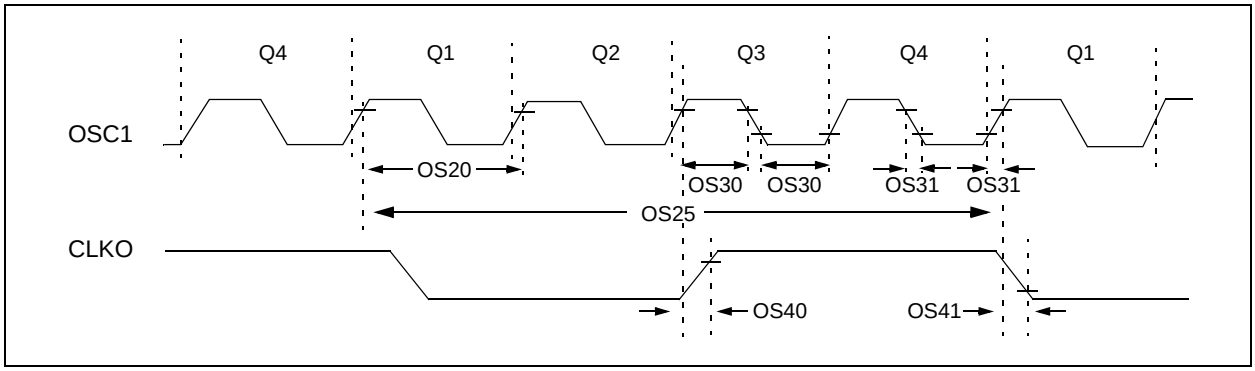


**TABLE 23-35: SPI MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time | 30 | — | — | ns | |
| SP71 | TscH | SCKx Input High Time | 30 | — | — | ns | |
| SP72 | TscF | SCKx Input Fall Time(3) | — | 10 | 25 | ns | |
| SP73 | TscR | SCKx Input Rise Time(3) | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time(3) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(3) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 30 | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}\downarrow$ to SCKx$\downarrow$ or SCKx$\uparrow$ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}\uparrow$ to SDOx Output High-Impedance(4) | 10 | — | 50 | ns | |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}\uparrow$ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | |
| SP60 | TssL2doV | $\overline{SDO}$x Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI pins.

**TABLE 23-37: I²C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(1) | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(1) | 0 | 0.3 | µs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.6 | — | µs | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | 0 | 3500 | ns | |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode(1) | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | |

**Note 1:** Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).