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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	30
Program Memory Size	24KB (8K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3011-20i-ml

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3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see Section 3.1.2 "Data Access From Program Memory Using Program Space Visibility"). The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the Isw of any address within program space, without going through data space. The TBLRDH and TBLWTH instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the lsw, and TBLRDH and TBLWTH access the space which contains the MSB.

Figure 3-2 illustrates how the EA is created for table operations and data space accesses (PSV = 1). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space.

- TBLRDL: Table Read Low Word: Read the lsw of the program address; P<15:0> maps to D<15:0>. Byte: Read one of the LSBs of the program address; P<7:0> maps to the destination byte when byte select = 0; P<15:8> maps to the destination byte when byte select = 1.
- TBLWTL: Table Write Low (refer to Section 6.0 "Flash Program Memory" for details on Flash programming).
- TBLRDH: Table Read High Word: Read the msw of the program address; P<23:16> maps to D<7:0>; D<15:8> will always

P<23:16 > maps to D<7:0>; D<15:8> will always be = 0.

Byte: Read one of the MSBs of the program address;

P<23:16> maps to the destination byte when byte select = 0;

The destination byte will always be = 0 when byte select = 1.

 TBLWTH: Table Write High (refer to Section 6.0 "Flash Program Memory" for details on Flash programming).



FIGURE 3-3: PROGRAM DATA TABLE ACCESS (Isw)

4.2.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes may, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected effective address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the effective address. When an address offset (e.g., [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remains unchanged.

4.3 Bit-Reversed Addressing

Bit-Reversed Addressing is intended to simplify data re-ordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which may be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.3.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing is enabled when:

- BWM (W register selection) in the MODCON register is any value other than 15 (the stack can not be accessed using Bit-Reversed Addressing) and
- 2. the BREN bit is set in the XBREV register and
- 3. the addressing mode used is Register Indirect with Pre-Increment or Post-Increment.

If the length of a bit-reversed buffer is $M = 2^N$ bytes, then the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the bit-reversed address modifier or 'pivot point' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is
	always clear). The XB value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing will only be executed for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It will not function for any other addressing mode or for byte-sized data, and normal addresses will be generated instead. When Bit-Reversed Addressing is active, the W Address Pointer will always be added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode will be ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing should not be enabled together. In the event that the user attempts to do this, Bit-Reversed Addressing will assume priority when active for the X WAGU, and X WAGU Modulo Addressing will be disabled. However, Modulo Addressing will continue to function in the X RAGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, then a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.



FIGURE 4-2: BIT-REVERSED ADDRESS EXAMPLE

5.1 Interrupt Priority

The user-assignable Interrupt Priority (IP<2:0>) bits for each individual interrupt source are located in the 3 LSbs of each nibble, within the IPCx register(s). Bit 3 of each nibble is not used and is read as a '0'. These bits define the priority level assigned to a particular interrupt by the user.

Note:	The user-assignable priority levels start at
	0, as the lowest priority, and Level 7, as
	the highest priority.

Since more than one interrupt request source may be assigned to a specific user-assigned priority level, a means is provided to assign priority within a given level. This method is called "Natural Order Priority".

Natural Order Priority is determined by the position of an interrupt in the vector table, and only affects interrupt operation when multiple interrupts with the same user-assigned priority become pending at the same time.

Table 5-1 lists the interrupt numbers and interrupt sources for the dsPIC DSC devices and their associated vector numbers.

- **Note 1:** The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.
 - **2:**The natural order priority number is the same as the INT number.

The ability for the user to assign every interrupt to one of seven priority levels implies that the user can assign a very high overall priority level to an interrupt with a low natural order priority. For example, the PWM Fault A Interrupt can be given a priority of 7. The INTO (external interrupt 0) may be assigned to priority Level 1, thus giving it a very low effective priority.

TABLE 5-1:INTERRUPT VECTOR TABLE

Interrupt Number	Vector Number	Interrupt Source					
	Highest	Natural Order Priority					
0	8	INT0 – External Interrupt 0					
1	9	IC1 – Input Capture 1					
2	10	OC1 – Output Compare 1					
3	10	T1 - Timer1					
4	12	IC2 – Input Capture 2					
5	13	OC2 – Output Compare 2					
6	14	T2 – Timer2					
7	15	T3 – Timer3					
8	16	SPI1					
9	17	U1RX – UART1 Receiver					
10	18	U1TX – UART1 Transmitter					
11	19	ADC – ADC Convert Done					
12	20	NVM – NVM Write Complete					
13	21	SI2C – I ² C Slave Interrupt					
14	22	MI2C – I ² C Master Interrupt					
15	23	Input Change Interrupt					
16	24	INT1 – External Interrupt 1					
17	25	IC7 – Input Capture 7					
18	26	IC8 – Input Capture 8					
19	27	OC3 – Output Compare 3 ⁽¹⁾					
20	28	OC4 - Output Compare 4(1)					
21	29	T4 – Timer4					
22	30	T5 – Timer5					
23	31	INT2 – External Interrupt 2					
24	32	U2RX – UART2 Receiver ⁽¹⁾					
25	33	U2TX – UART2 Transmitter ⁽¹⁾					
26	34	Reserved					
27	35	Reserved					
28	36	Reserved					
29	37	Reserved					
30	38	Reserved					
31	39	Reserved					
32	40	Reserved					
33	41	Reserved					
34	42	Reserved					
35	43	Reserved					
36	44	Reserved					
37	45	Reserved					
38	46	Reserved					
39	47	PWM – PWM Period Match					
40	48	QEI – QEI Interrupt					
41	49	Reserved					
42	50	Reserved					
43	51	FLTA – PWM Fault A					
44	52	Reserved					
45-53	53-61	Reserved					
1	Lowest N	Natural Order Priority					

Note 1: Available on dsPIC30F3011 only

FIGURE 10-1: 32-BIT TIMER2/3 BLOCK DIAGRAM







FIGURE 10-3: 16-BIT TIMER3 BLOCK DIAGRAM (TYPE C TIMER)



TABLE 10-1: TIMER2/3 REGISTER MAP⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR2	0106	06 Timer2 Register											uuuu uuuu uuuu uuuu					
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)									uuuu uuuu uuuu uuuu							
TMR3	010A	Timer3 Register									uuuu uuuu uuuu uuuu							
PR2	010C	Period Register 2										1111 1111 1111 1111						
PR3	010E				_	_			Pe	riod Registe	r 3	-	_					1111 1111 1111 1111
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	_	0000 0000 0000 0000
T3CON	0112	TON	—	TSIDL	_	_	—	_	—	—	TGATE	TCKPS1	TCKPS0	-	_	TCS	_	0000 0000 0000 0000

Legend: u = uninitialized bit; - = unimplemented bit, read as '0'

Note 1: Refer to "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

13.4.2 PWM PERIOD

The PWM period is specified by writing to the PRx register. The PWM period can be calculated using Equation 13-1.

EQUATION 13-1: PWM PERIOD

 $PWM \ period = [(PRx) + 1] \cdot 4 \cdot Tosc \cdot$ $(TMRx \ prescale \ value)$

PWM frequency is defined as *1/[PWM period]*.

When the selected TMRx is equal to its respective Period register, PRx, the following four events occur on the next increment cycle:

- TMRx is cleared.
- The OCx pin is set.
 - Exception 1: If PWM duty cycle is 0x0000, the OCx pin will remain low.
 - Exception 2: If duty cycle is greater than PRx, the pin will remain high.
- The PWM duty cycle is latched from OCxRS into OCxR.
- The corresponding timer interrupt flag is set.

See Figure 13-1 for key PWM period comparisons. Timer3 is referred to in the figure for clarity.



19.7 ADC Conversion Speeds

The dsPIC30F 10-bit ADC specifications permit a maximum 1 Msps sampling rate. Table 19-1 summarizes the conversion speeds for the dsPIC30F 10-bit A/D converter and the required operating conditions.

TABLE 19-1:	10-BIT ADC CONVERSION RATE PARAMETERS
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dsPIC30F 10-Bit ADC Conversion Rates										
ADC Speed	TAD Minimum	Sampling Time Min	Rs Max	Vdd	Temperature	A/D Channels Configuration				
Up to 1 Msps ⁽¹⁾	83.33 ns	12 Tad	500Ω	4.5V to 5.5V	-40°C to +85°C	ANX CH1, 2 or 3 S/H S/H ADC				
Up to 750 ksps ⁽¹⁾	95.24 ns	2 Tad	500Ω	4.5V to 5.5V	-40°C to +85°C	ANX CHX ADC				
Up to 600 ksps ⁽¹⁾	138.89 ns	12 TAD	500Ω	3.0V to 5.5V	-40°C to +125°C	ANX CH1, 2 or 3 S/H S/H ADC				
Up to 500 ksps	153.85 ns	1 Tad	5.0 kΩ	4.5V to 5.5V	-40°C to +125°C	ANX CHX ANX ADC ANX OF VREF-				
Up to 300 ksps	256.41 ns	1 Tad	5.0 kΩ	3.0V to 5.5V	-40°C to +125°C	ANX ANX OF VREF- ANX OF VREF- ANX OF VREF- ANX OF VREF-				

Note 1: External VREF- and VREF+ pins must be used for correct operation. See Figure 19-2 for recommended circuit.

19.7.1.3 1 Msps Configuration Items

The following configuration items are required to achieve a 1 Msps conversion rate.

- Comply with conditions provided in Table 20-2
- Connect external VREF+ and VREF- pins following the recommended circuit shown in Figure 19-2
- Set SSRC<2:0> = 111 in the ADCON1 register to enable the auto-convert option
- Enable automatic sampling by setting the ASAM control bit in the ADCON1 register
- Enable sequential sampling by clearing the SIMSAM bit in the ADCON1 register
- Enable at least two sample and hold channels by writing the CHPS<1:0> control bits in the ADCON2 register
- Write the SMPI<3:0> control bits in the ADCON2 register for the desired number of conversions between interrupts. At a minimum, set SMPI<3:0> = 0001 since at least two sample and hold channels should be enabled
- Configure the A/D clock period to be: 1

= 83.33 ns

by writing to the ADCS<5:0> control bits in the ADCON3 register

- Configure the sampling time to be 2 TAD by writing: SAMC<4:0> = 00010
- Select at least two channels per analog input pin by writing to the ADCHS register

19.7.2 750 ksps CONFIGURATION GUIDELINE

The following configuration items are required to achieve a 750 ksps conversion rate. This configuration assumes that a single analog input is to be sampled.

- Comply with conditions provided in Table 20-2
- Connect external VREF+ and VREF- pins following the recommended circuit shown in Figure 19-2
- Set SSRC<2:0> = 111 in the ADCON1 register to enable the auto-convert option
- Enable automatic sampling by setting the ASAM control bit in the ADCON1 register
- Enable one sample and hold channel by setting CHPS<1:0> = 00 in the ADCON2 register
- Write the SMPI<3:0> control bits in the ADCON2 register for the desired number of conversions between interrupts
- Configure the A/D clock period to be:

1

$$\frac{12+2}{(12+2) \times 750,000} = 95.24 \text{ ns}$$

by writing to the ADCS<5:0> control bits in the ADCON3 register

• Configure the sampling time to be 2 TAD by writing: SAMC<4:0> = 00010

19.7.3 600 ksps CONFIGURATION GUIDELINE

The configuration for 600 ksps operation is dependent on whether a single input pin is to be sampled or whether multiple pins will be sampled.

19.7.3.1 Single Analog Input

When performing conversions at 600 ksps for a single analog input, at least two sample and hold channels must be enabled. The analog input multiplexer must be configured so that the same input pin is connected to both sample and hold channels. The A/D converts the value held on one S/H channel, while the second S/H channel acquires a new input sample.

19.7.3.2 Multiple Analog Input

The A/D converter can also be used to sample multiple analog inputs using multiple sample and hold channels. In this case, the total 600 ksps conversion rate is divided among the different input signals. For example, four inputs can be sampled at a rate of 150 ksps for each signal or two inputs can be sampled at a rate of 300 ksps for each signal. Sequential sampling must be used in this configuration to allow adequate sampling time on each input.

19.7.3.3 600 ksps Configuration Items

The following configuration items are required to achieve a 600 ksps conversion rate.

- Comply with conditions provided in Table 20-2
- Connect external VREF+ and VREF- pins following the recommended circuit shown in Figure 19-2
- Set SSRC<2:0> = 111 in the ADCON1 register to enable the auto-convert option
- Enable automatic sampling by setting the ASAM control bit in the ADCON1 register
- Enable sequential sampling by clearing the SIMSAM bit in the ADCON1 register
- Enable at least two sample and hold channels by writing the CHPS<1:0> control bits in the ADCON2 register
- Write the SMPI<3:0> control bits in the ADCON2 register for the desired number of conversions between interrupts. At a minimum, set SMPI<3:0> = 0001 since at least two sample and hold channels should be enabled
- Configure the A/D clock period to be:

 $\frac{1}{12 \times 600,000} = 138.89 \text{ ns}$

by writing to the ADCS<5:0> control bits in the ADCON3 register

• Configure the sampling time to be 2 TAD by writing: SAMC<4:0> = 00010

Select at least two channels per analog input pin by writing to the ADCHS register.



FIGURE 20-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1



FIGURE 20-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



Field	Description							
Wb	Base W register ∈ {W0W15}							
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }							
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }							
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)							
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions \in {W4*W4,W5*W5,W6*W6,W7*W7}							
$\label{eq:withdef} \begin{array}{llllllllllllllllllllllllllllllllllll$								
Wn	One of 16 working registers ∈ {W0W15}							
Wnd	One of 16 destination working registers ∈ {W0W15}							
Wns	One of 16 source working registers ∈ {W0W15}							
WREG	W0 (working register used in File register instructions)							
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }							
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }							
Wx X data space Prefetch Address register for DSP instructions ∈ {[W8]+=6, [W8]+=4, [W8]+=2, [W8], [W8]-=6, [W8]-=4, [W8]-=2, [W9]+=6, [W9]+=4, [W9]+=2, [W9], [W9]-=6, [W9]-=4, [W9]-=2, [W9+W12],none}								
Wxd	X data space Prefetch Destination register for DSP instructions \in {W4W7}							
Wy	Y data space Prefetch Address register for DSP instructions ∈ {[W10]+=6, [W10]+=4, [W10]+=2, [W10], [W10]-=6, [W10]-=4, [W10]-=2, [W11]+=6, [W11]+=4, [W11]+=2, [W11], [W11]-=6, [W11]-=4, [W11]-=2, [W11+W12], none}							
Wyd	Y data space Prefetch Destination register for DSP instructions \in {W4W7}							

TABLE 21-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

DC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Operatir	ng Voltage	(2)								
DC10	Vdd	Supply Voltage	2.5	—	5.5	V	Industrial temperature			
DC11	Vdd	Supply Voltage	3.0	_	5.5	V	Extended temperature			
DC12	Vdr	RAM Data Retention Voltage ⁽³⁾	1.75	_	—	V				
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	—	Vss	V				
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	_	V/ms	0-5V in 0.1 sec 0-3V in 60 ms			

TABLE 23-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Note 1: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

3: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 23-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACT	ERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Parameter No.	Typical ⁽¹⁾	Мах	Units	Units Conditions						
Operating Cur	rent (IDD) ⁽²⁾									
DC31a	1.4	2.5	mA	25°C						
DC31b	1.4	2.5	mA	85°C	3.3V					
DC31c	1.4	2.5	mA	125°C		0.128 MIPS				
DC31e	3.0	4.5	mA	25°C		LPRC (512 kHz)				
DC31f	2.8	4.5	mA	85°C	5V					
DC31g	2.8	4.5	mA	125°C						
DC30a	3.2	5.0	mA	25°C						
DC30b	3.3	5.0	mA	85°C	3.3V					
DC30c	3.3	5.0	mA	125°C		1.8 MIPS				
DC30e	6.0	9.0	mA	25°C		FRC (7.37MHz)				
DC30f	5.9	9.0	mA	85°C	5V					
DC30g	5.9	9.0	mA	125°C						
DC23a	10.0	17.0	mA	25°C						
DC23b	10.0	17.0	mA	85°C	3.3V					
DC23c	11.0	17.0	mA	125°C						
DC23e	17.0	27.0	mA	25°C		4 WIF 3				
DC23f	17.0	27.0	mA	85°C	5V					
DC23g	18.0	27.0	mA	125°C						
DC24a	24.0	38.0	mA	25°C						
DC24b	25.0	38.0	mA	85°C	3.3V					
DC24c	25.0	38.0	mA	125°C						
DC24e	41.0	62.0	mA	25°C		10 MIF 3				
DC24f	41.0	62.0	mA	85°C	5V					
DC24g	41.0	62.0	mA	125°C						
DC27a	46.0	70.0	mA	25°C	3 2\/					
DC27b	46.0	70.0	mA	85°C	3.37					
DC27d	76.0	115.0	mA	25°C		20 MIPS				
DC27e	76.0	115.0	mA	85°C	5V					
DC27f	76.0	115.0	mA	125°C						
DC29a	109.0	155.0	mA	25°C	5\/	30 MIPS				
DC29b	108.0	155.0	mA	85°C	5.	30 Will 3				

Note 1: Data in "Typical" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. MCLR = VDD, WDT, FSCM, LVD and BOR are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating.





TABLE 23-19: CLKO AND I/O TIMING REQUIREMENTS

AC CHAR	ACTERISTI	CS	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characterist	Min	Typ ⁽⁴⁾	Max	Units	Conditions		
DO31	TIOR	Port Output Rise Tim	е	—	7	20	ns		
DO32	TIOF	Port Output Fall Time	—	7	20	ns			
DI35	TINP	INTx Pin High or Low	20	—		ns			
DI40	TRBP	CNx High or Low Tim	2 TCY	_	_	ns			

Note 1: These parameters are asynchronous events not related to any internal clock edges.

2: Measurements are taken in RC mode and EC mode where CLKO output is 4 x Tosc.

3: These parameters are characterized but not tested in manufacturing.

4: Data in "Typ" column is at 5V, 25°C unless otherwise stated.

FIGURE 23-12: MOTOR CONTROL PWM MODULE FAULT TIMING CHARACTERISTICS



FIGURE 23-13: MOTOR CONTROL PWM MODULE TIMING CHARACTERISTICS



TABLE 23-29: MOTOR CONTROL PWM MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standar (unless Operatir	$\begin{array}{l} \mbox{Standard Operating Conditions: } 2.5V \ to \ 5.5V \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}\mbox{C} \leq \mbox{TA} \leq +85^{\circ}\mbox{C for Industrial} \\ & -40^{\circ}\mbox{C} \leq \mbox{TA} \leq +125^{\circ}\mbox{C for Extended} \end{array}$						
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Conditions						
MP10	TFPWM	PWM Output Fall Time	—	—	_	ns	See parameter DO32			
MP11	TRPWM	PWM Output Rise Time	_	_		ns	See parameter DO31			
MP20	Tfd	Fault Input ↓ to PWM I/O Change	—	_	50	ns				
MP30	Тғн	Minimum Pulse Width	50		_	ns				

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 23-14: QEA/QEB INPUT CHARACTERISTICS



TABLE 23-30: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic ⁽¹⁾		Тур ⁽²⁾	Мах	Units	Conditions
TQ30	TQUL	Quadrature Input Low Time		6 Tcy	_	ns	
TQ31	ΤουΗ	Quadrature Input High Time		6 TCY	—	ns	
TQ35	ΤουΙΝ	Quadrature Input Period		12 Tcy	—	ns	
TQ36	ΤουΡ	Quadrature Phase Period		3 TCY	—	ns	
TQ40	TQUFL	Filter Time to Recognize Lov with Digital Filter	V,	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ41	TQUFH	Filter Time to Recognize Hig with Digital Filter	h,	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)

Note 1: These parameters are characterized but not tested in manufacturing.

2: N = Index Channel Digital Filter Clock Divide Select bits. Refer to Section 16. "Quadrature Encoder Interface (QEI)" in the "dsPIC30F Family Reference Manual" (DS70046).

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP70	TscL	SCKx Input Low Time	30	—	_	ns	
SP71	TscH	SCKx Input High Time	30	—	_	ns	
SP72	TscF	SCKx Input Fall Time ⁽³⁾	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time ⁽³⁾	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time ⁽³⁾	—	_	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time ⁽³⁾	—	—	_	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	_	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	_		ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	_	_	ns	
SP50	TssL2scH, TssL2scL	SSx↓ to SCKx↑ or SCKx↓ Input	120	_		ns	
SP51	TssH2doZ	SSx↑ to SDOx Output High-Impedance ⁽³⁾	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 Tcy + 40	—	_	ns	—

TABLE 23-34: SPI MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 50 pF load on all SPI pins.

TABLE 23-36: I²C[™] BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic		Min ⁽¹⁾	Max	Units	Conditions	
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)		μS		
			400 kHz mode	Tcy/2 (BRG + 1)		μs		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	_	μs		
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μS		
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		μS		
IM20	TF:SCL	SDA and SCL	100 kHz mode		300	ns	CB is specified to be	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
			1 MHz mode ⁽²⁾	—	100	ns		
IM21	TR:SCL	SDA and SCL	100 kHz mode	_	1000	ns	CB is specified to be	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
			1 MHz mode ⁽²⁾	_	300	ns		
IM25	TSU:DAT	Data Input	100 kHz mode	250	_	ns		
		Setup Time	400 kHz mode	100	—	ns		
			1 MHz mode ⁽²⁾	_		ns		
IM26	M26 THD:DAT	Data Input Hold Time	100 kHz mode	0	_	ns		
			400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽²⁾			ns		
IM30	TSU:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)		μS	Only relevant for	
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μs	Repeated Start	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		μS	condition	
IM31	THD:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)		μS	After this period the	
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μs	first clock pulse is	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		μS	generated	
IM33	TSU:STO	O Stop Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 1)		μS		
			400 kHz mode	Tcy/2 (BRG + 1)		μS		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		μS		
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)		ns		
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)		ns		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		ns		
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	ns		
		From Clock	400 kHz mode	—	1000	ns		
			1 MHz mode ⁽²⁾	_		ns		
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	Time the bus must be	
			400 kHz mode	1.3	—	μS	free before a new	
			1 MHz mode ⁽²⁾	—	—	μS	transmission can start	
IM50	Св	Bus Capacitive Loading		—	400	pF		

Note 1: BRG is the value of the I²C[™] Baud Rate Generator. Refer to Section 21. "Inter-Integrated Circuit (I²C)" in the "dsPIC30F Family Reference Manual" (DS70046). 2: Maximum pin capacitance = 10 pF for all I^2C pins (for 1 MHz mode only).

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	MILLIMETERS					
Dimensio	n Limits	MIN	NOM	MAX		
Number of Pins	Ν	28				
Pitch	е		1.27 BSC			
Overall Height	А	-	—	2.65		
Molded Package Thickness	A2	2.05	—	Ι		
Standoff §	A1	0.10 – 0.30				
Overall Width	Е	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (optional)	h	0.25 – 0.75				
Foot Length	L	0.40	-	1.27		
Footprint L1			1.40 REF			
Foot Angle Top	φ	0°	—	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	_	15°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A