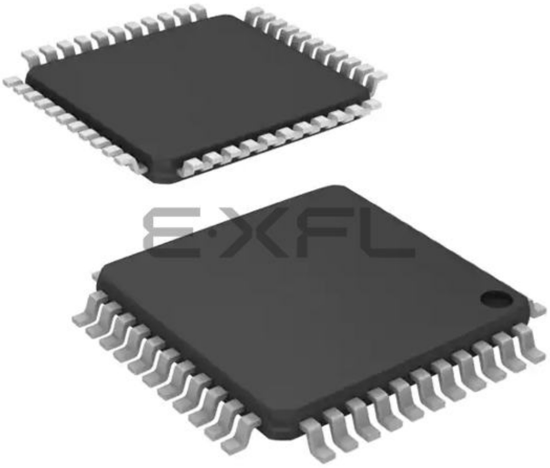
Microchip Technology - DSPIC30F3011T-30I/PT Datasheet



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Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	30
Program Memory Size	24KB (8K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3011t-30i-pt

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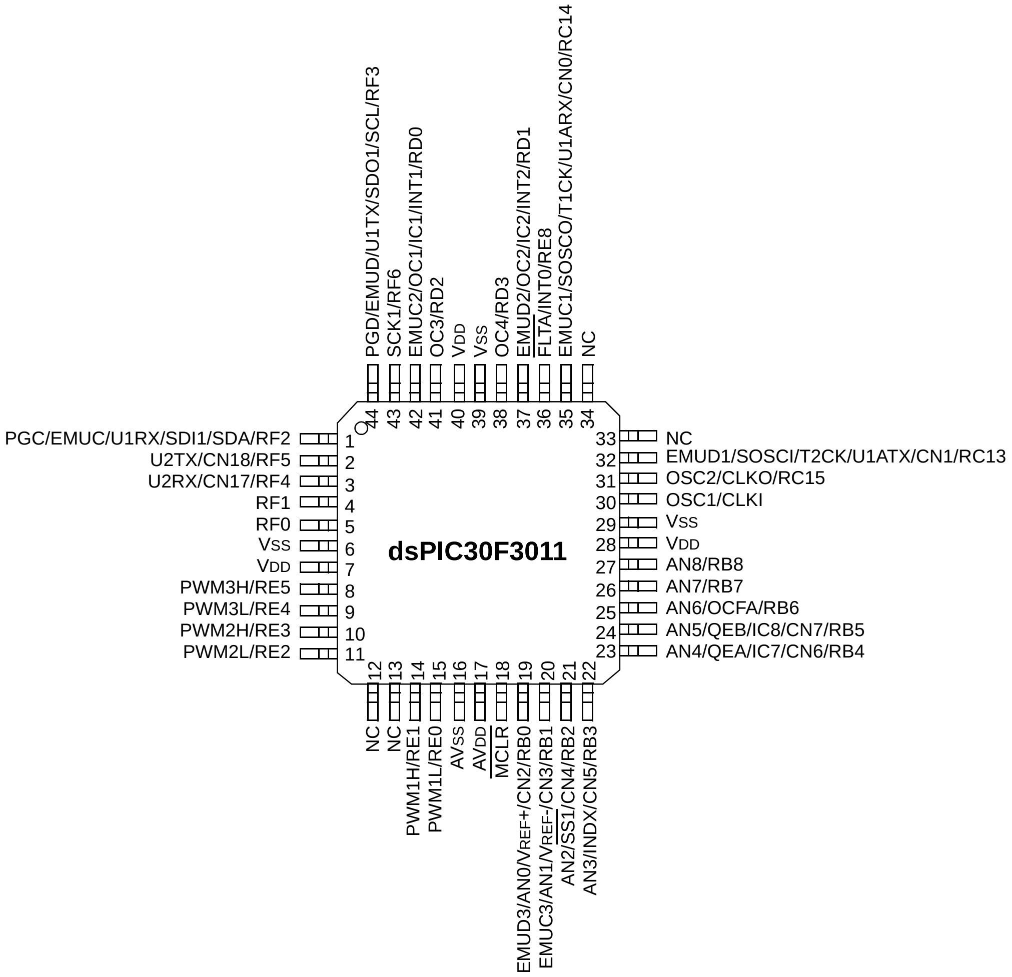
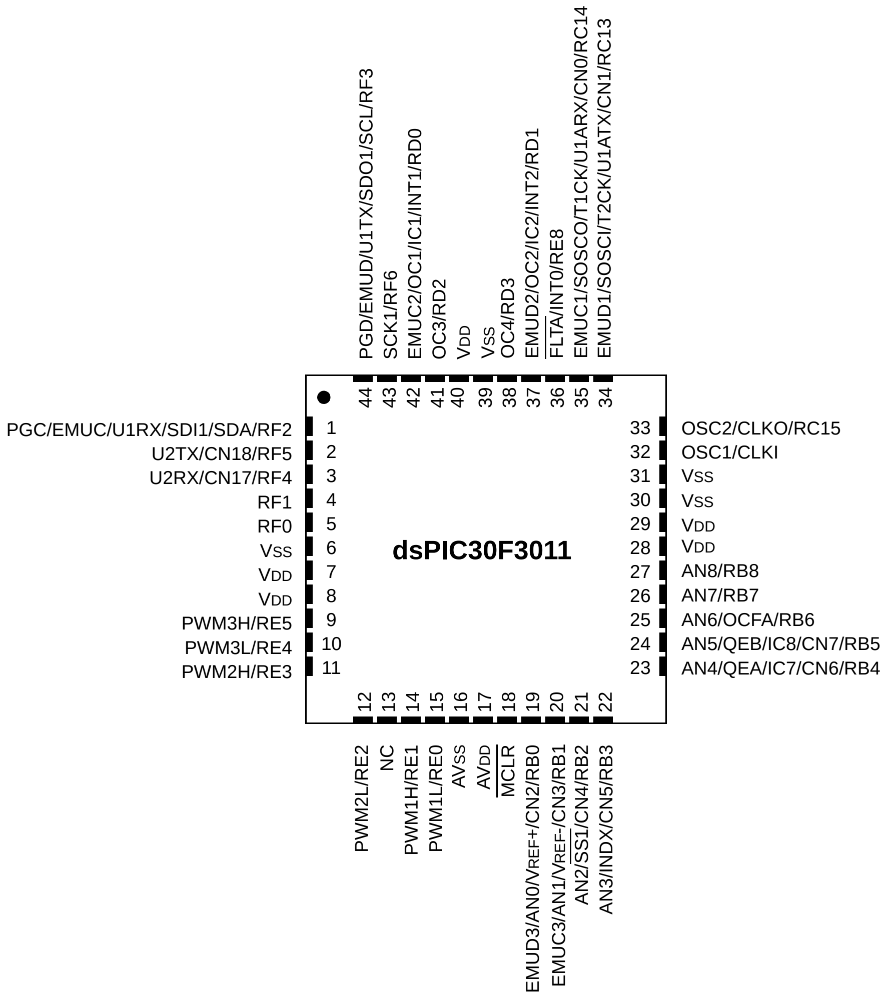
Pin Diagrams (Continued)

44-Pin TQFP



Pin Diagrams (Continued)

44-Pin QFN[1]



Note 1: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see **Section 3.1.2 "Data Access From Program Memory Using Program Space Visibility"**). The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lsw of any address within program space, without going through data space. The `TBLRDH` and `TBLWTH` instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word-wide address spaces, residing side by side, each with the same address range. `TBLRDL` and `TBLWTL` access the space which contains the lsw, and `TBLRDH` and `TBLWTH` access the space which contains the MSB.

Figure 3-2 illustrates how the EA is created for table operations and data space accesses (PSV = `1`). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space.

1. **`TBLRDL:`** Table Read Low
   Word: Read the lsw of the program address;
   P<15:0> maps to D<15:0>.
   Byte: Read one of the LSBs of the program address;
   P<7:0> maps to the destination byte when byte select = `0`;
   P<15:8> maps to the destination byte when byte select = `1`.
2. **`TBLWTL:`** Table Write Low (refer to **Section 6.0 "Flash Program Memory"** for details on Flash programming).
3. **`TBLRDH:`** Table Read High
   Word: Read the msw of the program address;
   P<23:16> maps to D<7:0>; D<15:8> will always be = `0`.
   Byte: Read one of the MSBs of the program address;
   P<23:16> maps to the destination byte when byte select = `0`;
   The destination byte will always be = `0` when byte select = `1`.
4. **`TBLWTH:`** Table Write High (refer to **Section 6.0 "Flash Program Memory"** for details on Flash programming).

FIGURE 3-3: PROGRAM DATA TABLE ACCESS (lsw)

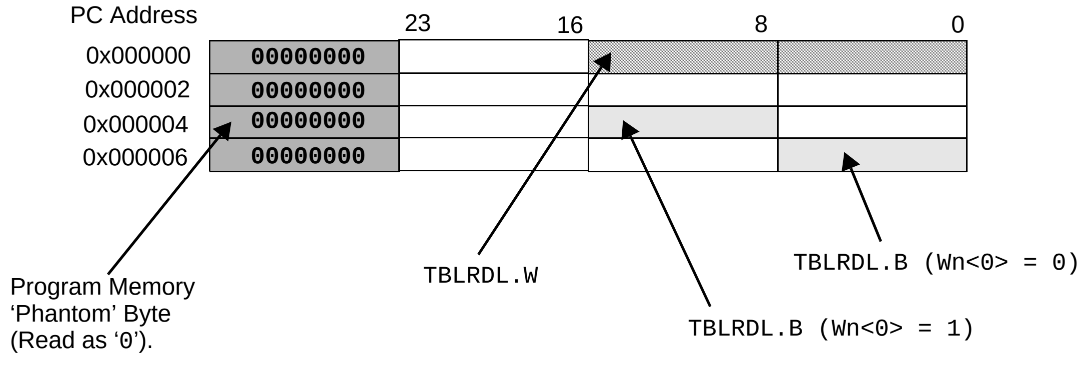
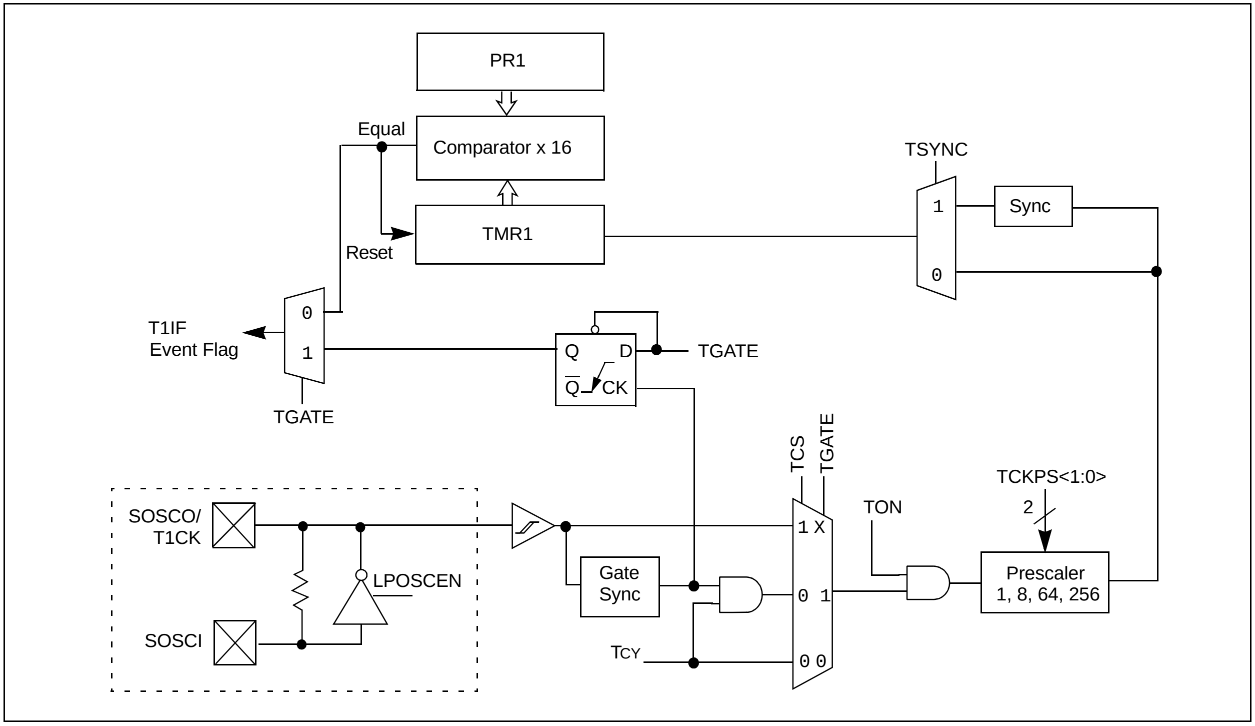


FIGURE 9-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM (TYPE A TIMER)



9.1 Timer Gate Operation

The 16-bit timer can be placed in the Gated Time Accumulation mode. This mode allows the internal TCY to increment the respective timer when the gate input signal (T1CK pin) is asserted high. Control bit, TGATE (T1CON<6>), must be set to enable this mode. The timer must be enabled (TON = `1`) and the timer clock source set to internal (TCS = `0`).

When the CPU goes into the Idle mode, the timer will stop incrementing unless TSIDL = `0`. If TSIDL = `1`, the timer will resume the incrementing sequence upon termination of the CPU Idle mode.

9.2 Timer Prescaler

The input clock (FOSC/4 or external clock) to the 16-bit Timer has a prescale option of 1:1, 1:8, 1:64 and 1:256, selected by control bits, TCKPS<1:0> (T1CON<5:4>). The prescaler counter is cleared when any of the following occurs:

- A write to the TMR1 register
- Clearing of the TON bit (T1CON<15>)
- A device Reset such as a POR and BOR

However, if the timer is disabled (TON = `0`), then the timer prescaler cannot be reset since the prescaler clock is halted.

The TMR1 register is not cleared when the T1CON register is written. It is cleared by writing to the TMR1 register.

9.3 Timer Operation During Sleep Mode

During CPU Sleep mode, the timer will operate if:

- The timer module is enabled (TON = `1`) and
- The timer clock source is selected as external (TCS = `1`) and
- The TSYNC bit (T1CON<2>) is asserted to a logic ‘`0`’, which defines the external clock source as asynchronous

When all three conditions are true, the timer will continue to count up to the Period register and be reset to 0x0000.

When a match between the timer and the Period register occurs, an interrupt can be generated, if the respective timer interrupt enable bit is asserted.

10.0 TIMER2/3 MODULE

> **Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the 32-bit general purpose timer module (Timer2/3) and associated operational modes. Figure 10-1 depicts the simplified block diagram of the 32-bit Timer2/3 module. Figure 10-2 and Figure 10-3 show Timer2/3 configured as two independent 16-bit timers; Timer2 and Timer3, respectively.

> **Note:** Timer2 is a 'Type B' timer and Timer3 is a 'Type C' timer. Please refer to appropriate timer type in **Section 23.0 "Electrical Characteristics"**.

The Timer2/3 module is a 32-bit timer, which can be configured as two 16-bit timers, with selectable operating modes. These timers are utilized by other peripheral modules such as:

- Input Capture
- Output Compare/Simple PWM

The following sections provide a detailed description, including setup and control registers, along with associated block diagrams for the operational modes of the timers.

The 32-bit timer has the following modes:

- Two independent 16-bit timers (Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit timer operation
- Single 32-bit synchronous counter

Further, the following operational characteristics are supported:

- ADC Event Trigger
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match

These operating modes are determined by setting the appropriate bit(s) in the 16-bit T2CON and T3CON SFRs.

For 32-bit timer/counter operation, Timer2 is the lsw and Timer3 is the msw of the 32-bit timer.

> **Note:** For 32-bit timer operation, T3CON control bits are ignored. Only T2CON control bits are used for setup and control. Timer2 clock and gate inputs are utilized for the 32-bit timer module, but an interrupt is generated with the Timer3 Interrupt Flag (T3IF) and the interrupt is enabled with the Timer3 Interrupt Enable bit (T3IE).

16-Bit Mode: In the 16-bit mode, Timer2 and Timer3 can be configured as two independent 16-bit timers. Each timer can be set up in either 16-bit Timer mode or 16-bit Synchronous Counter mode. See **Section 9.0 "Timer1 Module"** for details on these two operating modes.

The only functional difference between Timer2 and Timer3 is that Timer2 provides synchronization of the clock prescaler output. This is useful for high-frequency external clock inputs.

32-Bit Timer Mode: In the 32-Bit Timer mode, the timer increments on every instruction cycle up to a match value, preloads into the combined 32-bit Period register, PR3/PR2, then resets to '`0`' and continues to count.

For synchronous 32-bit reads of the Timer2/Timer3 pair, reading the lsw (TMR2 register) will cause the msw to be read and latched into a 16-bit holding register, termed TMR3HLD.

For synchronous 32-bit writes, the holding register (TMR3HLD) must first be written to. When followed by a write to the TMR2 register, the contents of TMR3HLD will be transferred and latched into the MSB of the 32-bit timer (TMR3).

32-Bit Synchronous Counter Mode: In the 32-Bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal, which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in the combined 32-bit Period register, PR3/PR2, then resets to '`0`' and continues.

When the timer is configured for the Synchronous Counter mode of operation and the CPU goes into the Idle mode, the timer will stop incrementing unless the TSIDL (T2CON<13>) bit = `0`. If TSIDL = `1`, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

NOTES:

12.1 Simple Capture Event Mode

The simple capture events in the dsPIC30F product family are:

- Capture every falling edge
- Capture every rising edge
- Capture every 4th rising edge
- Capture every 16th rising edge
- Capture every rising and falling edge

These simple Input Capture modes are configured by setting the appropriate bits, ICM<2:0> (ICxCON<2:0>).

12.1.1 CAPTURE PRESCALER

There are four input capture prescaler settings, specified by bits, ICM<2:0> (ICxCON<2:0>). Whenever the capture channel is turned off, the prescaler counter will be cleared. In addition, any Reset will clear the prescaler counter.

12.1.2 CAPTURE BUFFER OPERATION

Each capture channel has an associated FIFO buffer, which is four 16-bit words deep. There are two status flags, which provide status on the FIFO buffer:

- ICBNE – Input Capture Buffer Not Empty
- ICOV – Input Capture Overflow

The ICBNE will be set on the first input capture event and remain set until all capture events have been read from the FIFO. As each word is read from the FIFO, the remaining words are advanced by one position within the buffer.

In the event that the FIFO is full with four capture events and a fifth capture event occurs prior to a read of the FIFO, an overflow condition will occur and the ICOV bit will be set to a logic ‘`1`’. The fifth capture event is lost and is not stored in the FIFO. No additional events will be captured till all four events have been read from the buffer.

If a FIFO read is performed after the last read and no new capture event has been received, the read will yield indeterminate results.

12.1.3 TIMER2 AND TIMER3 SELECTION MODE

Each capture channel can select between one of two timers for the time base, Timer2 or Timer3.

Selection of the timer resource is accomplished through SFR bit, ICTMR (ICxCON<7>). Timer3 is the default timer resource available for the input capture module.

12.1.4 HALL SENSOR MODE

When the input capture module is set for capture on every edge, rising and falling, ICM<2:0> = `001`, the following operations are performed by the input capture logic:

- The input capture interrupt flag is set on every edge, rising and falling.
- The interrupt on Capture Mode Setting bits, ICI<1:0>, is ignored, since every capture generates an interrupt.
- A capture overflow condition is not generated in this mode.

12.2 Input Capture Operation During Sleep and Idle Modes

An input capture event will generate a device wake-up or interrupt, if enabled, if the device is in CPU Idle or Sleep mode.

Independent of the timer being enabled, the input capture module will wake-up from the CPU Sleep or Idle mode when a capture event occurs if ICM<2:0> = `111` and the interrupt enable bit is asserted. The same wake-up can generate an interrupt if the conditions for processing the interrupt have been satisfied. The wake-up feature is useful as a method of adding extra external pin interrupts.

12.2.1 INPUT CAPTURE IN CPU SLEEP MODE

CPU Sleep mode allows input capture module operation with reduced functionality. In the CPU Sleep mode, the ICI<1:0> bits are not applicable, and the input capture module can only function as an external interrupt source.

The capture module must be configured for interrupt only on the rising edge (ICM<2:0> = `111`) in order for the input capture module to be used while the device is in Sleep mode. The prescale settings of 4:1 or 16:1 are not applicable in this mode.

14.3 Position Measurement Mode

There are two measurement modes which are supported and are termed x2 and x4. These modes are selected by the QEIM<2:0> mode select bits located in SFR, QEICON<10:8>.

When control bits, QEIM<2:0> = `100` or `101`, the x2 Measurement mode is selected and the QEI logic only looks at the Phase A input for the position counter increment rate. Every rising and falling edge of the Phase A signal causes the position counter to be incremented or decremented. The Phase B signal is still utilized for the determination of the counter direction, just as in the x4 Measurement mode.

Within the x2 Measurement mode, there are two variations of how the position counter is reset:

1. Position counter reset by detection of index pulse, QEIM<2:0> = `100`.
2. Position counter reset by match with MAXCNT, QEIM<2:0> = `101`.

When control bits, QEIM<2:0> = `110` or `111`, the x4 Measurement mode is selected and the QEI logic looks at both edges of the Phase A and Phase B input signals. Every edge of both signals causes the position counter to increment or decrement.

Within the x4 Measurement mode, there are two variations of how the position counter is reset:

1. Position counter reset by detection of index pulse, QEIM<2:0> = `110`.
2. Position counter reset by match with MAXCNT, QEIM<2:0> = `111`.

The x4 Measurement mode provides for finer resolution data (more position counts) for determining motor position.

14.4 Programmable Digital Noise Filters

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. Schmitt Trigger inputs and a three-clock cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in noise prone applications, such as a motor system.

The filter ensures that the filtered output signal is not permitted to change until a stable value has been registered for three consecutive clock cycles.

For the QEA, QEB and INDX pins, the clock divide frequency for the digital filter is programmed by bits, QECK<2:0> (DFLTCON<6:4>), and are derived from the base instruction cycle, TCY.

To enable the filter output for channels, QEA, QEB and INDX, the QEOUT bit must be '`1`'. The filter network for all channels is disabled on POR and BOR.

14.5 Alternate 16-Bit Timer/Counter

When the QEI module is not configured for the QEI mode, QEIM<2:0> = `001`, the module can be configured as a simple 16-bit timer/counter. The setup and control of the auxiliary timer is accomplished through the QEICON SFR register. This timer functions identically to Timer1. The QEA pin is used as the timer clock input.

When configured as a timer, the POSCNT register serves as the Timer Count register and the MAXCNT register serves as the Period register. When a Timer/Period register match occurs, the QEI interrupt flag will be asserted.

The only exception between the general purpose timers and this timer is the added feature of external up/down input select. When the UPDN pin is asserted high, the timer will increment up. When the UPDN pin is asserted low, the timer will be decremented.

Note: Changing the operational mode (i.e., from QEI to timer or vice versa), will not affect the Timer/Position Count register contents.

The UPDN control/status bit (QEICON<11>) can be used to select the count direction state of the Timer register. When UPDN = `1`, the timer will count up. When UPDN = `0`, the timer will count down.

In addition, control bit, UPDN_SRC (QEICON<0>), determines whether the timer count direction state is based on the logic state written into the UPDN control/status bit (QEICON<11>), or the QEB pin state. When UPDN_SRC = `1`, the timer count direction is controlled from the QEB pin. Likewise, when UPDN_SRC = `0`, the timer count direction is controlled by the UPDN bit.

Note: This timer does not support the External Asynchronous Counter mode of operation. If using an external clock source, the clock will automatically be synchronized to the internal instruction cycle.

14.6 QEI Module Operation During CPU Sleep Mode

14.6.1 QEI OPERATION DURING CPU SLEEP MODE

The QEI module will be halted during the CPU Sleep mode.

14.6.2 TIMER OPERATION DURING CPU SLEEP MODE

During CPU Sleep mode, the timer will not operate, because the internal clocks are disabled.

17.2 I^{2}C Module Addresses

The I2CADD register contains the Slave mode addresses. The register is a 10-bit register.

If the A10M bit (I2CCON<10>) is ‘`0`’, the address is interpreted by the module as a 7-bit address. When an address is received, it is compared to the 7 LSbs of the I2CADD register.

If the A10M bit is ‘`1`’, the address is assumed to be a 10-bit address. When an address is received, it will be compared with the binary value, ‘`11110 A9 A8`’ (where `A9` and `A8` are two Most Significant bits of I2CADD). If that value matches, the next address will be compared with the Least Significant 8 bits of I2CADD, as specified in the 10-bit addressing protocol.

The 7-bit I^{2}C slave addresses supported by the dsPIC30F are shown in Table 17-1.

TABLE 17-1: 7-BIT I^{2}C™ SLAVE ADDRESSES

Address	Description
0x00	General Call Address or Start Byte
0x01-0x03	Reserved
0x04-0x07	HS mode Master Codes
0x08-0x77	Valid 7-Bit Addresses
0x78-0x7B	Valid 10-Bit Addresses (lower 7 bits)
0x7C-0x7F	Reserved

17.3 I^{2}C 7-Bit Slave Mode Operation

Once enabled (I2CEN = `1`), the slave module will wait for a Start bit to occur (i.e., the I^{2}C module is ‘Idle’). Following the detection of a Start bit, 8 bits are shifted into I2CRSR and the address is compared against I2CADD. In 7-bit mode (A10M = `0`), bits I2CADD<6:0> are compared against I2CRSR<7:1> and I2CRSR<0> is the R_W bit. All incoming bits are sampled on the rising edge of SCL.

If an address match occurs, an Acknowledgement will be sent, and the Slave Event Interrupt Flag (SI2CIF) is set on the falling edge of the ninth (ACK) bit. The address match does not affect the contents of the I2CRCV buffer or the RBF bit.

17.3.1 SLAVE TRANSMISSION

If the R_W bit received is a ‘`1`’, then the serial port will go into Transmit mode. It will send an ACK on the ninth bit and then hold SCL to ‘`0`’ until the CPU responds by writing to I2CTRN. SCL is released by setting the SCLREL bit, and 8 bits of data are shifted out. Data bits are shifted out on the falling edge of SCL, such that SDA is valid during SCL high. The interrupt pulse is sent on the falling edge of the ninth clock pulse, regardless of the status of the ACK received from the master.

17.3.2 SLAVE RECEPTION

If the R_W bit received is a ‘`0`’ during an address match, then Receive mode is initiated. Incoming bits are sampled on the rising edge of SCL. After 8 bits are received, if I2CRCV is not full or I2COV is not set, I2CRSR is transferred to I2CRCV. ACK is sent on the ninth clock.

If the RBF flag is set, indicating that I2CRCV is still holding data from a previous operation (RBF = `1`), then ACK is not sent; however, the interrupt pulse is generated. In the case of an overflow, the contents of the I2CRSR are not loaded into the I2CRCV.

Note: The I2CRCV will be loaded if the I2COV bit = `1` and the RBF flag = `0`. In this case, a read of the I2CRCV was performed, but the user did not clear the state of the I2COV bit before the next receive occurred. The Acknowledgement is not sent (ACK = `1`) and the I2CRCV is updated.

17.4 I^{2}C 10-Bit Slave Mode Operation

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match is more complex.

The I^{2}C specification dictates that a slave must be addressed for a write operation, with two address bytes following a Start bit.

The A10M bit is a control bit that signifies that the address in I2CADD is a 10-bit address rather than a 7-bit address. The address detection protocol for the first byte of a message address is identical for 7-bit and 10-bit messages, but the bits being compared are different.

I2CADD holds the entire 10-bit address. Upon receiving an address following a Start bit, I2CRSR<7:3> is compared against a literal ‘`11110`’ (the default 10-bit address) and I2CRSR<2:1> are compared against I2CADD<9:8>. If a match occurs and if R_W = `0`, the interrupt pulse is sent. The ADD10 bit will be cleared to indicate a partial address match. If a match fails or R_W = `1`, the ADD10 bit is cleared and the module returns to the Idle state.

The low byte of the address is then received and compared with I2CADD<7:0>. If an address match occurs, the interrupt pulse is generated and the ADD10 bit is set, indicating a complete 10-bit address match. If an address match did not occur, the ADD10 bit is cleared and the module returns to the Idle state.

18.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding Interrupt Flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

a) If UTXISEL = `0`, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This implies that the transmit buffer has at least one empty word.

b) If UTXISEL = `1`, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two interrupt modes during operation is possible and sometimes offers more flexibility.

18.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) will cause the UxTX line to be driven to logic ‘`0`’. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a Break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB or starting other transmitter activity. Transmission of a Break character does not generate a transmit interrupt.

18.4 Receiving Data

18.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

1. Set up the UART (see **Section 18.3.1 “Transmitting in 8-Bit Data Mode”** and **Section 18.3.2 “Transmitting in 9-Bit Data Mode”**).
2. Enable the UART (see **Section 18.3.1 “Transmitting in 8-Bit Data Mode”** and **Section 18.3.2 “Transmitting in 9-Bit Data Mode”**).
3. A receive interrupt will be generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read the received data from UxRXREG. The act of reading UxRXREG will move the next word to the top of the receive FIFO, and the PERR and FERR values will be updated.

18.4.2 RECEIVE BUFFER (UxRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = `1` indicates that the receive buffer has data available. URXDA = `0` implies that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer will be read and no data shift will occur within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a power-saving mode.

18.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding Interrupt Flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

a) If URXISEL<1:0> = `00` or `01`, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.

b) If URXISEL<1:0> = `10`, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which, as a result of the transfer, contains 3 characters.

c) If URXISEL<1:0> = `11`, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which, as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

18.5 Reception Error Handling

18.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

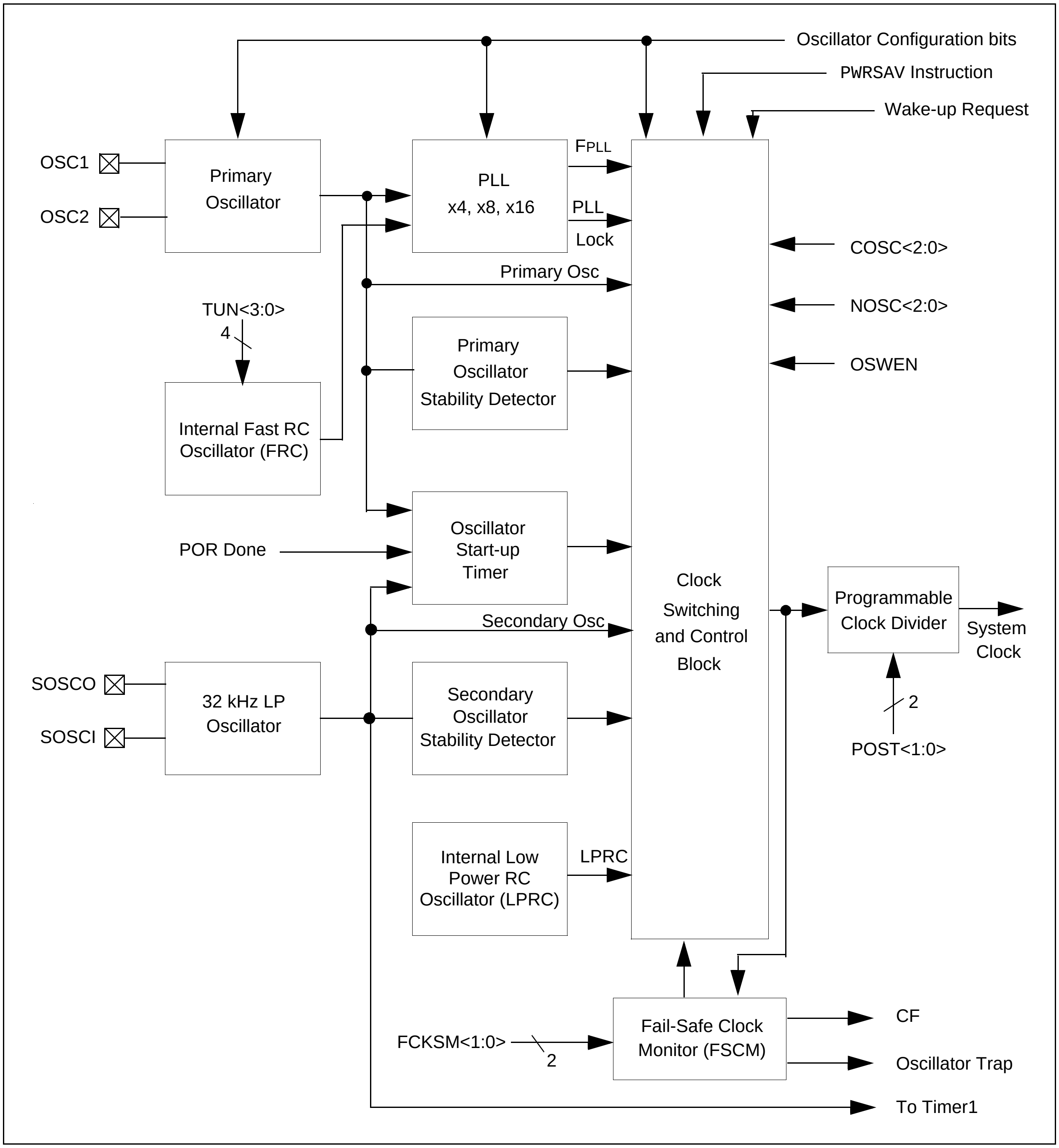
a) The receive buffer is full.

b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.

c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

FIGURE 20-1: OSCILLATOR SYSTEM BLOCK DIAGRAM



23.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC30F electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

For detailed information about the dsPIC30F architecture and core, refer to the *“dsPIC30F Family Reference Manual”* (DS70046).

Absolute maximum ratings for the dsPIC30F family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{\text{MCLR}}$) **(Note 1)**	-0.3V to (V_{DD} + 0.3V)
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +5.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V_{SS}	0V to +13.25V
Maximum current out of V_{SS} pin	300 mA
Maximum current into V_{DD} pin **(Note 2)**	250 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports **(Note 2)**	200 mA

Note 1: Voltage spikes below Vss at the $\overline{\text{MCLR}}$/V_{PP} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$/V_{PP} pin, rather than pulling this pin directly to Vss.

2: Maximum allowable current is a function of device maximum power dissipation. See Table 23-2.

†**NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

23.1 DC Characteristics

TABLE 23-1: OPERATING MIPS VS. VOLTAGE

V_{DD} Range	Temp Range	Max MIPS	
		dsPIC30F301X-30I	**dsPIC30F301X-20E**
4.5-5.5V	-40°C to 85°C	30	—
4.5-5.5V	-40°C to 125°C	—	20
3.0-3.6V	-40°C to 85°C	20	—
3.0-3.6V	-40°C to 125°C	—	15
2.5-3.0V	-40°C to 85°C	10	—

TABLE 23-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
dsPIC30F301X-30I					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
dsPIC30F301X-20E					
Operating Junction Temperature Range	T_J	-40	—	+150	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma\ I_{OH})$ I/O Pin power dissipation: $P_{I/O} = \Sigma\ (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 23-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 28-pin SPDIP (SP)	θ_{JA}	42	—	°C/W	**1**
Package Thermal Resistance, 28-pin SOIC (SO)	θ_{JA}	49	—	°C/W	**1**
Package Thermal Resistance, 40-pin PDIP (P)	θ_{JA}	37	—	°C/W	**1**
Package Thermal Resistance, 44-pin TQFP (PT, 10x10x1 mm)	θ_{JA}	45	—	°C/W	**1**
Package Thermal Resistance, 44-pin QFN (ML)	θ_{JA}	28	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-ja (θ_{JA}) numbers are achieved by package simulations.

23.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC30F AC characteristics and timing parameters.

TABLE 23-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 2.5V to 5.5V** **(unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Operating voltage V_{DD} range as described in **Section 23.1 "DC Characteristics"**.

FIGURE 23-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

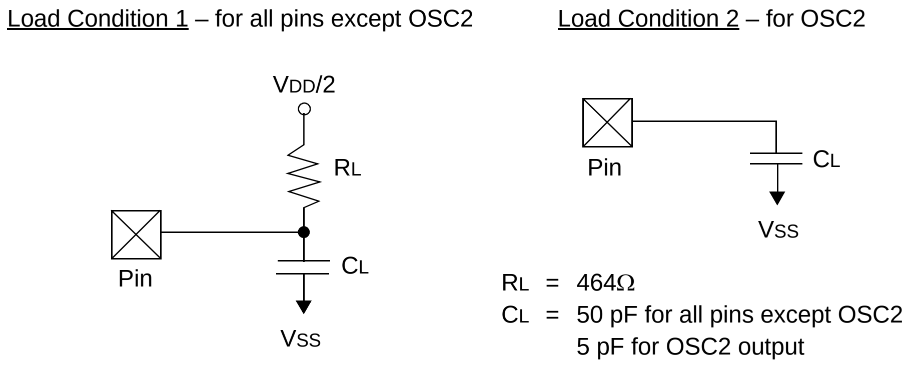
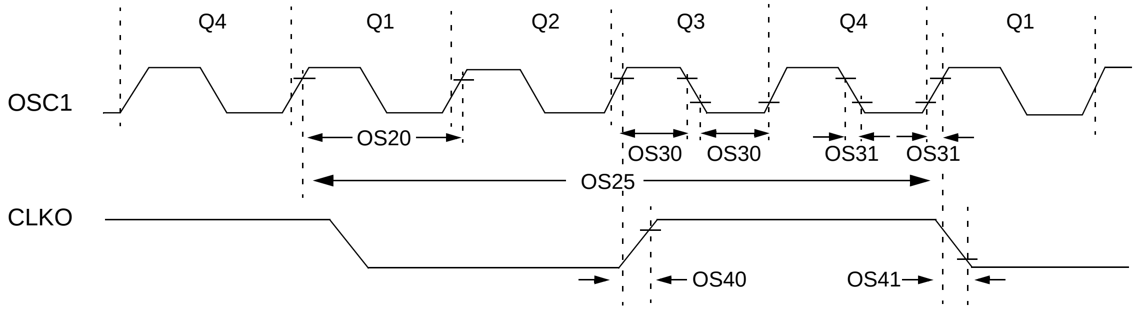


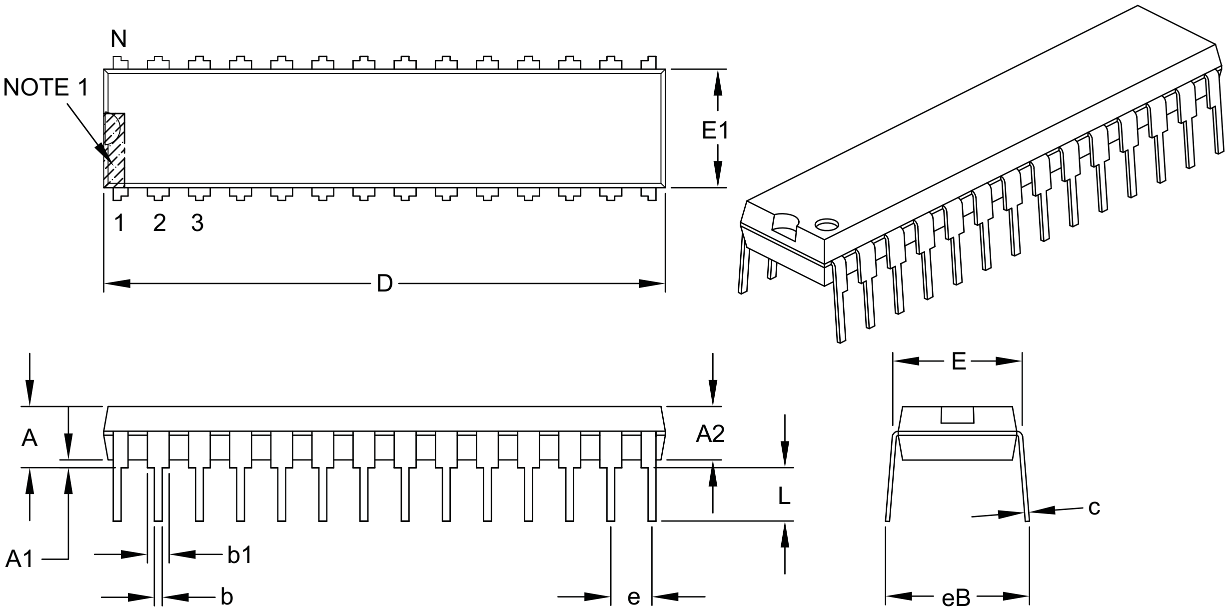
FIGURE 23-3: EXTERNAL CLOCK TIMING



24.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

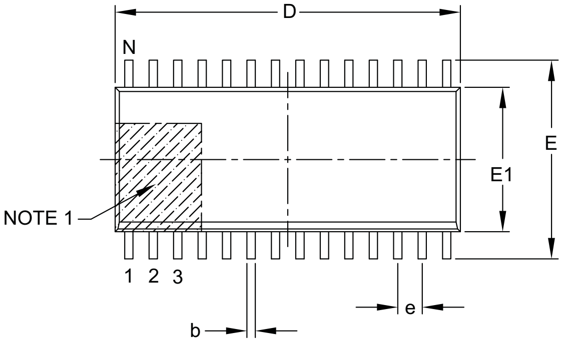
Notes:

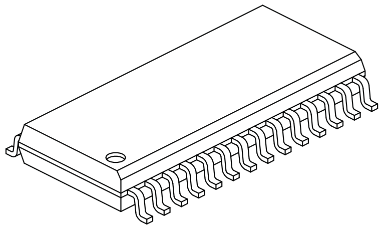
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

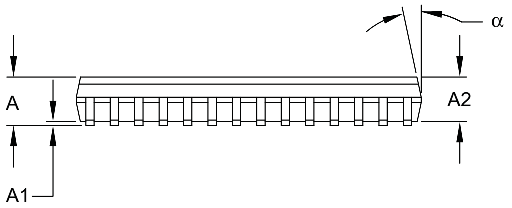
Microchip Technology Drawing C04-070B

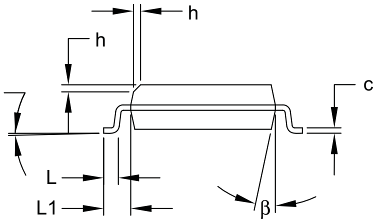
28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	ϕ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

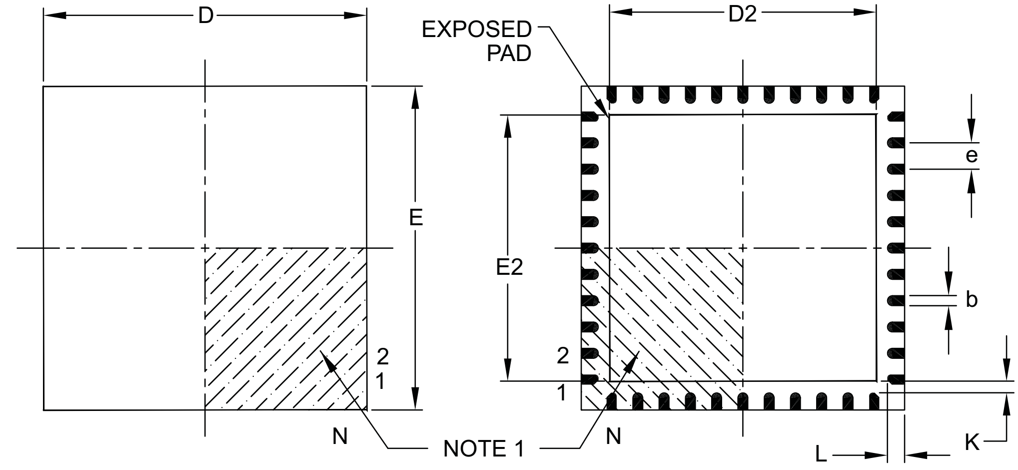
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

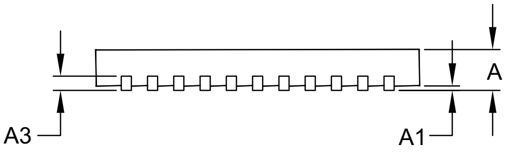
Microchip Technology Drawing C04-052B

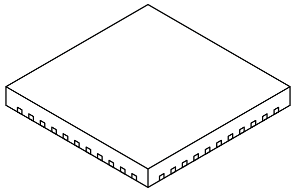
44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B