Infineon Technologies - SAF-XC164GM-16F20F BA Datasheet

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Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164gm-16f20f-ba

XC164GM
Revision History: V1.2, 2007-03

Previous Version(s):
V1.1, 2006-08
V1.0, 2005-11

Page	Subjects (major changes since last revision)
6	Design steps of the derivatives differentiated.
52	Power consumption of the derivatives differentiated.
53	Figure 10 adapted.
54	Figure 12 adapted.
64	Packages of the derivatives differentiated.
65	Thermal resistances of the derivatives differentiated.
all	“Preliminary” removed

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Table 1 XC164GM Derivative Synopsis

Derivative[1)]	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAF-XC164GM-16F40F SAF-XC164GM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164GM-8F40F SAF-XC164GM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164GM-4F40F SAF-XC164GM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1

1) This Data Sheet is valid for:
devices starting with and including design step BA for the -16F derivatives, and for devices starting with and including design step AA for -4F/8F derivatives.

2 General Device Information

The XC164GM derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.

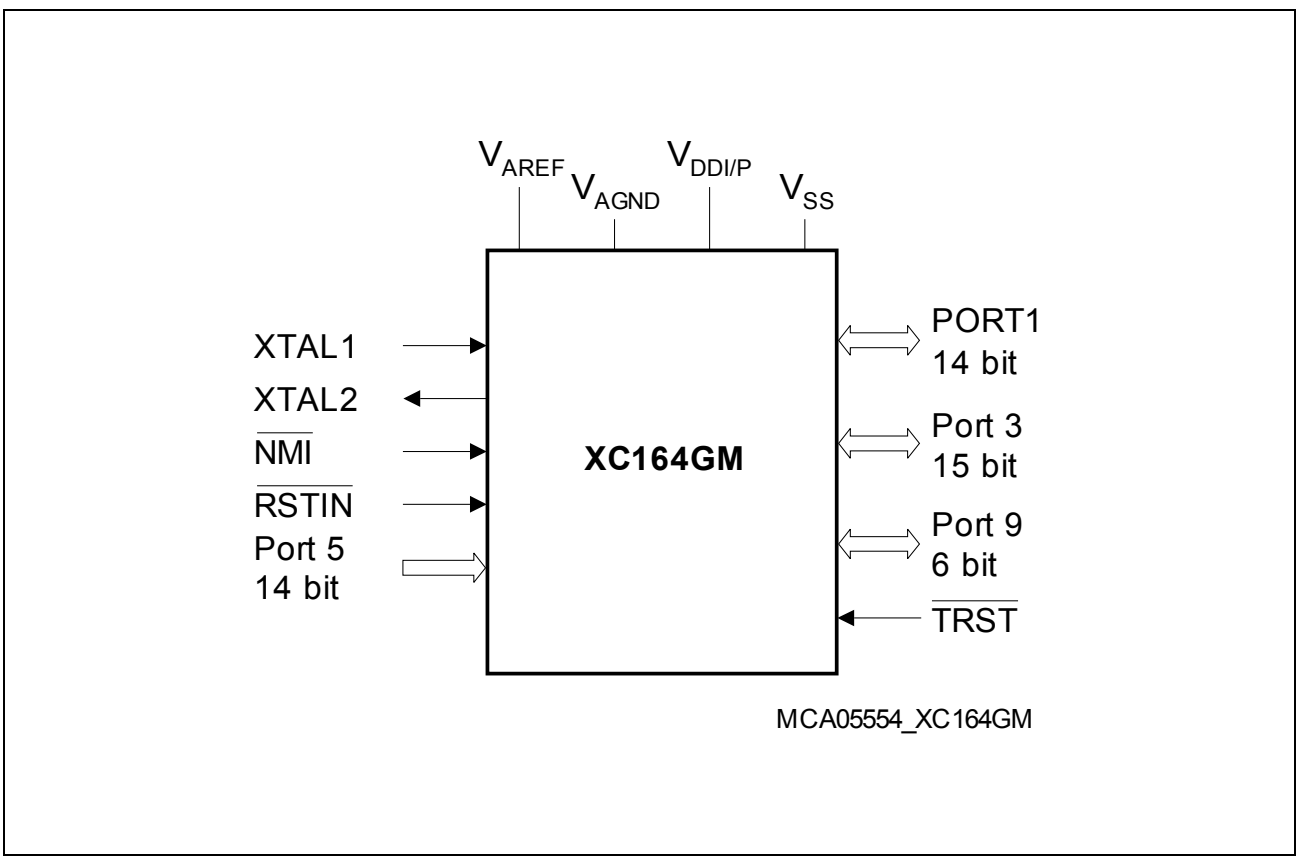

Figure 1 Logic Symbol

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
Port 5	9-18, 21-24	I	Port 5 is a 14-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	9	I	AN0
P5.1	10	I	AN1
P5.2	11	I	AN2
P5.3	12	I	AN3
P5.4	13	I	AN4
P5.5	14	I	AN5
P5.10	15	I	AN10 (T6EUD): GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	16	I	AN11 (T5EUD): GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.6	17	I	AN6
P5.7	18	I	AN7
P5.12	21	I	AN12 (T6IN): GPT2 Timer T6 Count/Gate Input
P5.13	22	I	AN13 (T5IN): GPT2 Timer T5 Count/Gate Input
P5.14	23	I	AN14 (T4EUD): GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	24	I	AN15 (T2EUD): GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.
$\overline{\text{TRST}}$	62	I	Test-System Reset Input. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{RSTIN}}$ enables the hardware configuration and activates the XC164GM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.

Table 4 XC164GM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$

Table 4 XC164GM Interrupt Nodes (cont'd)

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ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
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CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$

register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC164GM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

3.13 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled until the EINIT instruction has been executed (compatible mode), or it can be disabled and enabled at any time by executing instructions DISWDT and ENWDT (enhanced mode). Thus, the chip's start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded and the low byte is cleared. Thus, time intervals between 13 µs and 419 ms can be monitored (@ 40 MHz).
The default Watchdog Timer interval after reset is 3.28 ms (@ 40 MHz).

3.14 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC164GM with high flexibility. The master clock f_{MC} is the reference clock signal, and is used for TwinCAN and is output to the external system. The CPU clock f_{CPU} and the system clock f_{SYS} are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also **Section 4.4.1**.

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock/OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

The oscillator watchdog can be disabled by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

3.16 Power Management

The XC164GM provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC164GM into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC164GM's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC164GM by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164GM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)3)
Supply Voltage Difference	$'V_{DD}$	-0.5	–	V	$V_{DDP} - V_{DDI}$ 4)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 5)6)
		-2	5	mA	Per analog input pin 5)6)
Overload current coupling factor for analog inputs 7)	K_{OVA}	–	$1.0\ u10^{-4}$	–	$I_{OV} > 0$
		–	$1.5\ u10^{-3}$	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins 7)	K_{OVD}	–	$5.0\ u10^{-3}$	–	$I_{OV} > 0$
		–	$1.0\ u10^{-2}$	–	$I_{OV} < 0$
Absolute sum of overload currents	$6\|I_{OV}\|$	–	50	mA	6)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 8)
Ambient temperature	T_A	0	70	6C	SAB-XC164…
		-40	85	6C	SAF-XC164…
		-40	125	6C	SAK-XC164…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

4.2 DC Parameters

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V_{IL}	SR	-0.5	0.2 uV_{DDP} - 0.1	V	–
Input low voltage XTAL1[2)]	V_{ILC}	SR	-0.5	0.3 uV_{DDI}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	0.45 u V_{DDP}	V	[3)]
Input high voltage TTL (all except XTAL1)	V_{IH}	SR	0.2 uV_{DDP} + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1[2)]	V_{IHC}	SR	0.7 uV_{DDI}	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 uV_{DDP} - 0.2	V_{DDP} + 0.5	V	[3)]
Input Hysteresis (Special Threshold)	HYS		0.04 u V_{DDP}	–	V	V_{DDP} in [V], Series resistance = 0 : [3)]
Output low voltage	V_{OL}	CC	–	1.0	V	I_{OL} dI$_{OLmax}$[4)]
			–	0.45	V	I_{OL} dI$_{OLnom}$[4)5)]
Output high voltage[6)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	I_{OH} t I$_{OHmax}$[4)]
			V_{DDP} - 0.45	–	V	I_{OH} t I$_{OHnom}$[4)5)]
Input leakage current (Port 5)[7)]	I_{OZ1}	CC	–	r300	nA	0 V < V_{IN} < V_{DDP}, T_A d125 °C
				r200	nA	0 V < V_{IN} < V_{DDP}, T_A d85 °C[12)]
Input leakage current (all other[8)])[7)]	I_{OZ2}	CC	–	r500	nA	0.45 V < V_{IN} < V_{DDP}
Configuration pull-up current[9)]	I_{CPUH}[10)]		–	-10	µA	V_{IN} = V_{IHmin}
	I_{CPUL}[11)]		-100	–	µA	V_{IN} = V_{ILmax}

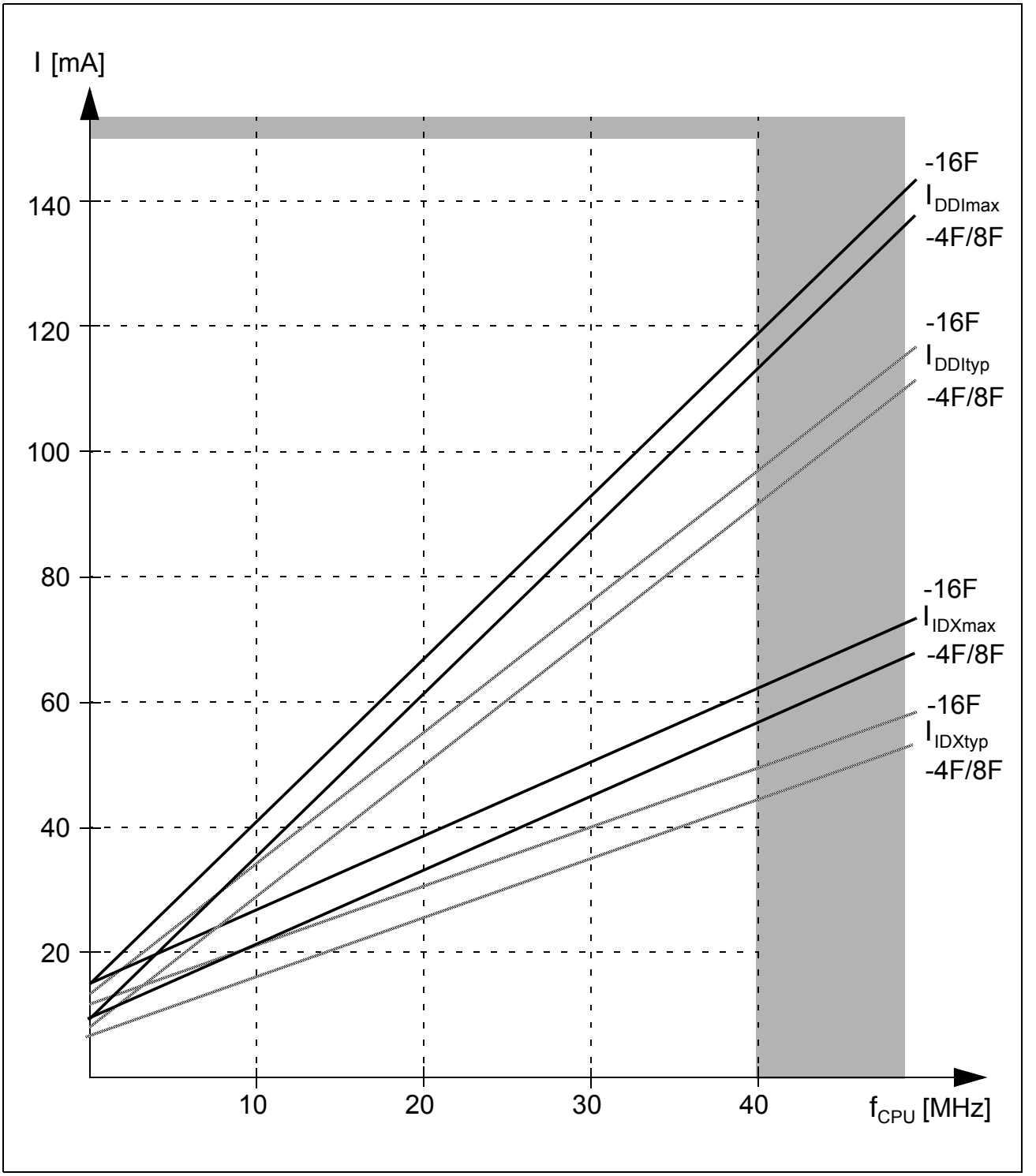

Figure 10 Supply/Idle Current as a Function of Operating Frequency

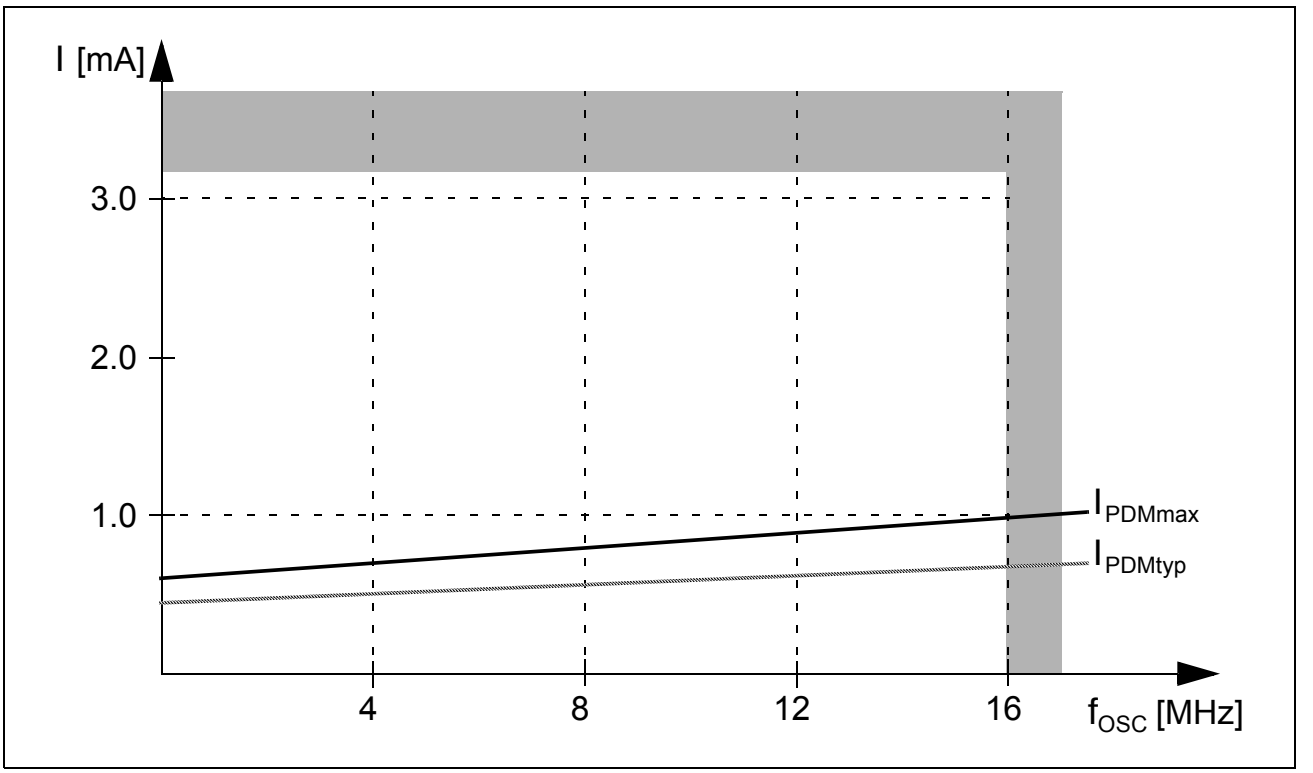

Figure 11 **Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency**

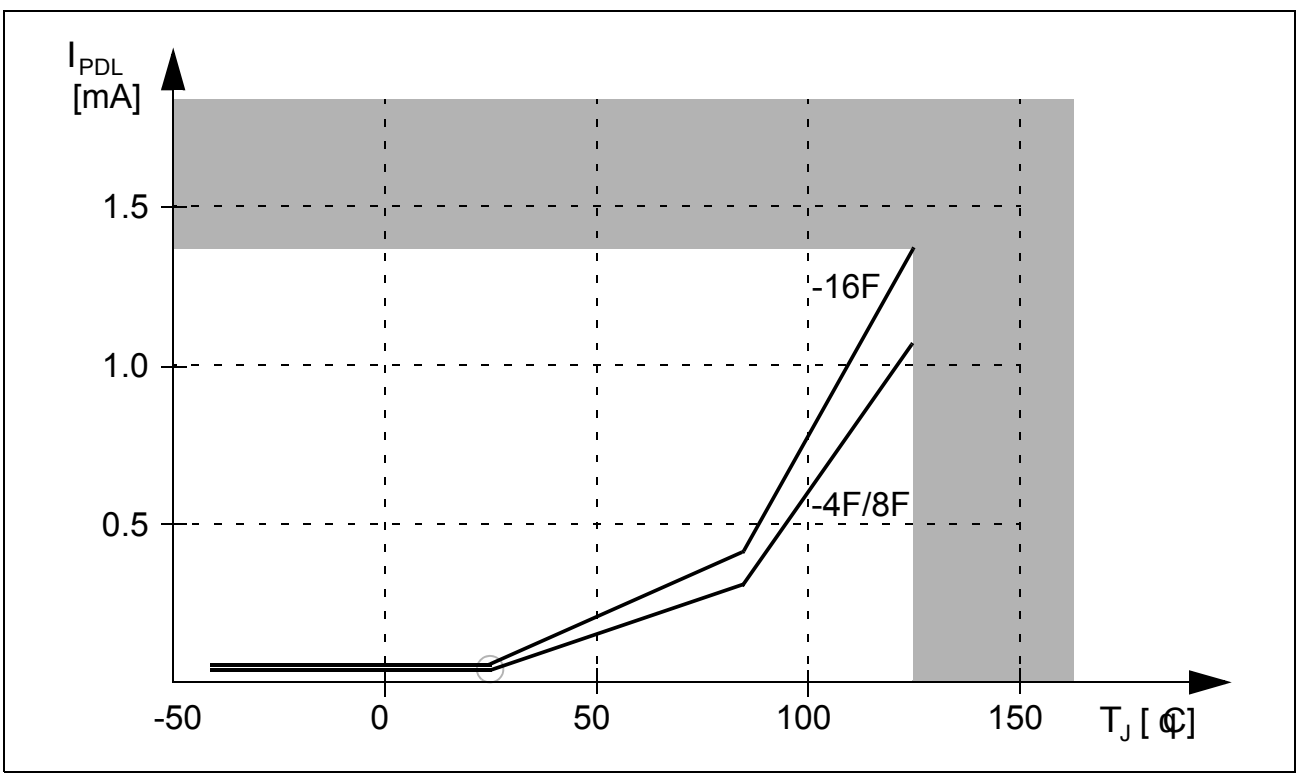

Figure 12 **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

4.3 Analog/Digital Converter Parameters

These parameters describe how the optimum ADC performance can be reached.

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	52 ut_{BC} + t_S + 6 ut_{SYS}		–	Post-calibr. on
	t_{C10}	CC	40 ut_{BC} + t_S + 6 ut_{SYS}		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	44 ut_{BC} + t_S + 6 ut_{SYS}		–	Post-calibr. on
	t_{C8}	CC	32 ut_{BC} + t_S + 6 ut_{SYS}		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	r2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	k :	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	k :	6)

1) TUE is tested at V_{AREF} = V_{DDP} + 0.1 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (i.e. V_{AREF} t 4.0 V) or exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DDP} + 0.2 V) the maximum TUE is increased to r3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be r4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result ($t_{SYS} = 1/f_{SYS}$).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 ut_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 k : , $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 k : .

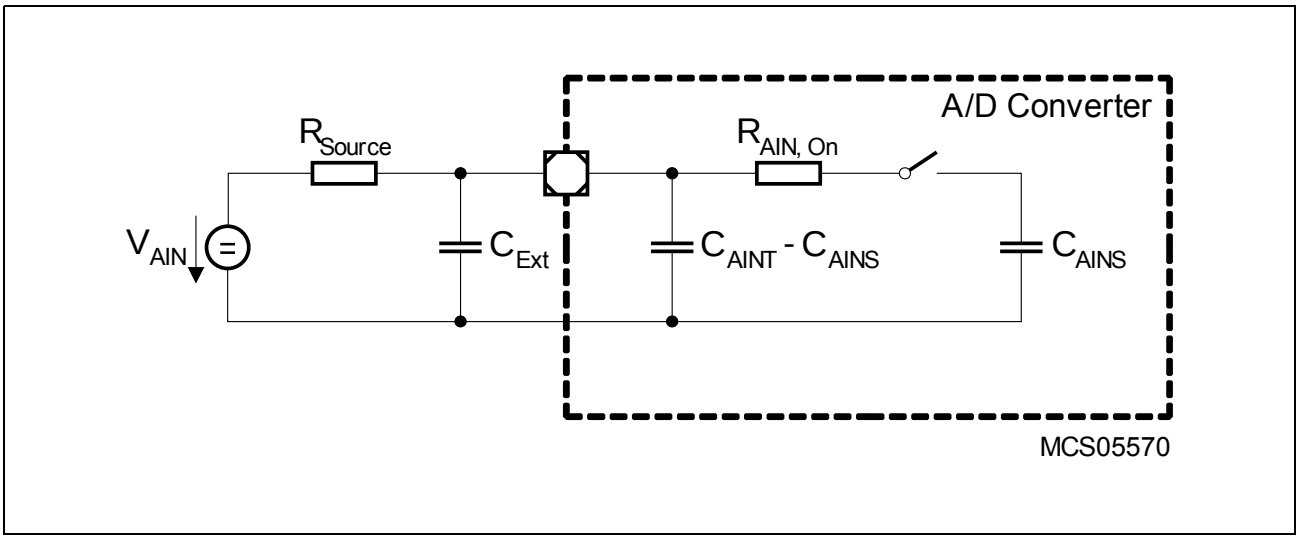

Figure 13 Equivalent Circuitry for Analog Inputs

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 16 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.