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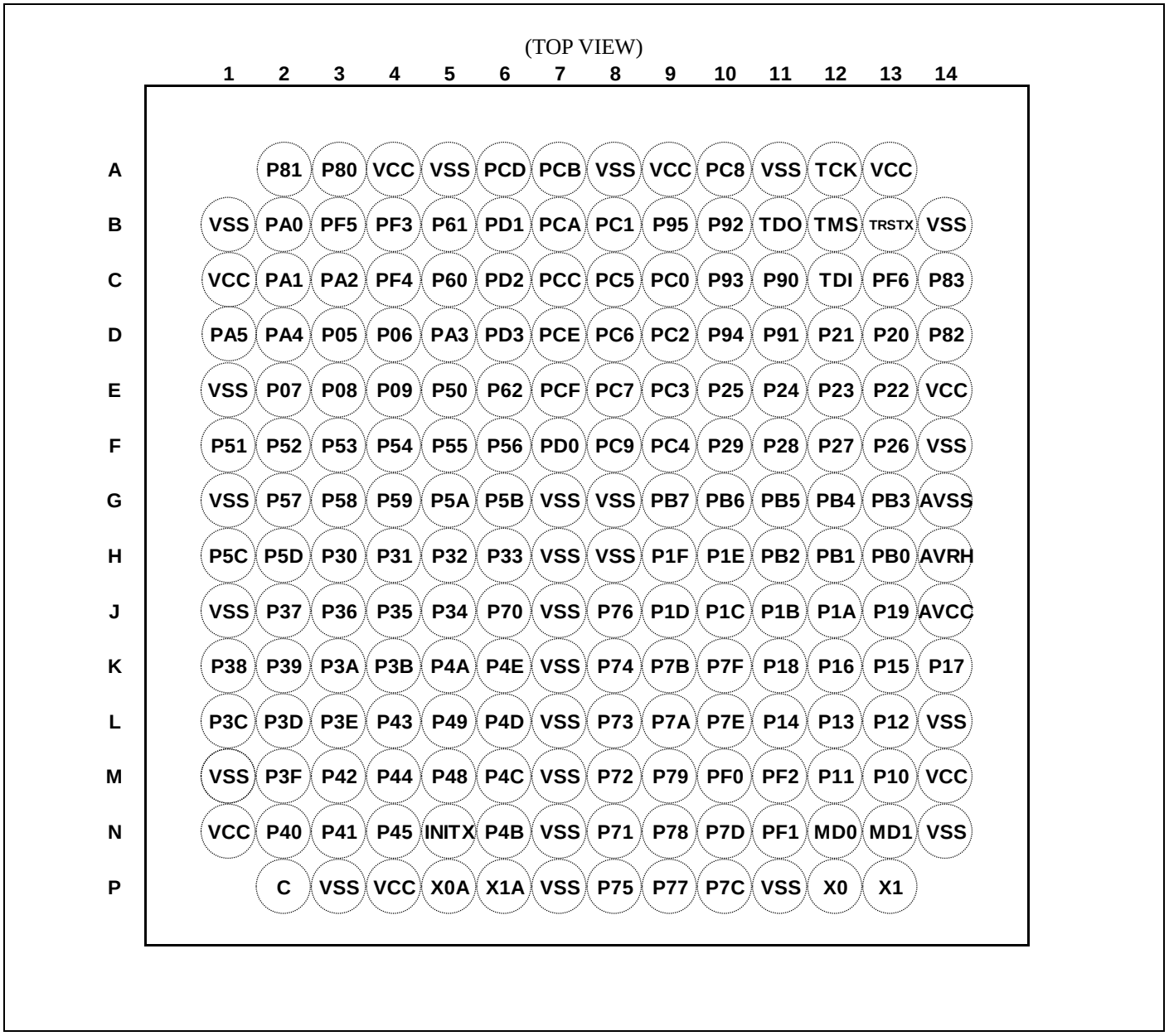
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf416spmc-gk7e1

BGA-192P-M06



Note

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

TIOA09_0, TIOA09_1, and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "●Base Timer" in "■Handling Devices" for details.

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
67	59	M8	P72 SIN2_0 INT14_2 AIN2_0 MADATA07_0	E	H
68	60	L8	P73 SOT2_0 INT15_2 BIN2_0 MADATA08_0	E	H
69	61	K8	P74 SCK2_0 ZIN2_0 MADATA09_0	E	I
70	62	P8	P75 SIN3_0 ADTG_8 INT07_1 MADATA10_0	E	H
71	63	J8	P76 SOT3_0 TIOA07_2 INT11_2 MADATA11_0	E	H
72	64	P9	P77 SCK3_0 TIOB07_2 INT12_2 MADATA12_0	E	H
73	65	N9	P78 AIN1_0 TIOA15_0 MADATA13_0	E	I
74	66	M9	P79 BIN1_0 TIOB15_0 INT23_1 MADATA14_0	E	H
-	-	E1	VSS	-	
-	-	G1	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
124	100	E12	P23 AN30 SCK0_0 TIOA07_1 RTO00_1	F	K
125	101	E13	P22 AN31 SOT0_0 TIOB07_1 ZIN1_1	F	K
126	102	D12	P21 SIN0_0 INT06_1 BIN1_1	E	H
127	103	D13	P20 INT05_0 CROUT_0 AIN1_1 MAD18_0	E	H
128	104	C13	PF6 FRCK2_0 NMIX	I*	J
129	105	E14	VCC	-	
130	106	D14	P82	H	O
131	107	C14	P83	H	O
132	108	B14	VSS	-	
133	109	A13	VCC	-	
134	110	B13	P00 TRSTX	E	E
135	111	A12	P01 TCK SWCLK	E	E
136	112	C12	P02 TDI	E	E
137	113	B12	P03 TMS SWDIO	E	E
138	114	B11	P04 TDO SWO	E	E
139	-	C11	P90 TIOB08_0 RTO20_1 INT30_0 MAD19_0	E	H
-	-	A8	VSS	-	

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT00_0	External interrupt request 00 input pin	13	13	E5
	INT00_1		8	8	D3
	INT00_2		165	135	C6
	INT01_0	External interrupt request 01 input pin	14	14	F1
	INT01_1		9	9	D4
	INT01_2		123	99	E11
	INT02_0	External interrupt request 02 input pin	15	15	F2
	INT02_1		91	75	M12
	INT02_2		120	96	F12
	INT03_0	External interrupt request 03 input pin	6	6	D2
	INT03_1		94	78	L11
	INT03_2		28	-	H3
	INT04_0	External interrupt request 04 input pin	31	-	H6
	INT04_1		97	81	K14
	INT04_2		29	-	H4
	INT05_0	External interrupt request 05 input pin	127	103	D13
	INT05_1		100	84	J12
	INT05_2		30	-	H5
	INT06_0	External interrupt request 06 input pin	170	-	B4
	INT06_1		126	102	D12
	INT06_2		64	56	K6
	INT07_0	External interrupt request 07 input pin	171	-	C4
	INT07_1		70	62	P8
	INT07_2		16	16	F3
	INT08_0	External interrupt request 08 input pin	172	140	B3
	INT08_1		33	-	J4
	INT08_2		19	19	F6
	INT09_0	External interrupt request 09 input pin	119	95	F11
	INT09_1		34	26	J3
	INT09_2		22	22	G4
	INT10_0	External interrupt request 10 input pin	76	-	K9
	INT10_1		35	27	J2
	INT10_2		7	7	D1
	INT11_0	External interrupt request 11 input pin	77	-	P10
	INT11_1		36	28	K1
	INT11_2		71	63	J8
	INT12_0	External interrupt request 12 input pin	78	-	N10
	INT12_1		46	38	N2
	INT12_2		72	64	P9
	INT13_0	External interrupt request 13 input pin	81	-	M10
	INT13_1		47	39	N3
	INT13_2		66	58	N8
	INT14_0	External interrupt request 14 input pin	82	-	N11
	INT14_1		58	50	M5
	INT14_2		67	59	M8

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P60	General-purpose I/O port 6	169	139	C5
	P61		168	138	B5
	P62		167	137	E6
	P70	General-purpose I/O port 7	65	57	J6
	P71		66	58	N8
	P72		67	59	M8
	P73		68	60	L8
	P74		69	61	K8
	P75		70	62	P8
	P76		71	63	J8
	P77		72	64	P9
	P78		73	65	N9
	P79		74	66	M9
	P7A		75	67	L9
	P7B		76	-	K9
	P7C		77	-	P10
	P7D		78	-	N10
	P7E		79	-	L10
	P7F		80	-	K10
	P80	General-purpose I/O port 8	174	142	A3
	P81		175	143	A2
	P82		130	106	D14
	P83		131	107	C14
	P90	General-purpose I/O port 9	139	-	C11
	P91		140	-	D11
	P92		141	-	B10
	P93		142	-	C10
	P94		143	-	D10
	P95		144	-	B9
	PA0	General-purpose I/O port A	2	2	B2
	PA1		3	3	C2
	PA2		4	4	C3
	PA3		5	5	D5
	PA4		6	6	D2
	PA5		7	7	D1
	PB0	General-purpose I/O port B	110	-	H13
	PB1		111	-	H12
	PB2		112	-	H11
	PB3		113	-	G13
	PB4		114	-	G12
	PB5		115	-	G11
	PB6		116	-	G10
	PB7		117	-	G9

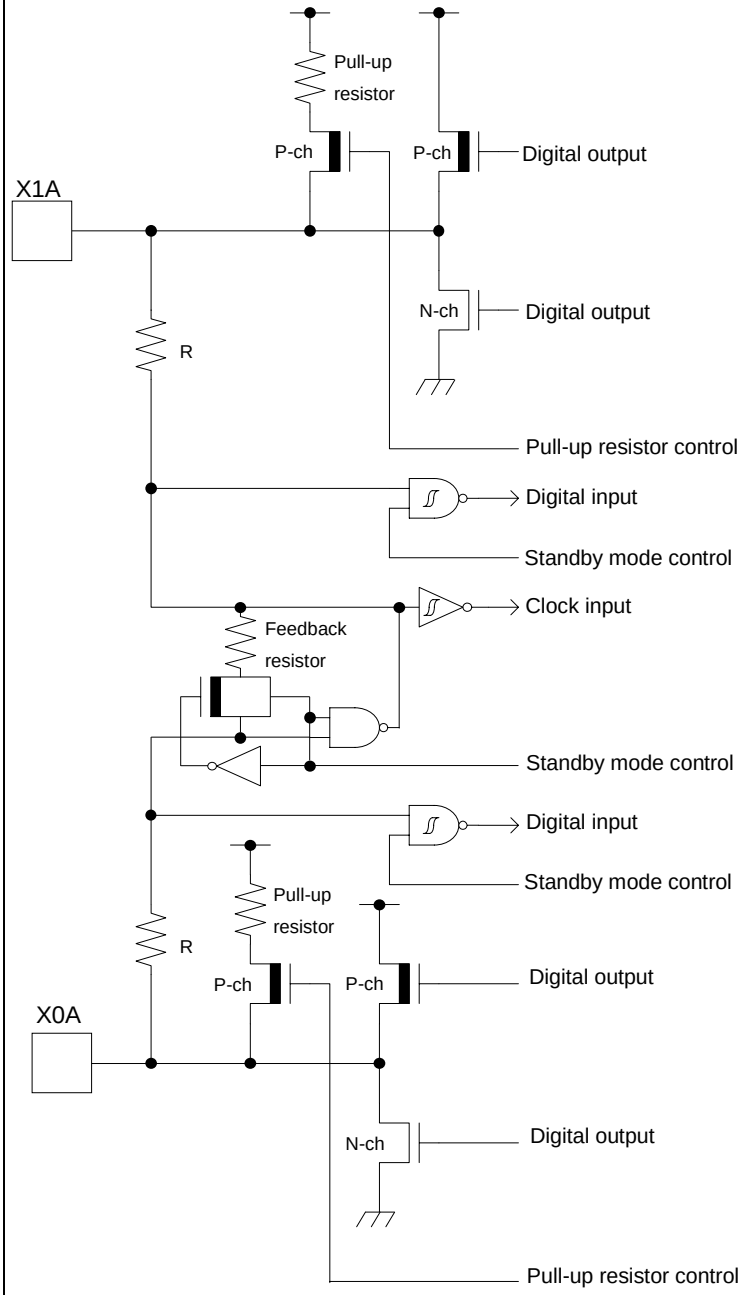
Module	Pin name	Function	Pin no		
			LQFP-176	LQFP-144	BGA-192
GPIO	PC0	General-purpose I/O port C	145	115	C9
	PC1		146	116	B8
	PC2		147	117	D9
	PC3		148	118	E9
	PC4		149	119	F9
	PC5		150	120	C8
	PC6		151	121	D8
	PC7		152	122	E8
	PC8		153	123	A10
	PC9		154	124	F8
	PCA		155	125	B7
	PCB		158	128	A7
	PCC		159	129	C7
	PCD		160	130	A6
	PCE		161	131	D7
	PCF		162	132	E7
	PD0	General-purpose I/O port D	163	133	F7
	PD1		164	134	B6
	PD2		165	135	C6
	PD3		166	136	D6
	PE0	General-purpose I/O port E	84	68	N13
	PE2		86	70	P12
	PE3		87	71	P13
	PF0	General-purpose I/O port F*	81	-	M10
	PF1		82	-	N11
	PF2		83	-	M11
	PF3		170	-	B4
	PF4		171	-	C4
	PF5		172	140	B3
	PF6		128	104	C13

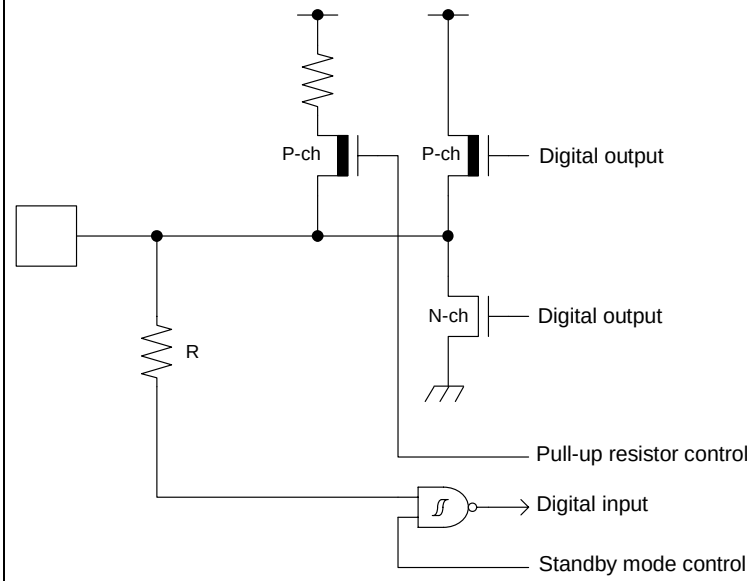
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	37	29	K2
	DTTI0X_1		104	88	H10
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	32	-	J5
	FRCK0_1		105	89	H9
	FRCK0_2		91	75	M12
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0 ICxx describes channel number.	36	28	K1
	IC00_1		100	84	J12
	IC00_2		92	76	L13
	IC01_0		35	27	J2
	IC01_1		101	85	J11
	IC01_2		93	77	L12
	IC02_0		34	26	J3
	IC02_1		102	86	J10
	IC02_2		94	78	L11
	IC03_0		33	-	J4
	IC03_1		103	87	J9
	IC03_2		95	79	K13
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG0 output modes.	38	30	K3
	RTO00_1 (PPG00_1)		124	100	E12
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG0 output modes.	39	31	K4
	RTO01_1 (PPG00_1)		123	99	E11
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG0 output modes.	40	32	L1
	RTO02_1 (PPG02_1)		122	98	E10
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG0 output modes.	41	33	L2
	RTO03_1 (PPG02_1)		121	97	F13
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG0 output modes.	42	34	L3
	RTO04_1 (PPG04_1)		120	96	F12
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG0 output modes.	43	35	M2
	RTO05_1 (PPG04_1)		119	95	F11

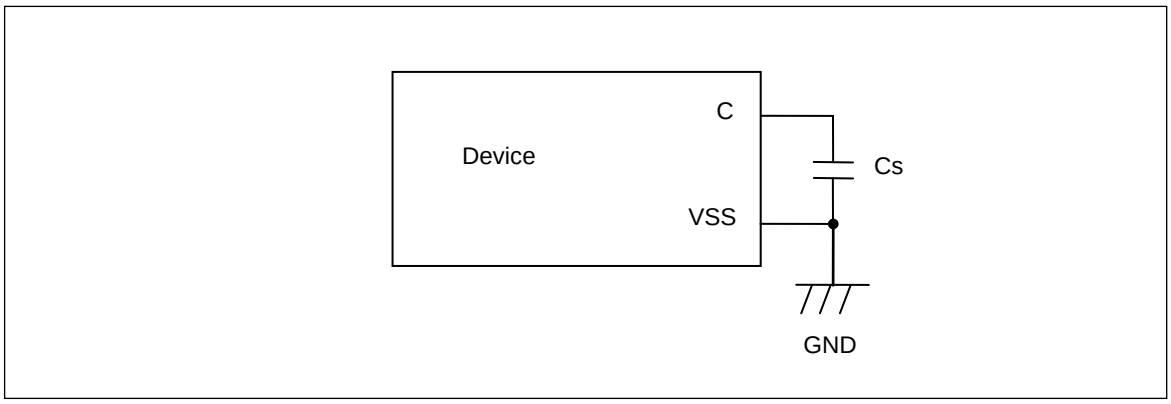
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
RESET	INITX	External Reset Input. A reset is valid when INITX="L".	57	49	N5
Mode	MD0	Mode 0 Pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	85	69	N12
	MD1	Mode 1 Pin. During serial programming to Flash memory, MD1="L" must be input.	84	68	N13
POWER	VCC	Power supply Pin	1	1	C1
	VCC	Power supply Pin	45	37	N1
	VCC	Power supply Pin	54	46	P4
	VCC	Power supply Pin	89	73	M14
	VCC	Power supply Pin	133	109	A13
	VCC	Power supply Pin	173	141	A4
	VCC	Power supply Pin	129	105	E14
	VCC	Power supply Pin	156	126	A9
GND	VSS	GND Pin	27	25	J1
	VSS	GND Pin	44	36	M1
	VSS	GND Pin	53	45	P3
	VSS	GND Pin	88	72	N14
	VSS	GND Pin	109	93	F14
	VSS	GND Pin	132	108	B14
	VSS	GND Pin	157	127	A11
	VSS	GND Pin	176	144	B1
	VSS	GND Pin	-	-	E1
	VSS	GND Pin	-	-	G1
	VSS	GND Pin	-	-	P7
	VSS	GND Pin	-	-	P11
	VSS	GND Pin	-	-	L14
	VSS	GND Pin	-	-	A8
	VSS	GND Pin	-	-	A5
	VSS	GND Pin	-	-	N7
	VSS	GND Pin	-	-	M7
	VSS	GND Pin	-	-	L7
	VSS	GND Pin	-	-	K7
	VSS	GND Pin	-	-	J7
	VSS	GND Pin	-	-	G7
	VSS	GND Pin	-	-	H7
	VSS	GND Pin	-	-	H8
	VSS	GND Pin	-	-	G8

Module	Pin name	Function	Pin No.		
			LQFP-176	LQFP-144	BGA-192
CLOCK	X0	Main clock (oscillation) input pin	86	70	P12
	X0A	Sub clock (oscillation) input pin	55	47	P5
	X1	Main clock (oscillation) I/O pin	87	71	P13
	X1A	Sub clock (oscillation) I/O pin	56	48	P6
	CROUT_0	Built-in high-speed CR-osc clock output port	127	103	D13
	CROUT_1		152	122	E8
Analog POWER	AVCC	A/D converter analog power pin	106	90	J14
	AVRH	A/D converter analog reference voltage input pin	107	91	H14
Analog GND	AVSS	A/D converter GND pin	108	92	G14
C pin	C	Power stabilization capacity pin	52	44	P2

*: 5 V tolerant I/O

Type	Circuit	Remarks
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ■ Oscillation feedback resistor : Approximately 5 MΩ ■ With Standby mode control When the GPIO is selected. ■ CMOS level output. ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor : Approximately 50 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
L		■ CMOS level output ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor : Approximately 50 kΩ ■ I_{OH} = -8 mA, I_{OL}= 8 mA ■ When this pin is used as an I2C pin, the digital output P-ch transistor is always off ■ +B input is available



■**Mode pins (MD0)**
Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

■**Notes on power-on**
Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC =VCC and AVSS = VSS.

Turning on :VCC → AVCC → AVRH
Turning off : AVRH → AVCC → VCC

■**Serial Communication**
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

■**Differences in features among the products with different memory sizes and between Flash products and MASK products**
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■**Base Timer**
In the case of using ch.8 and ch.9 at I/O mode 1 (timer full mode), the TIOA09 pin cannot be used for external startup trigger input (TGIN).
Be sure to use the pin with making ESG1 and ESG2 bits of the Timer Control Register (Ch.9-TMCR) in the Base Timer to be "0b00" in order to disable trigger input.

List of Pin Status

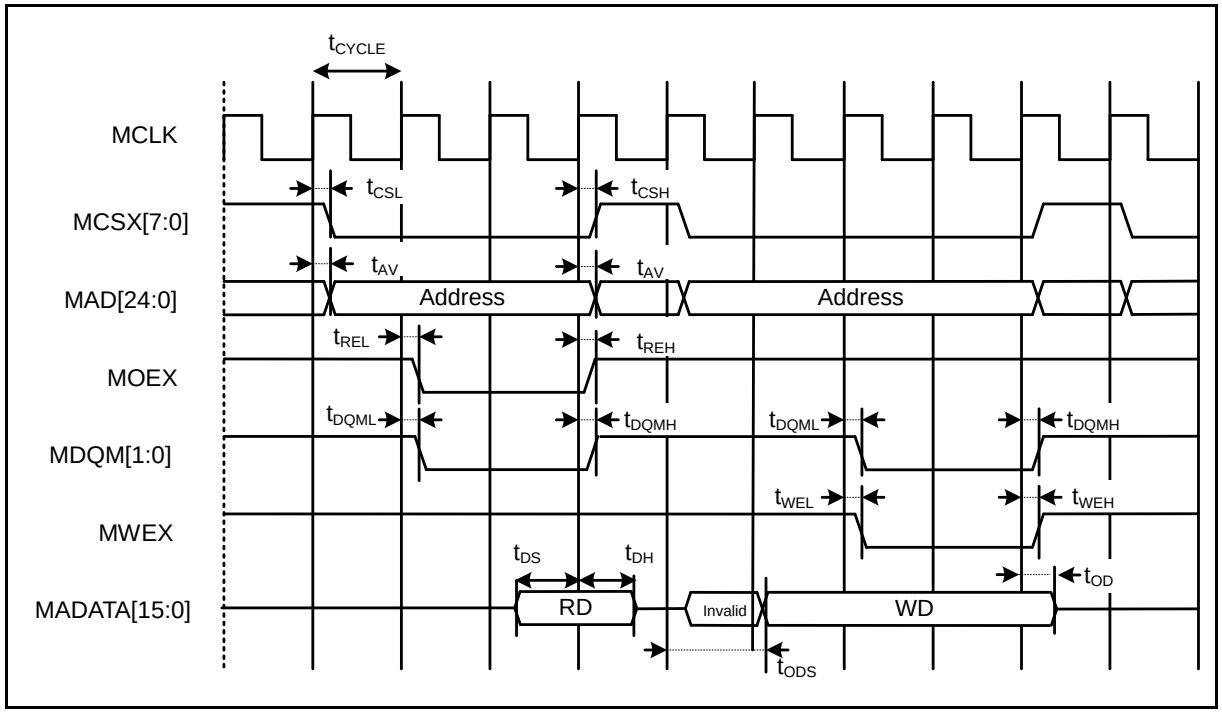
Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or stop mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

■Separate Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{CSH}		Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{REH}		Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	Vcc ≧ 4.5 V	19	-	ns
			Vcc < 4.5 V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	Vcc ≧ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX delay time	t_{WEL}	MCLK, MWEX	Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{WEH}		Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{DQMH}		Vcc ≧ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCLK ↑ → Data output time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≧ 4.5 V	MCLK+1	MCLK+18	ns
			Vcc < 4.5 V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≧ 4.5 V	1	18	ns
			Vcc < 4.5 V		24	

Note: When the external load capacitance = 30 pF.

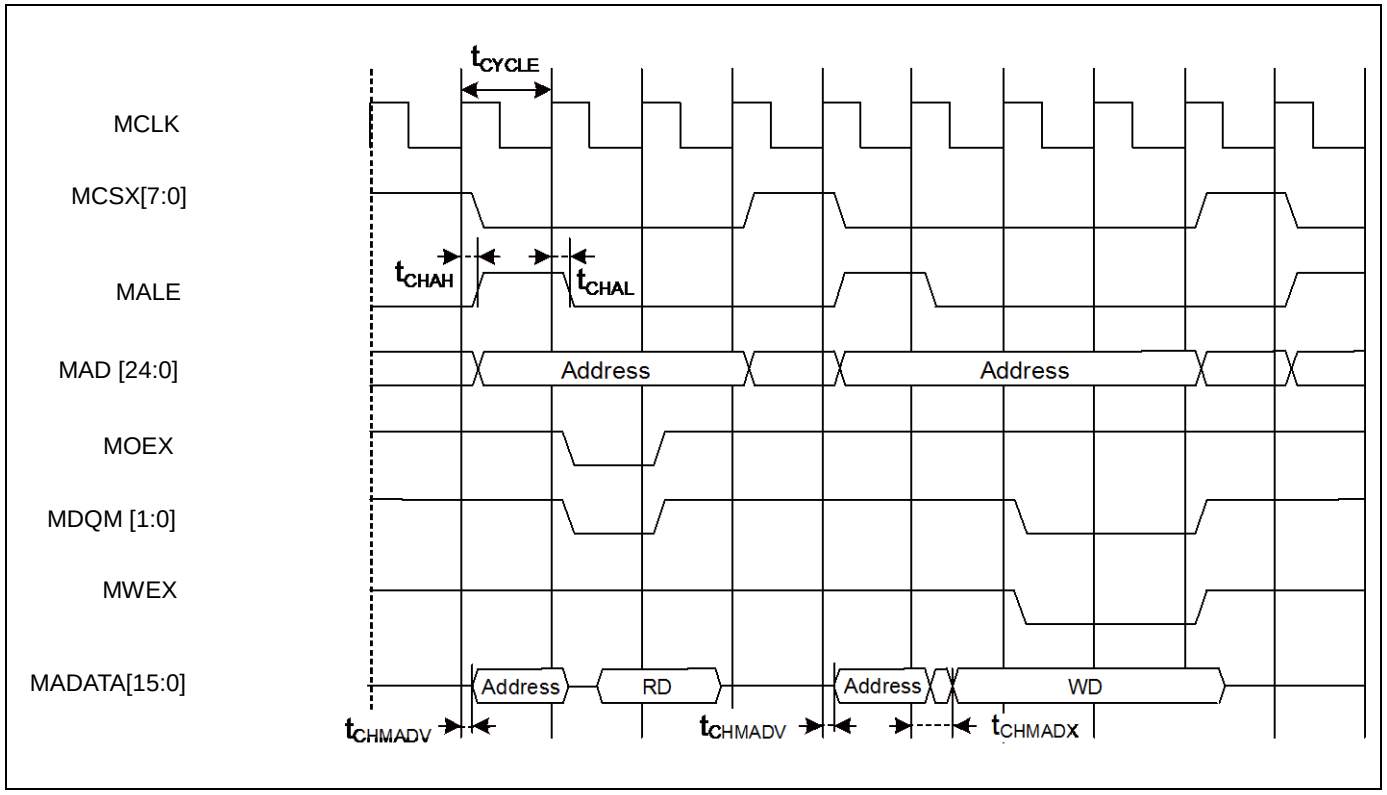


■Multiplexed Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	Vcc ≥ 4.5 V	1	9	ns	
			Vcc < 4.5 V		12	ns	
	t_{CHAH}		Vcc ≥ 4.5 V	1	9	ns	
			Vcc < 4.5 V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	1	t_{OD}	ns	
			Vcc < 4.5 V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		Vcc ≥ 4.5 V	1	t_{OD}	ns	
			Vcc < 4.5 V				

Note: When the external load capacitance = 30 pF.



12.4.13 I^2C Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	8 MHz ≤ t_{CYCP} ≤ 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz < t_{CYCP} ≤ 60 MHz	3 t_{CYCP}*4	-	3 t_{CYCP}*4	-	ns	*5
		60 MHz < t_{CYCP} ≤ 72 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	*5

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

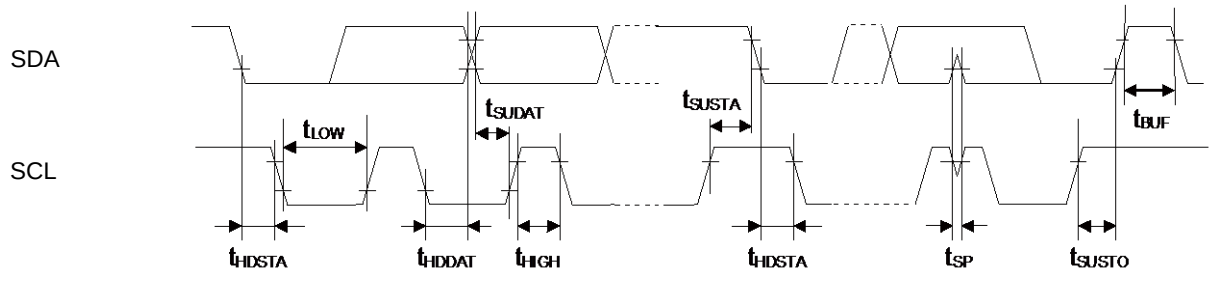
*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

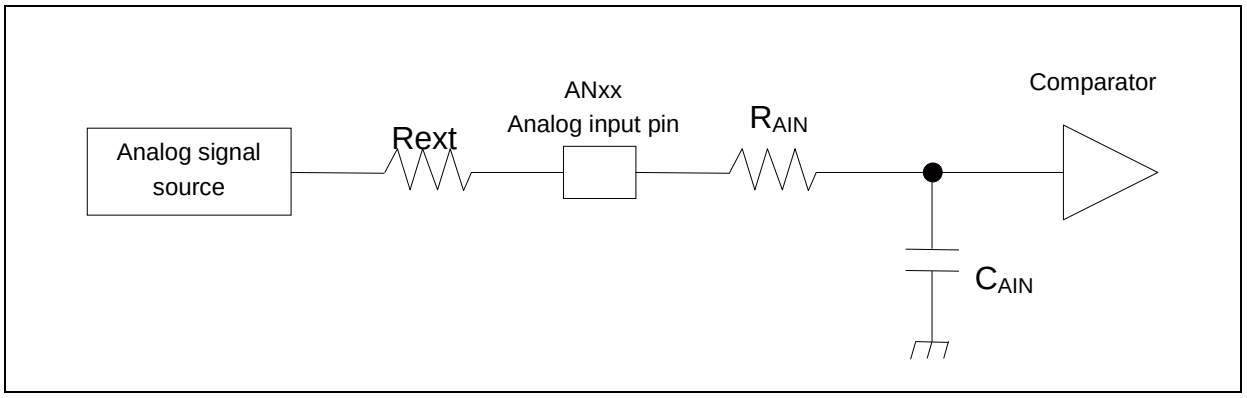
*4: t_{CYCP} is the APB bus clock cycle time.

About the APB bus number which I^2C is connected to, see "■Block Diagram" in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.

*5: The number of steps of the noise filter can be changed with register settings.
Change the number of the noise filter steps according to APB2 bus clock frequency.





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

R_{AIN}: input resistance of A/D = 2 kΩ at $4.5 \leq AV_{CC} \leq 5.5$

input resistance of A/D = 3.8 kΩ at $2.7 \leq AV_{CC} < 4.5$

C_{AIN} input capacity of A/D = 12.9 pF at $2.7 \leq AV_{CC} \leq 5.5$

Rext: Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc Compare time

Tcck Compare clock cycle

12.8 Return Time from Low-Power Consumption Mode

12.8.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

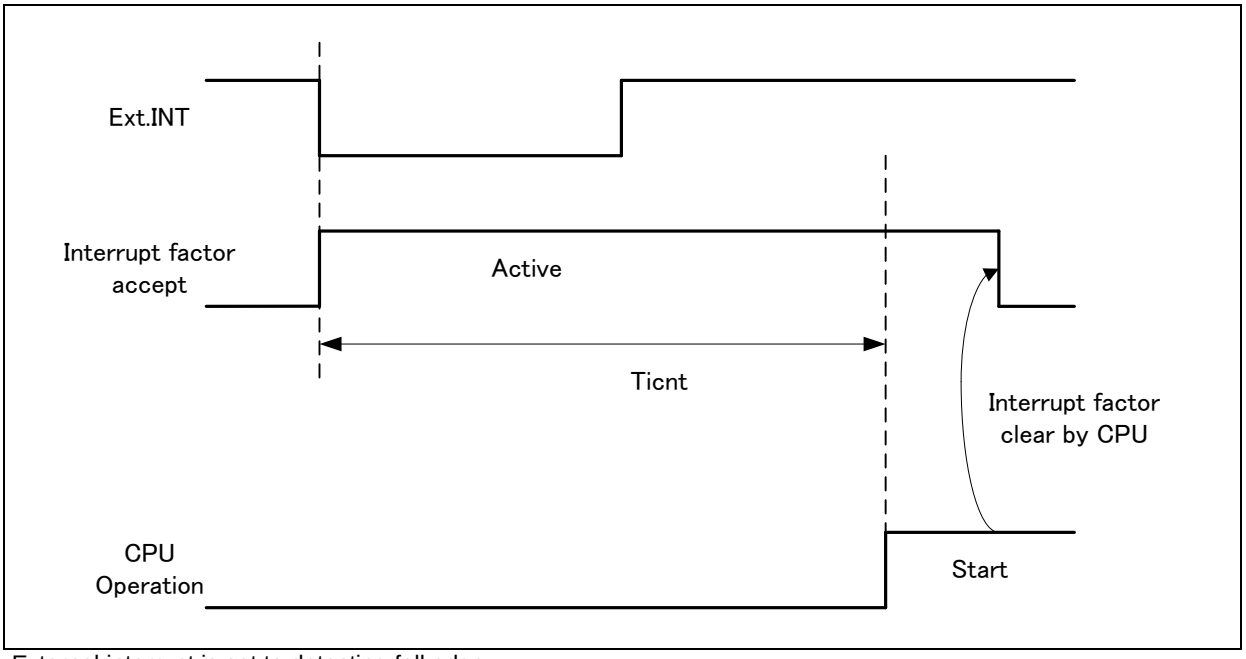
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		40	80	µs	
Low-speed CR TIMER mode		453	737	µs	
Sub TIMER mode		453	737	µs	
STOP mode		453	737	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

15. Major Changes

Spansion Publication Number: MB9B410T-DS706-00018

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
-	-	Preliminary → Data Sheet
2	■ FEATURES • Multi-function Serial Interface (Max 8channels)	Revised the following description. "4 channels with 16-byte FIFO" →"4 channels with 16steps×9-bit FIFO"
6	■ PRODUCT LINEUP Multi-function Serial Interface (UART/CSIO/LIN/I^2C)	Added the following description. "ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO"
8 to 10	■ PIN ASSIGNMENT	Added the description of "Note".
53	■ I/O CIRCUIT TYPE	Added the following description to "Type H". I_{OH} = -20.5mA, I_{OL} = 18.5mA
60 to 62	■ HANDLING DEVICES	• Revised the description of "•Power supply pins". • Revised the description of "•C pin". • Added the description of "•Base Timer".
63	■ BLOCK DIAGRAM	Corrected the figure. • TIOA: input → input/output • TIOB: output → input
74	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	• Corrected the value of "Analog reference voltage (AVRH)". Min: AV_{SS} → 2.7V • Added the "Smoothing capacitor (C_S)". • Added the footnote.
76	3. DC Characteristics (1) Current Rating	• Revised the value of "TBD". • Revised the unit. • Deleted "and estimated values."
79	4. AC Characteristics (1) Main Clock Input Characteristics	• Revised the value of Input frequency (F_{CH}) at "Vcc ≥ 4.5V". Max: 50 → 48 • Added "Internal operating clock frequency (F_{CM}): Master clock".
81	(4-1) Operating Conditions of Main PLL (In the case of using main clock for input of PLL)	Added "Main PLL clock frequency (F_{CLKPLL})".
	(4-2) Operating Conditions of Main PLL (In the case of using built-in high-speed CR clock for the input clock of the main PLL)	

Page	Section	Change Results
85 to 87	■Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
94 to 101	■Electrical Characteristics 4. AC Characteristics (9) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
108	■Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AVcc < 4.5 V · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
113 to 116	■Electrical Characteristics 8. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
117	■Ordering Information	Change to full part number

NOTE: Please see "Document History" about later revised information.

Document History

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Document Number: 002-04689

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TOYO	02/10/2015	Migrated to Cypress and assigned document number 002-4689. No change to document contents or format.
*A	5142656	TOYO	03/10/2016	Updated to Cypress template