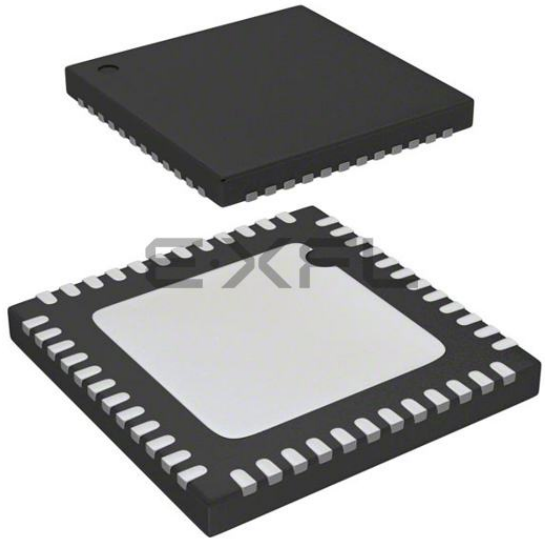

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151ccu6tr

2 Description

The ultra-low-power STM32L151xC and STM32L152xC devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 256 Kbytes and RAM up to 32 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xC and STM32L152xC devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xC and STM32L152xC devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, three USARTs and an USB. The STM32L151xC and STM32L152xC devices offer up to 23 capacitive sensing channels to simply add a touch sensing functionality to any application.

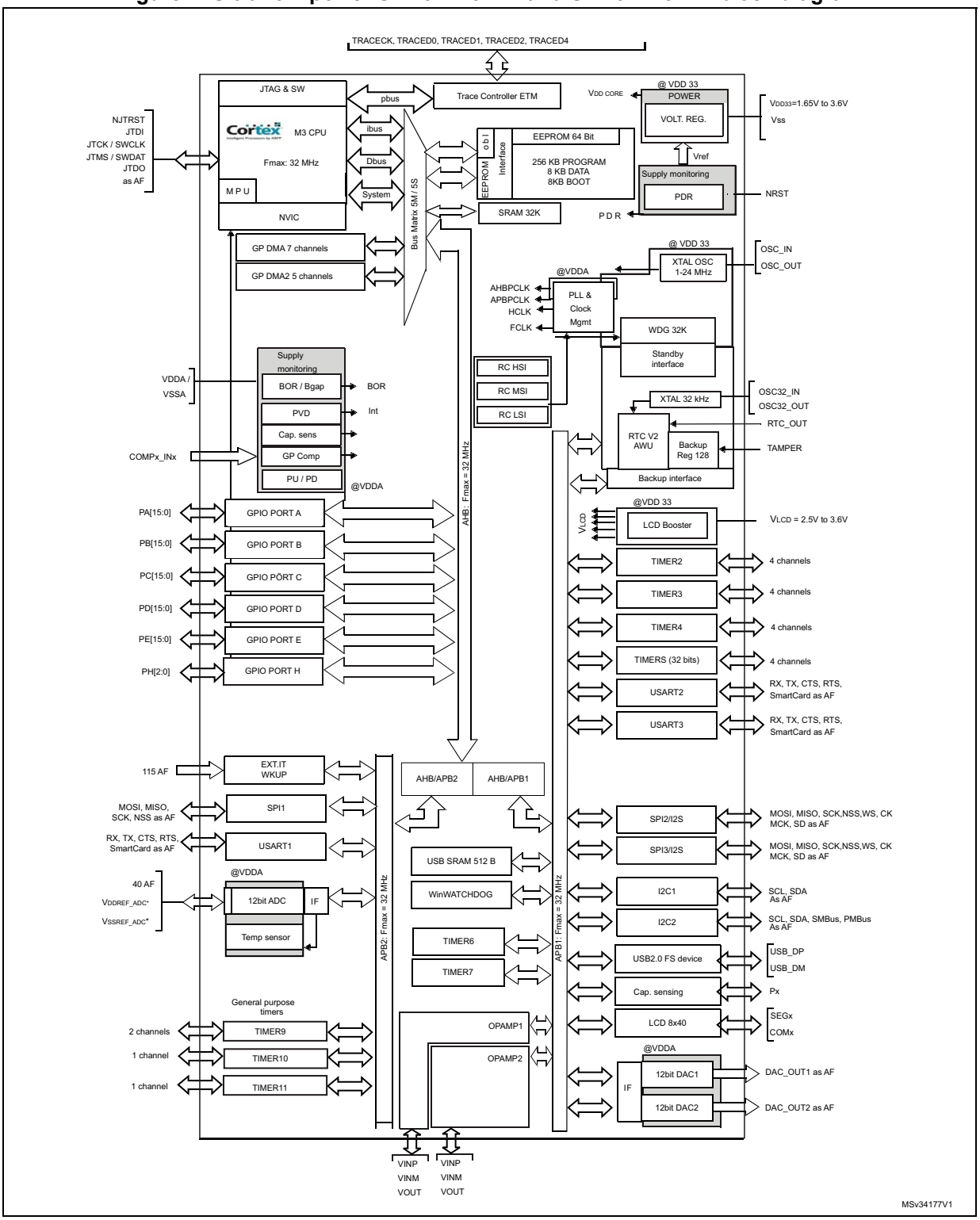
They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xC devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xC and STM32L152xC devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.

3 Functional overview

Figure 1. Ultra-low-power STM32L151xC and STM32L152xC block diagram



- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

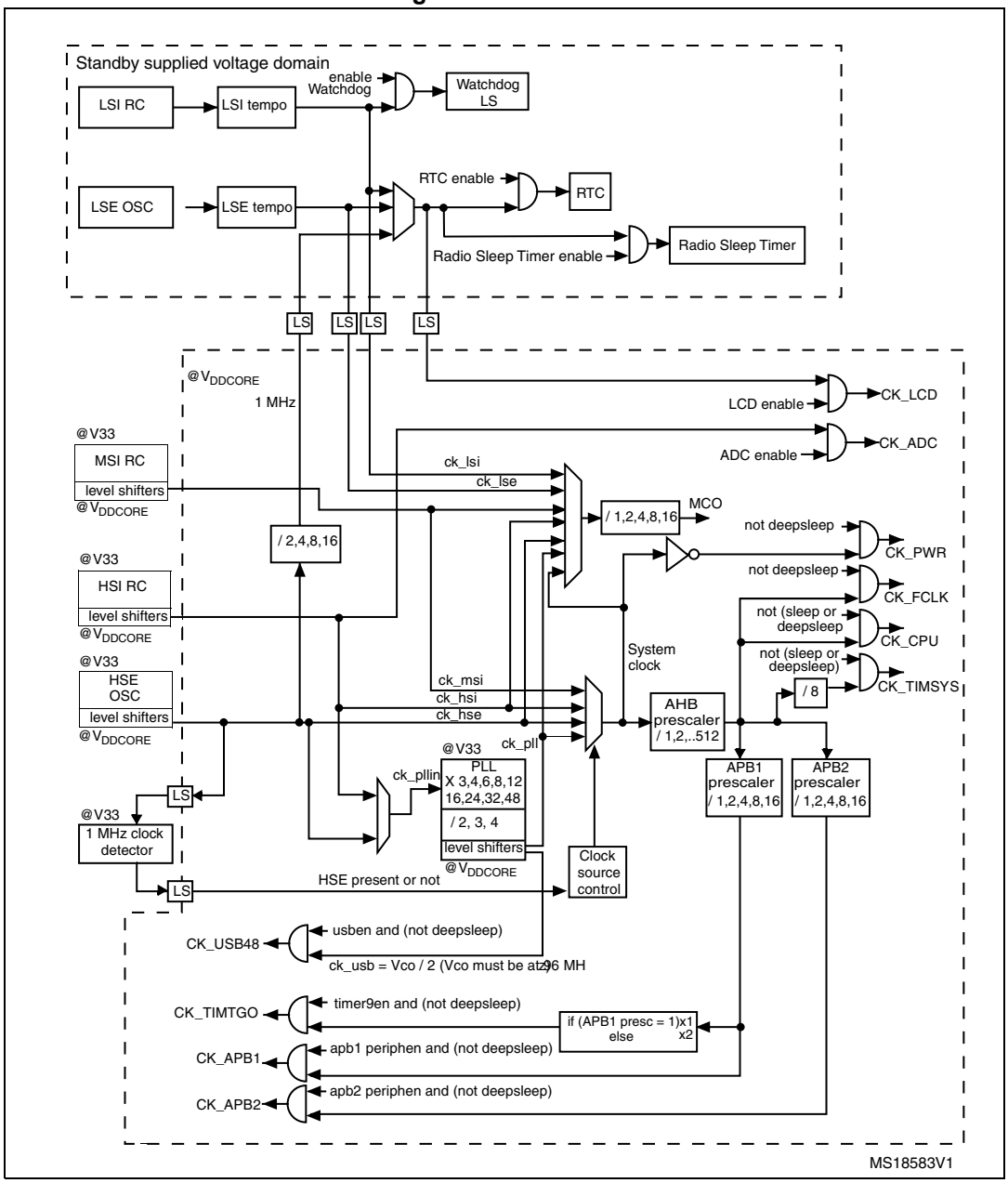
  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Figure 2. Clock tree



3.19 Development support

3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

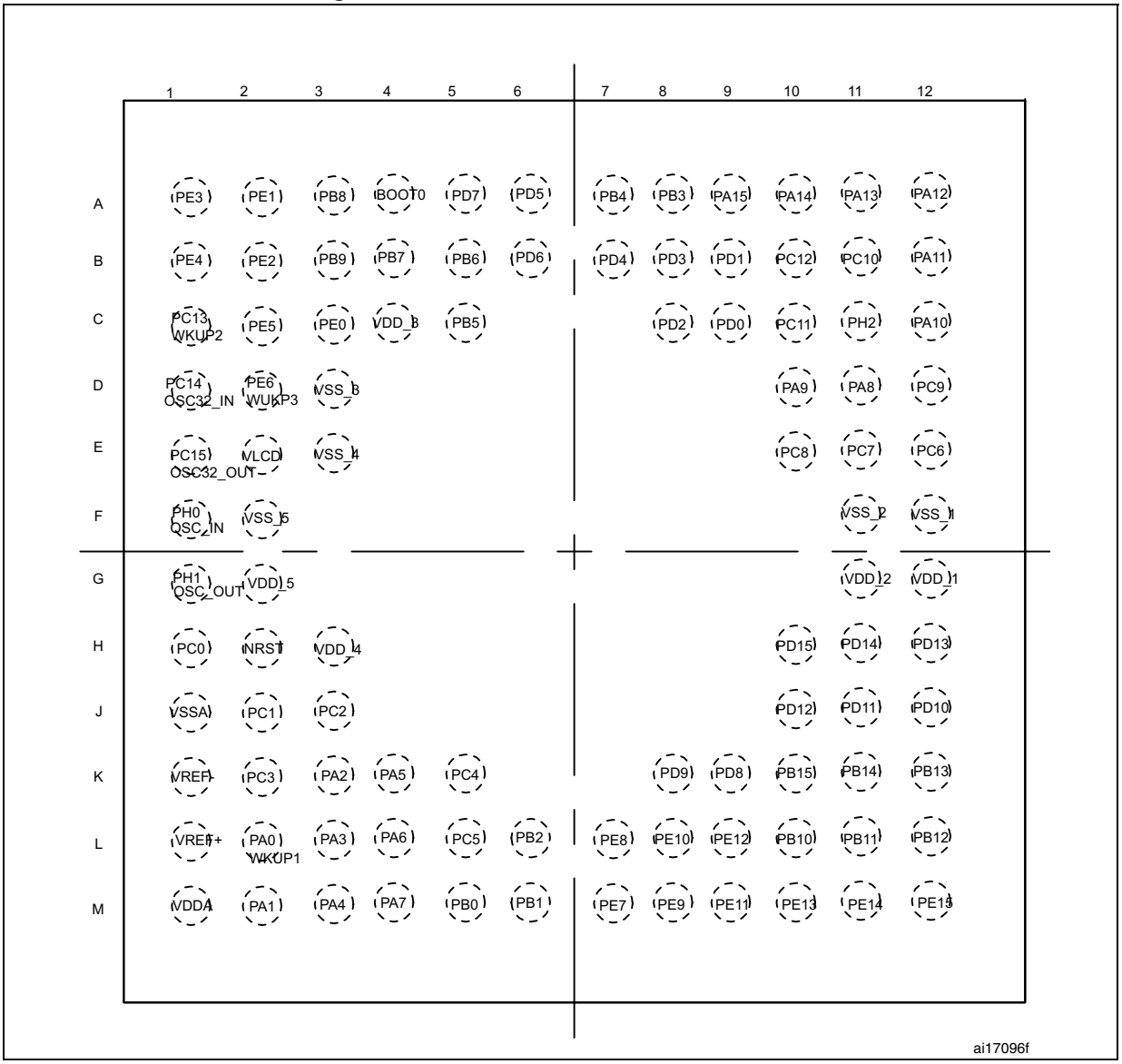
The JTAG port can be permanently disabled with a JTAG fuse.

3.19.2 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151xC and STM32L152xC device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pin descriptions

Figure 3. STM32L15xVC UFBGA100 ballout



1. This figure shows the package top view.

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type[1]	I / O Structure	Main function[2] (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
E11	64	38	E1	-	PC7	I/O	FT	PC7	TIM3_CH2/I2S3_MCK/ LCD_SEG25	-
E10	65	39	D1	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
D12	66	40	E2	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
D11	67	41	E3	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
D10	68	42	C1	30	PA9	I/O	FT	PA9	USART1_TX/ LCD_COM1	-
C12	69	43	D2	31	PA10	I/O	FT	PA10	USART1_RX/ LCD_COM2	-
B12	70	44	B1	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM
A12	71	45	D3	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
A11	72	46	C2	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
C11	73	-	-	-	PH2	I/O	FT	PH2	-	-
F11	74	47	A1	35	V_{SS_2}	S	-	V_{SS_2}	-	-
G11	75	48	B2	36	V_{DD_2}	S	-	V_{DD_2}	-	-
A10	76	49	C3	37	PA14	I/O	FT	JTCK-SWCLK	JTCK-SWCLK	-
A9	77	50	A2	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/ SPI1_NSS/ SPI3_NSS/I2S3_WS/ LCD_SEG17/JTDI	-
B11	78	51	B3	-	PC10	I/O	FT	PC10	SPI3_SCK/I2S3_CK/ USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4	-

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
C10	79	52	A3	-	PC11	I/O	FT	PC11	SPI3_MISO/ USART3_RX/ LCD_SEG29/ LCD_SEG41/ LCD_COM5	-
B10	80	53	B4	-	PC12	I/O	FT	PC12	SPI3_MOSI/I2S3_SD/ USART3_CK/ LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
C9	81	-	-	-	PD0	I/O	FT	PD0	TIM9_CH1/SPI2_NSS/ I2S2_WS	-
B9	82	-	-	-	PD1	I/O	FT	PD1	SPI2_SCK/I2S2_CK	-
C8	83	54	A4	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31 /LCD_SEG43/ LCD_COM7	-
B8	84	-	-	-	PD3	I/O	FT	PD3	SPI2_MISO/ USART2_CTS	-
B7	85	-	-	-	PD4	I/O	FT	PD4	SPI2_MOSI/I2S2_SD/ USART2_RTS	-
A6	86	-		-	PD5	I/O	FT	PD5	USART2_TX	-
B6	87	-	-	-	PD6	I/O	FT	PD6	USART2_RX	-
A5	88	-	-	-	PD7	I/O	FT	PD7	TIM9_CH2/USART2_CK	-
A8	89	55	C4	39	PB3	I/O	FT	JTDO	TIM2_CH2/SPI1_SCK/ SPI3_SCK/I2S3_CK/ LCD_SEG7/JTDO	COMP2_INM
A7	90	56	D4	40	PB4	I/O	FT	NJTRST	TIM3_CH1/SPI1_MISO/ SPI3_MISO/LCD_SEG8 /NJTRST	COMP2_INP
C5	91	57	A5	41	PB5	I/O	FT	PB5	TIM3_CH2/I2C1_SMBA/ SPI1_MOSI/SPI3_MOSI /I2S3_SD/LCD_SEG9	COMP2_INP

Alternate functions

Table 10. Alternate function input/output

Port name	Digital alternate function number												
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-		-		-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-		-		-	-
PA0-WKUP1	-	TIM2_CH1_ ETR	TIM5_CH1	-	-	-	-	USART2_CTS		-		TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS		SEG0		TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX		SEG1		TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX		SEG2		TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK		-		TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-		-		TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_ CH1	-	SPI1_MISO	-	-		SEG3		TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_ CH1	-	SPI1_MOSI	-	-		SEG4		TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK		COM0		TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX		COM1		TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX		COM2		TIMx_IC3	EVENT OUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS		-		TIMx_IC4	EVENT OUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS		-		TIMx_IC1	EVENT OUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-		-		TIMx_IC2	EVENT OUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-		-		TIMx_IC3	EVEN TOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-		SEG17		TIMx_IC4	EVEN TOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

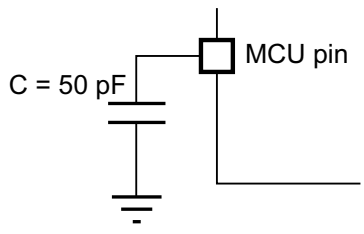
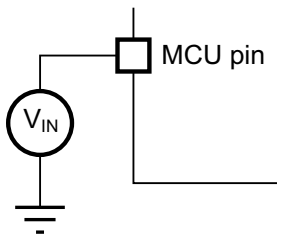


Figure 11. Pin input voltage



5. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to the Dhrystone 2.1 code, unless otherwise specified. The current consumption values are derived from tests performed under ambient temperature T_A = 25 °C and V_{DD} supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 27: High-speed external user clock characteristics*.
- For maximum current consumption $V_{DD} = V_{DDA}$ = 3.6 V is applied to all supply pins.
- For typical current consumption $V_{DD} = V_{DDA}$ = 3.0 V is applied to all supply pins if not specified otherwise.

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.8	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.435	1	
			T_A = 55°C	0.99	3	
			T_A= 85°C	2.4	9	
			T_A = 105°C	5.5	22(5)	
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	MSI = 4.2 MHz	T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(6)		1.45	-	

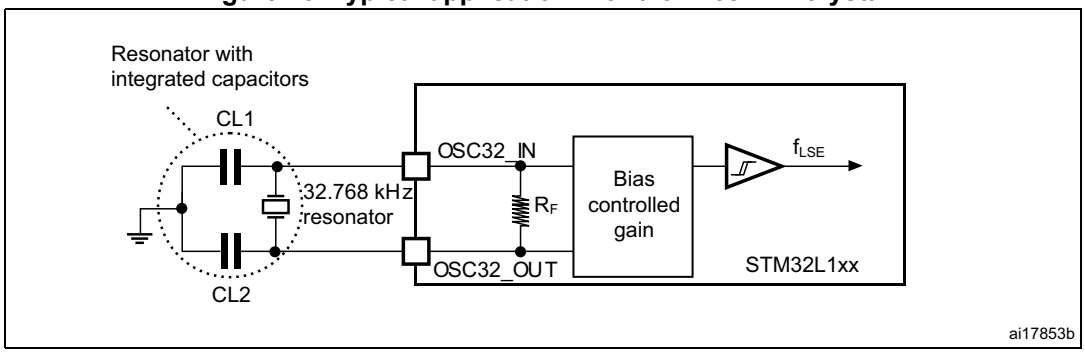
1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
3. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Guaranteed by test in production.
6. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining part of the wakeup period, the current corresponds the Run mode current.

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 18). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if the user chooses a resonator with a load capacitance of C_L = 6 pF and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 18. Typical application with a 32.768 kHz crystal



6.3.7 Internal clock source characteristics

The parameters given in *Table 31* are derived from tests performed under the conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 31. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 32. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift 0°C ≤T_A ≤105°C	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation, LCD levels).

The test results are given in the *Table 42*.

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all 5 V tolerant (FT) pins	-5 (1)	NA	mA
	Injected current on BOOT0	-0	NA	
	Injected current on any other pin	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 45*, respectively.

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 14*.

Table 45. I/O AC characteristics(1)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	400	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	625	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	625	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	1	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	250	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	25	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	125	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	8	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	30	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151xx, STM32L152xx and STM32L162xx reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

Figure 30. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

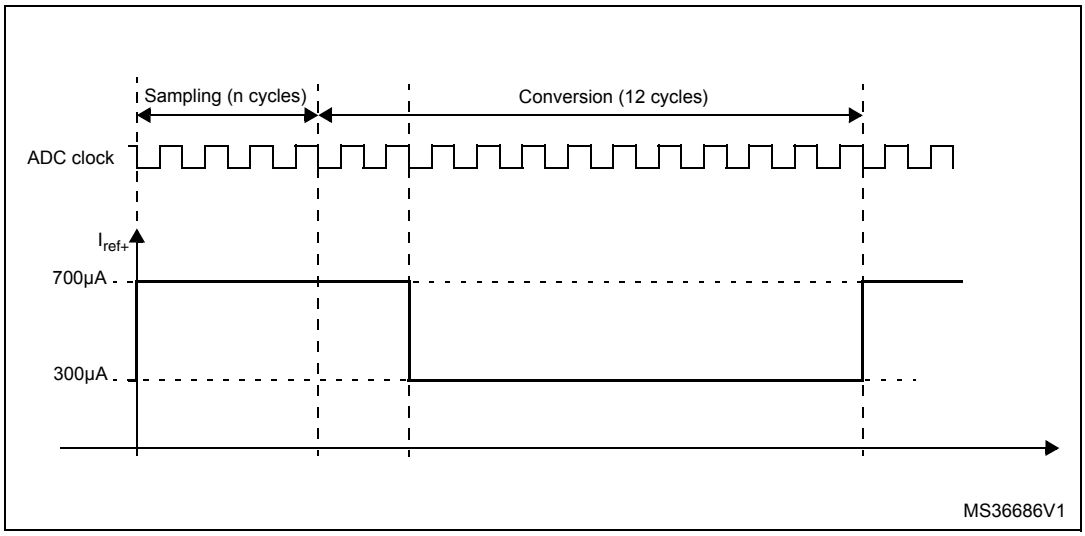


Table 58. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kΩ)				Ts (cycles) f_{ADC}=16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for f_{ADC} = 16 MHz. For f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (µs),

General PCB design guidelines

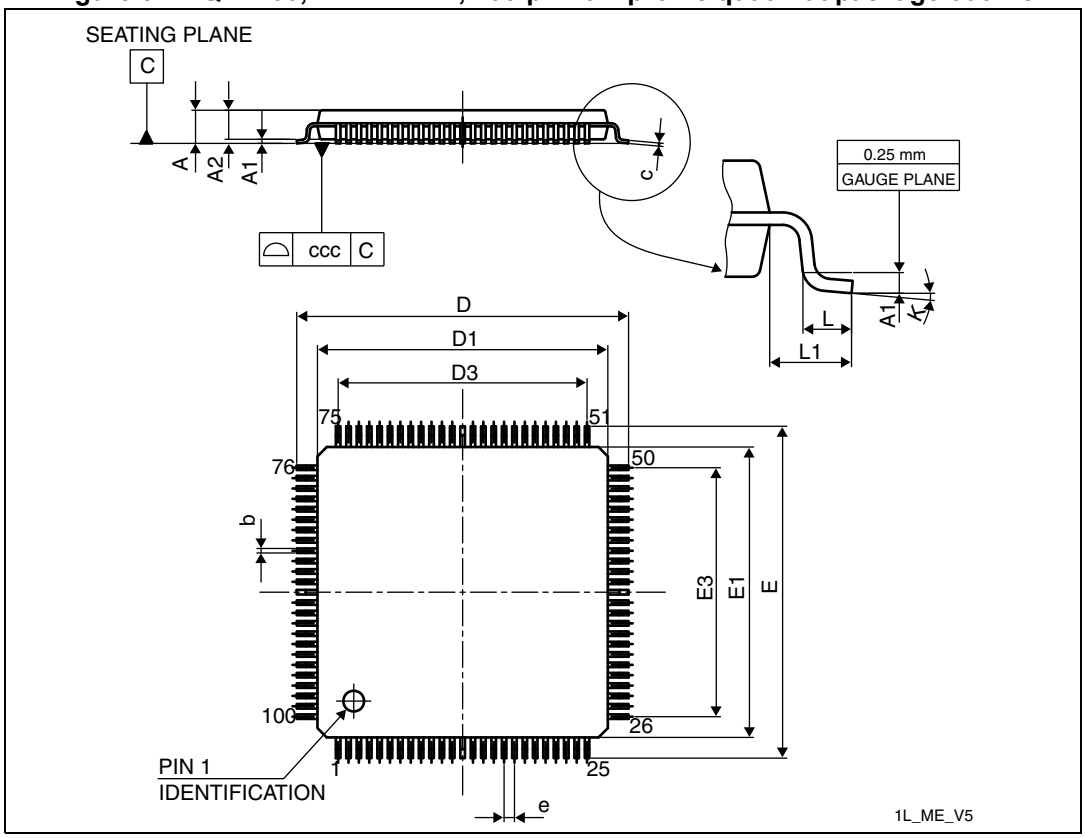
Power supply decoupling should be performed as shown in *Figure 12*. The applicable procedure depends on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 32. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

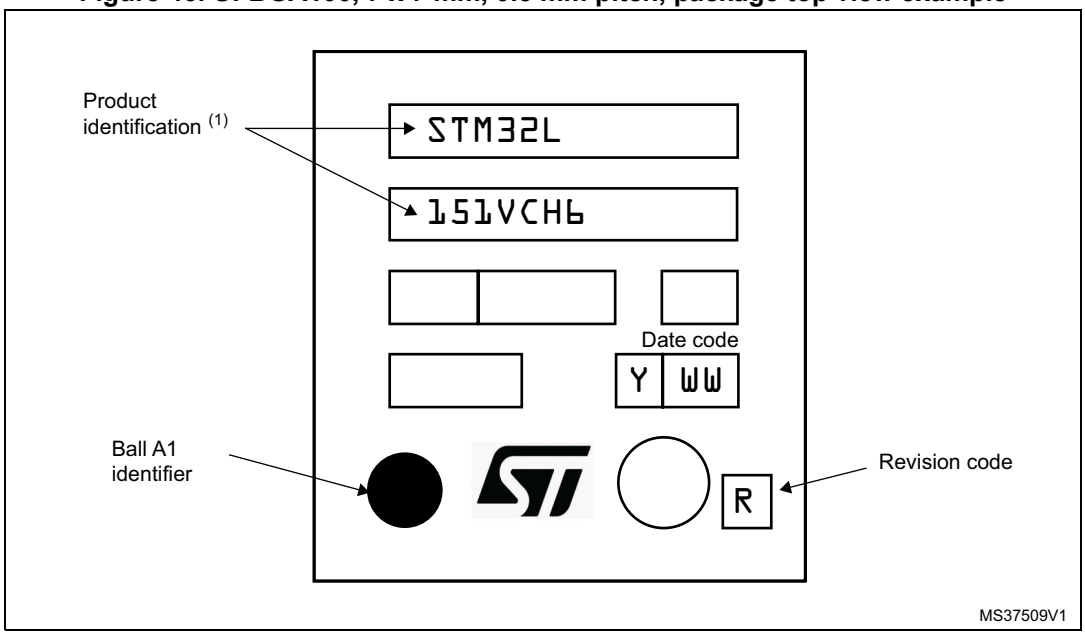
Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 46. UFBGA100, 7 x 7 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity