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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rct6

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3.1 Low-power modes

The ultra-low-power STM32L151xC and STM32L152xC devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V - 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep** mode

  This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.
- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.

introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.16 Timers and watchdogs

The ultra-low-power STM32L151xC and STM32L152xC devices include seven general-purpose timers, two basic timers, and two watchdog timers.

Table 7 compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xC and STM32L152xC devices (see *Table 7* for differences).

TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
C1	7	2	D5	2	PC13-WKUP2	I/O	FT	PC13	-	WKUP2/ RTC_TAMP1/ RTC_TS/RTC_OUT
D1	8	3	D7	3	PC14-OSC32_IN(4)	I/O	TC	PC14	-	OSC32_IN
E1	9	4	D6	4	PC15-OSC32_OUT	I/O	TC	PC15	-	OSC32_OUT
F2	10	-	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
G2	11	-	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
F1	12	5	F6	5	PH0-OSC_IN(5)	I/O	TC	PH0	-	OSC_IN
G1	13	6	F7	6	PH1-OSC_OUT(5)	I/O	TC	PH1	-	OSC_OUT
H2	14	7	E7	7	NRST	I/O	RST	NRST	-	-
H1	15	8	E6	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
J2	16	9	E5	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
J3	17	10	G7	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
K2	18	11	G6	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP
J1	19	12	F5	8	V_{SSA}	S	-	V_{SSA}	-	-
K1	20	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
L1	21	-	-	-	V_{REF+}	S	-	V_{REF+}	-	-
M1	22	13	H7	9	V_{DDA}	S	-	V_{DDA}	-	-
L2	23	14	E4	10	PA0-WKUP1	I/O	FT	PA0	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/ RTC_TAMP2/ ADC_IN0/ COMP1_INP

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
M2	24	15	G5	11	PA1	I/O	FT	PA1	TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0	ADC_IN1/ COMP1_INP/ OPAMP1_VINP
K3	25	16	H6	12	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/USART2_TX /LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
L3	26	17	J7	13	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/USART2_RX /LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
E3	27	18	-	-	V_{SS_4}	S	-	V_{SS_4}	-	-
H3	28	19	-	-	V_{DD_4}	S	-	V_{DD_4}	-	-
M3	29	20	J6	14	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
K4	30	21	H4	15	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
L4	31	22	G4	16	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/ SPI1_MISO/LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
M4	32	23	J5	17	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM
K5	33	24	F4	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
L5	34	25	J4	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
M5	35	26	J3	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VLCDRAIL3/ VREF_OUT

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
E11	64	38	E1	-	PC7	I/O	FT	PC7	TIM3_CH2/I2S3_MCK/ LCD_SEG25	-
E10	65	39	D1	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
D12	66	40	E2	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
D11	67	41	E3	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
D10	68	42	C1	30	PA9	I/O	FT	PA9	USART1_TX/ LCD_COM1	-
C12	69	43	D2	31	PA10	I/O	FT	PA10	USART1_RX/ LCD_COM2	-
B12	70	44	B1	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM
A12	71	45	D3	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
A11	72	46	C2	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
C11	73	-	-	-	PH2	I/O	FT	PH2	-	-
F11	74	47	A1	35	V_{SS_2}	S	-	V_{SS_2}	-	-
G11	75	48	B2	36	V_{DD_2}	S	-	V_{DD_2}	-	-
A10	76	49	C3	37	PA14	I/O	FT	JTCK-SWCLK	JTCK-SWCLK	-
A9	77	50	A2	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/ SPI1_NSS/ SPI3_NSS/I2S3_WS/ LCD_SEG17/JTDI	-
B11	78	51	B3	-	PC10	I/O	FT	PC10	SPI3_SCK/I2S3_CK/ USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4	-

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
C10	79	52	A3	-	PC11	I/O	FT	PC11	SPI3_MISO/ USART3_RX/ LCD_SEG29/ LCD_SEG41/ LCD_COM5	-
B10	80	53	B4	-	PC12	I/O	FT	PC12	SPI3_MOSI/I2S3_SD/ USART3_CK/ LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
C9	81	-	-	-	PD0	I/O	FT	PD0	TIM9_CH1/SPI2_NSS/ I2S2_WS	-
B9	82	-	-	-	PD1	I/O	FT	PD1	SPI2_SCK/I2S2_CK	-
C8	83	54	A4	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31 /LCD_SEG43/ LCD_COM7	-
B8	84	-	-	-	PD3	I/O	FT	PD3	SPI2_MISO/ USART2_CTS	-
B7	85	-	-	-	PD4	I/O	FT	PD4	SPI2_MOSI/I2S2_SD/ USART2_RTS	-
A6	86	-		-	PD5	I/O	FT	PD5	USART2_TX	-
B6	87	-	-	-	PD6	I/O	FT	PD6	USART2_RX	-
A5	88	-	-	-	PD7	I/O	FT	PD7	TIM9_CH2/USART2_CK	-
A8	89	55	C4	39	PB3	I/O	FT	JTDO	TIM2_CH2/SPI1_SCK/ SPI3_SCK/I2S3_CK/ LCD_SEG7/JTDO	COMP2_INM
A7	90	56	D4	40	PB4	I/O	FT	NJTRST	TIM3_CH1/SPI1_MISO/ SPI3_MISO/LCD_SEG8 /NJTRST	COMP2_INP
C5	91	57	A5	41	PB5	I/O	FT	PB5	TIM3_CH2/I2C1_SMBA/ SPI1_MOSI/SPI3_MOSI /I2S3_SD/LCD_SEG9	COMP2_INP

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number												
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS		-		TIMx_IC4	EVENT OUT
PD4	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	USART2_RTS		-		TIMx_IC1	EVENT OUT
PD5	-	-	-	-	-		-	USART2_TX		-		TIMx_IC2	EVENT OUT
PD6	-	-	-		-	-	-	USART2_RX		-		TIMx_IC3	EVENT OUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK		-		TIMx_IC4	EVENT OUT
PD8	-	-	-	-	-	-	-	USART3_TX		SEG28		TIMx_IC1	EVENT OUT
PD9	-	-	-	-	-	-	-	USART3_RX		SEG29		TIMx_IC2	EVENT OUT
PD10	-	-	-	-	-	-	-	USART3_CK		SEG30		TIMx_IC3	EVENT OUT
PD11	-	-	-	-	-	-	-	USART3_CTS		SEG31		TIMx_IC4	EVENT OUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS		SEG32		TIMx_IC1	EVENT OUT
PD13	-	-	TIM4_CH2	-	-	-	-	-		SEG33		TIMx_IC2	EVENT OUT
PD14	-	-	TIM4_CH3	-	-	-	-	-		SEG34		TIMx_IC3	EVENT OUT
PD15	-	-	TIM4_CH4	-	-	-	-	-		SEG35		TIMx_IC4	EVENT OUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-		SEG36		TIMx_IC1	EVENT OUT
PE1	-	-	-	TIM11_CH1	-	-	-	-		SEG37		TIMx_IC2	EVENT OUT
PE2	TRACECK	-	TIM3_ETR	-				-		SEG 38		TIMx_IC3	EVENT OUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-		SEG 39		TIMx_IC4	EVENT OUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-		-		TIMx_IC1	EVENT OUT
PE5	TRACED2	-	-	TIM9_CH1	-	-	-	-		-		TIMx_IC2	EVENT OUT
PE6-WKUP3	TRACED3	-	-	TIM9_CH2	-	-	-	-		-		TIMx_IC3	EVENT OUT
PE7	-	-	-	-	-	-	-	-		-		TIMx_IC4	EVENT OUT

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} – V_{SS}\|$	Variations between all different ground pins(3)	-	50	
$V_{REF+} – V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 12* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
$I_{VSS(\Sigma)}$(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4), RST and B pins	-5/+0	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation(5)	–40	85	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	110	

1. When the ADC is used, refer to *Table 56: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and up to 140 mV in operation.
3. To sustain a voltage higher than VDD+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 73: Thermal characteristics on page 128*).
5. In low-power dissipation state, T_A can be extended to -40°C to 105°C temperature range as long as T_J does not exceed T_J max (see *Table 73: Thermal characteristics on page 128*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the conditions summarized in *Table 14*.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

Flash memory and data EEPROM

Table 36. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming/ erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	600	900	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 37. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

6.3.16 Communications interfaces

I²C interface characteristics

The device I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 48*. Refer also to *Section 6.3.13: I/O port characteristics* for more details on the input/output ction characteristics (SDA and SCL).

Table 48. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	µs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	µs
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns

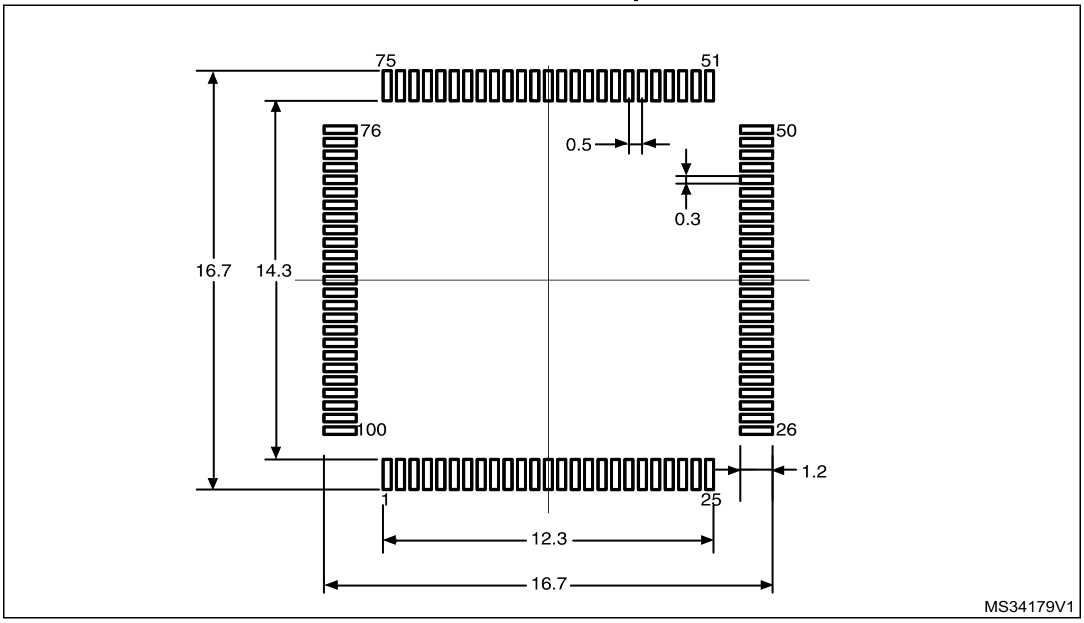
1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$.

Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

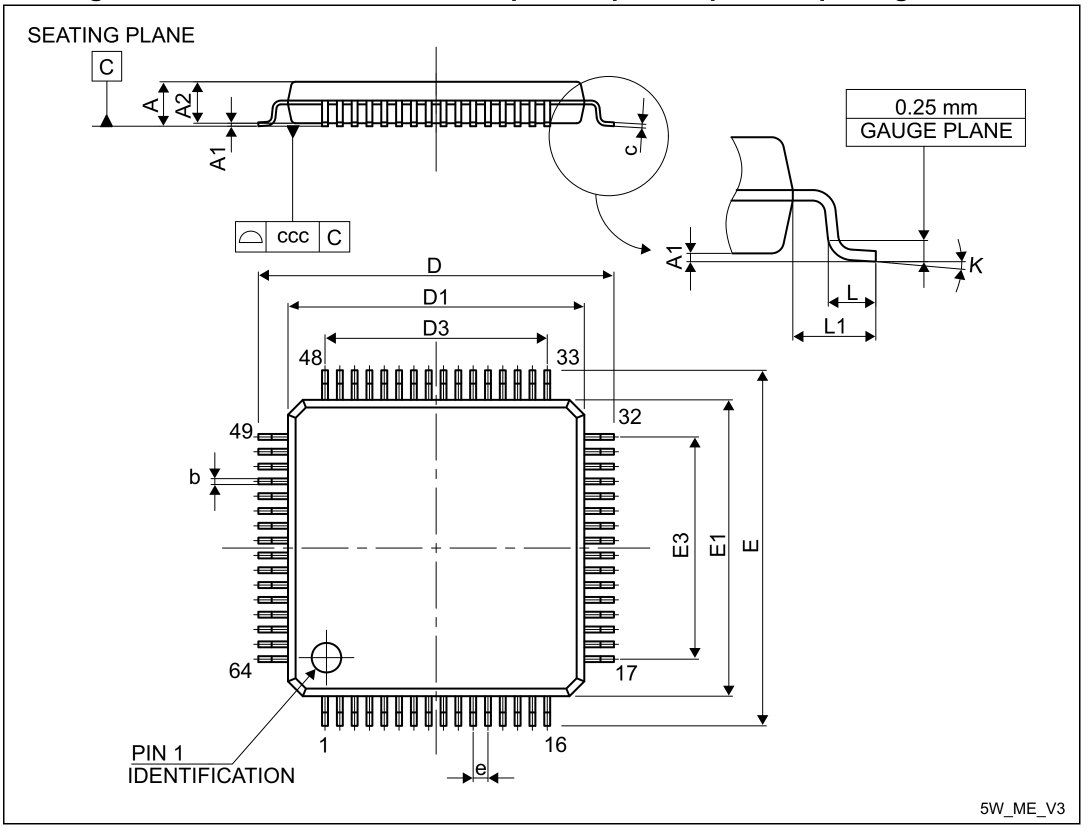
Figure 33. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.2 LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 35. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline



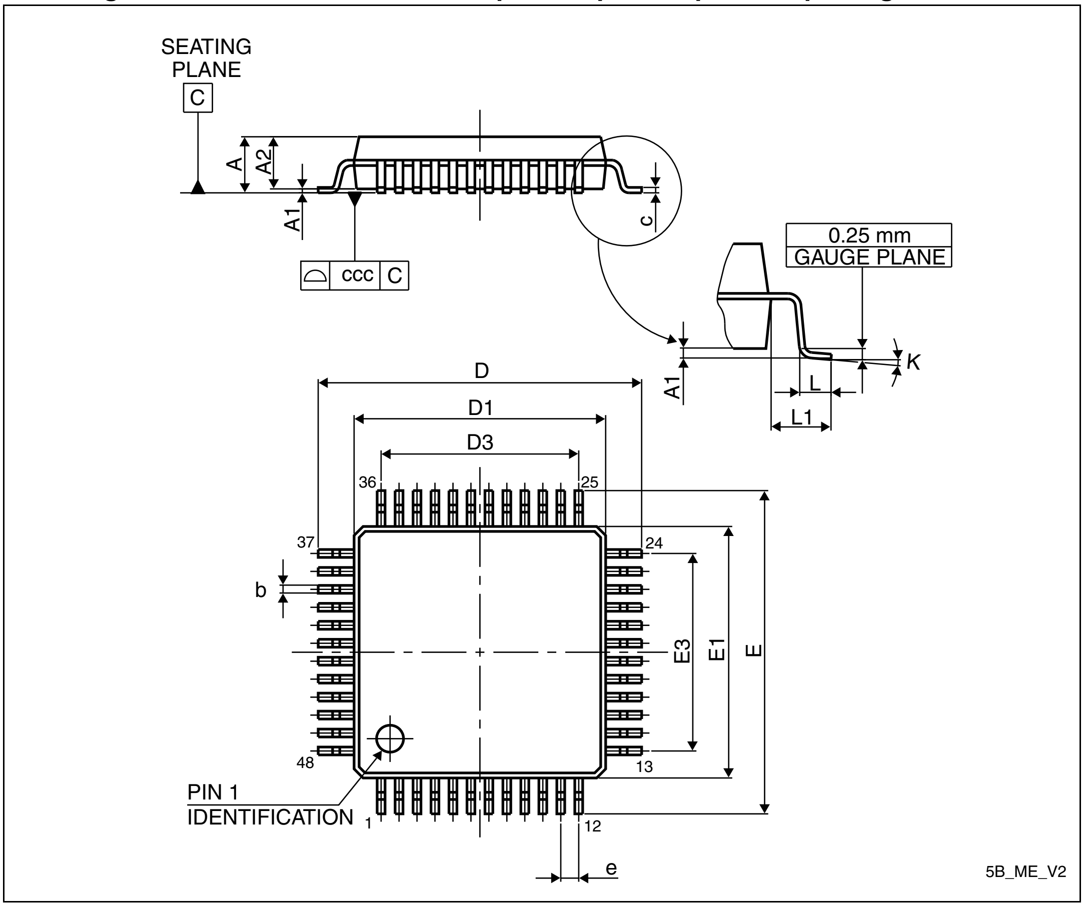
1. Drawing is not to scale.

Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

7.3 LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 38. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 73. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm	59	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP63 - 0.400 mm pitch	49	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	