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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rct6tr

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3.1 Low-power modes

The ultra-low-power STM32L151xC and STM32L152xC devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V - 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep** mode

  This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xC and STM32L152xC devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xC and STM32L152xC devices embed a nested vectored interrupt controller able to handle up to 53 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rail decoupling capability

Table 6. V_{LCD} rail decoupling

	Bias			Pin	
	1/2	1/3	1/4		
$V_{LCDRAIL1}$	1/2 V_{LCD}	2/3 V_{LCD}	1/2 V_{LCD}	PB2	
$V_{LCDRAIL2}$	N/A	1/3 V_{LCD}	1/4 V_{LCD}	PB12	PE11
$V_{LCDRAIL3}$	N/A	N/A	3/4 V_{LCD}	PB0	PE12

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xC and STM32L152xC devices with up to 25 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 24 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 61: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 16: Embedded internal reference voltage calibration values*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151xC and STM32L152xC devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Operational amplifier

The STM32L151xC and STM32L152xC devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.13 Ultra-low-power comparators and reference voltage

The STM32L151xC and STM32L152xC devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.15 Touch sensing

The STM32L151xC and STM32L152xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation

3.19 Development support

3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

3.19.2 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151xC and STM32L152xC device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 8. Legend/abbreviations used in the pinout table

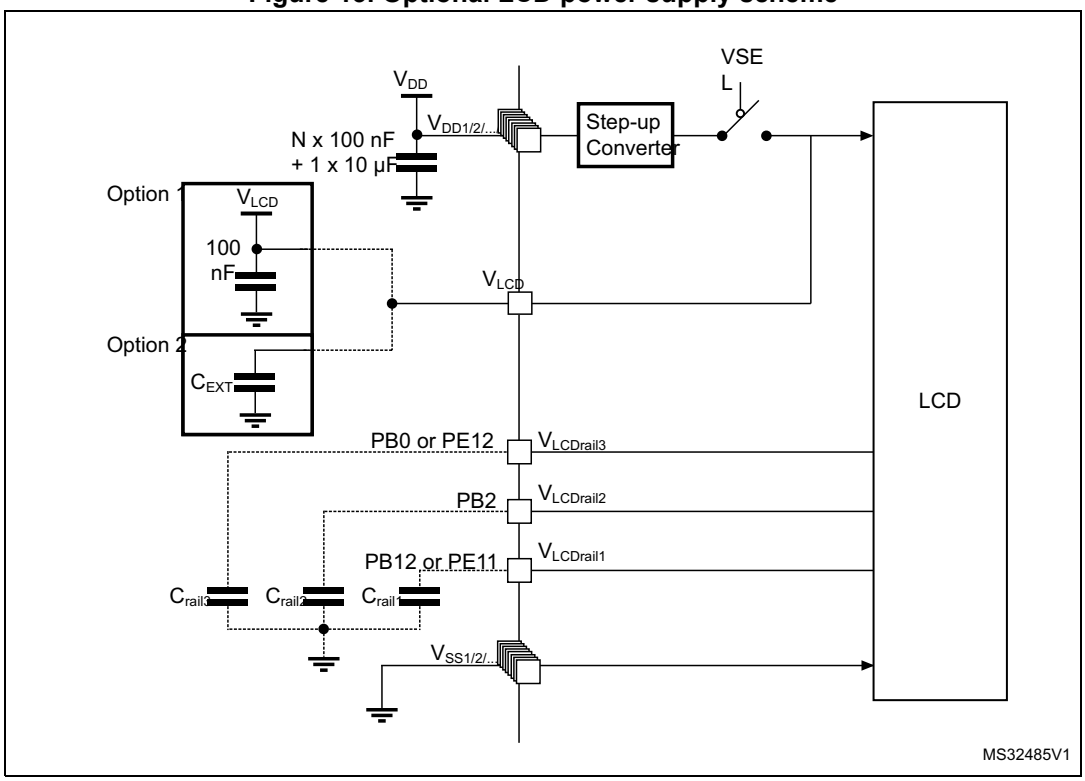
Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151xC and STM32L152xC pin definitions

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT	PE2	TIM3_ETR/LCD_SEG38 /TRACECLK	-
A1	2	-	-	-	PE3	I/O	FT	PE3	TIM3_CH1/LCD_SEG39 /TRACED0	-
B1	3	-	-	-	PE4	I/O	FT	PE4	TIM3_CH2/TRACED1	-
C2	4	-	-	-	PE5	I/O	FT	PE5	TIM9_CH1/TRACED2	-
D2	5	-	-	-	PE6-WKUP3	I/O	FT	PE6	TIM9_CH2/ TRACED3	WKUP3/ RTC_TAMP3
E2	6	1	C7	1	V_{LCD}(3)	S	-	V_{LCD}	-	-

6.1.7 Optional LCD power supply scheme

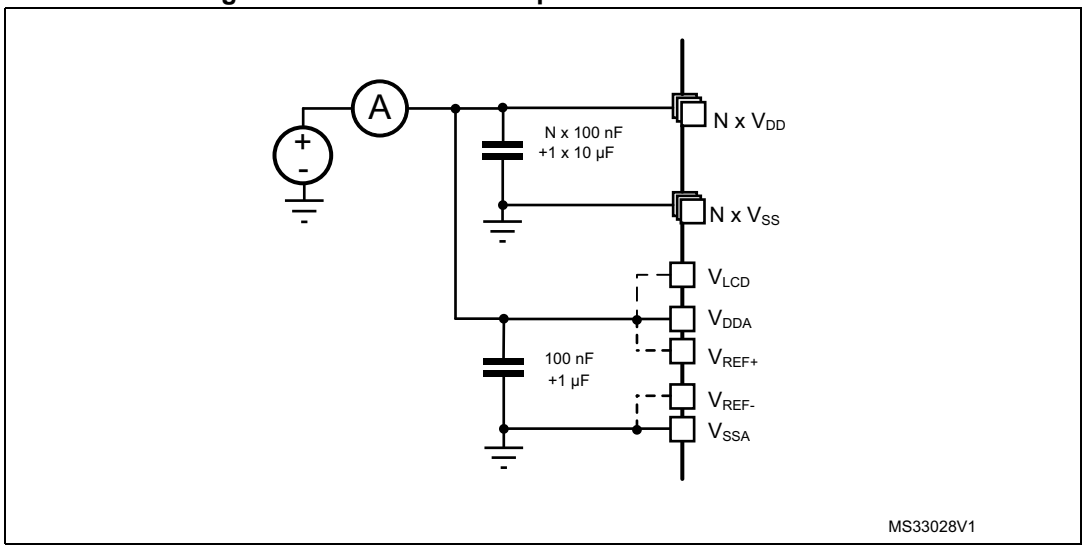
Figure 13. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.3.3 Embedded internal reference voltage

The parameters given in *Table 17* are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

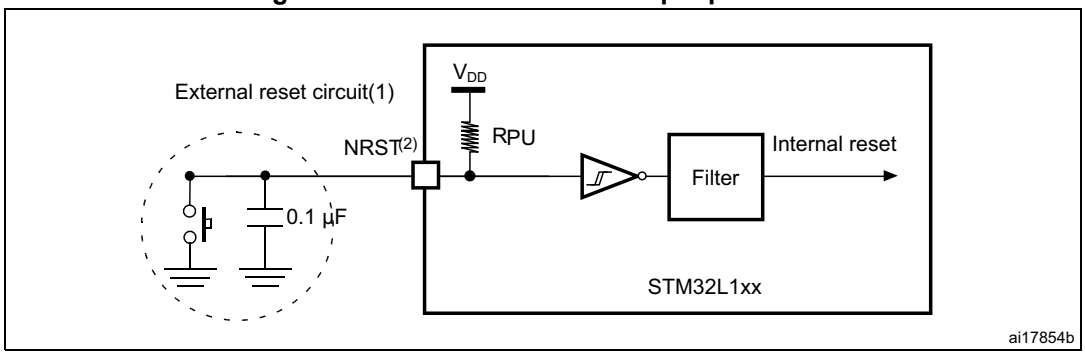
Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$ (1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3) (4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current (5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in the *Table 47* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output ction characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

Table 53. USB: full speed electrical characteristics (continued)

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

I2S characteristics

Table 54. I2S characteristics

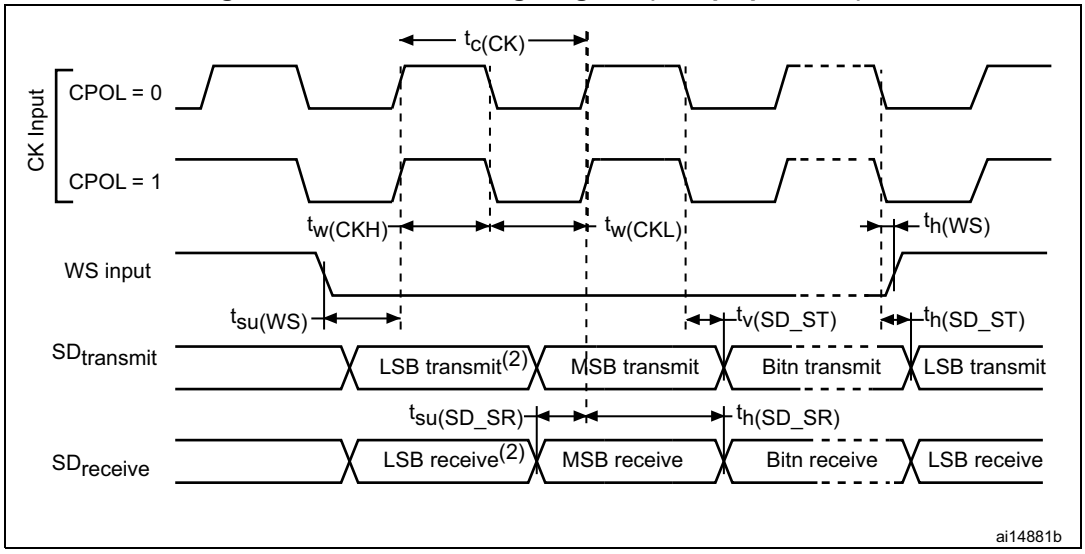
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main Clock Output		256 x 8K	256xFs [1]	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver, 48KHz	30	70	%
$t_{r(CK)}$	I2S clock rise time	Capacitive load CL=30pF	-	8	ns
$t_{f(CK)}$	I2S clock fall time			8	
$t_{v(WS)}$	WS valid time	Master mode	4	24	
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	15	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	8	-	
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	9	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	4	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	64	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	22	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	12	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8	-	

1. The maximum for 256xFs is 8 MHz

Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the

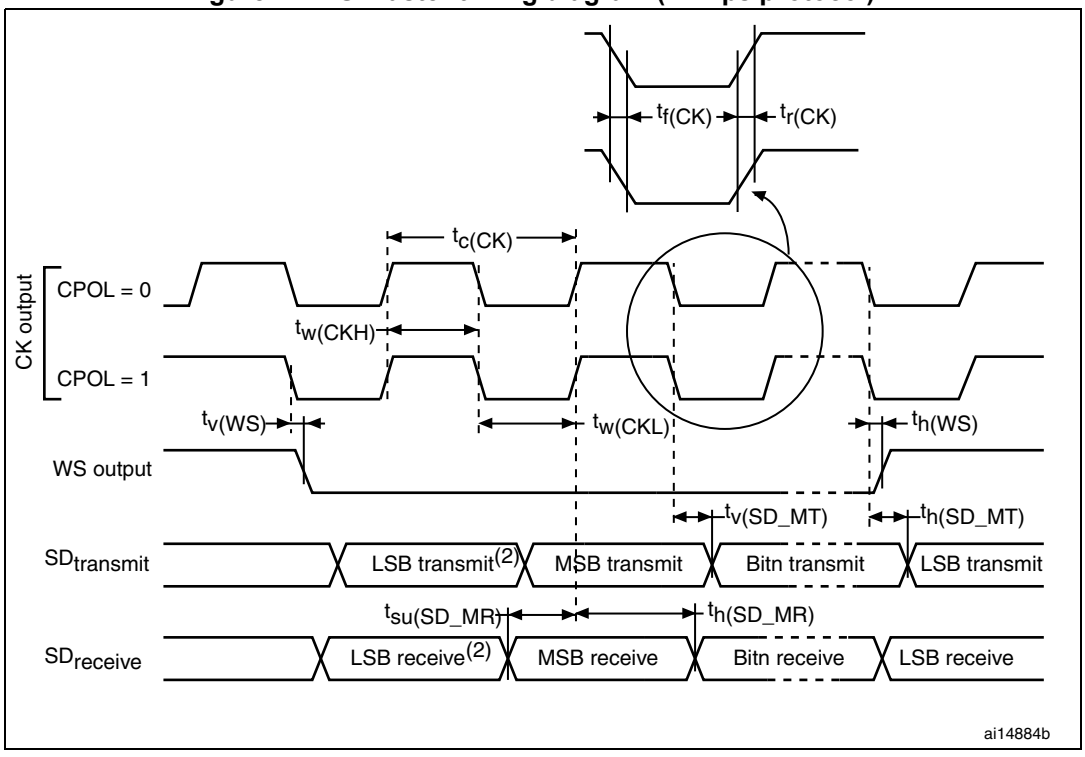
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 26. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 56* are guaranteed by design.

Table 55. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage range 1 & 2	2.4 V ≤V_{DDA} ≤3.6 V	V_{REF+} = V_{DDA}	0.480	16	MHz
				V_{REF+} < V_{DDA} V_{REF+} > 2.4 V		8	
				V_{REF+} < V_{DDA} V_{REF+} ≤2.4 V		4	
			1.8 V ≤V_{DDA} ≤2.4 V	V_{REF+} = V_{DDA}		8	
				V_{REF+} < V_{DDA}		4	
		Voltage range 3				4	

Table 56. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}(2)	Current on the V_{REF} input pin	Peak	-	400	700	
		Average	-		450	
V_{AIN}	Conversion voltage range(3)	-	0(4)	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	-	-	1	Msps
		Multiplexed channels	-	-	0.76	
	10-bit sampling rate	Direct channels	-	-	1.07	Msps
		Multiplexed channels	-	-	0.8	
	8-bit sampling rate	Direct channels	-	-	1.23	Msps
		Multiplexed channels	-	-	0.89	
	6-bit sampling rate	Direct channels	-	-	1.45	Msps
		Multiplexed channels	-	-	1	

Figure 28. ADC accuracy characteristics

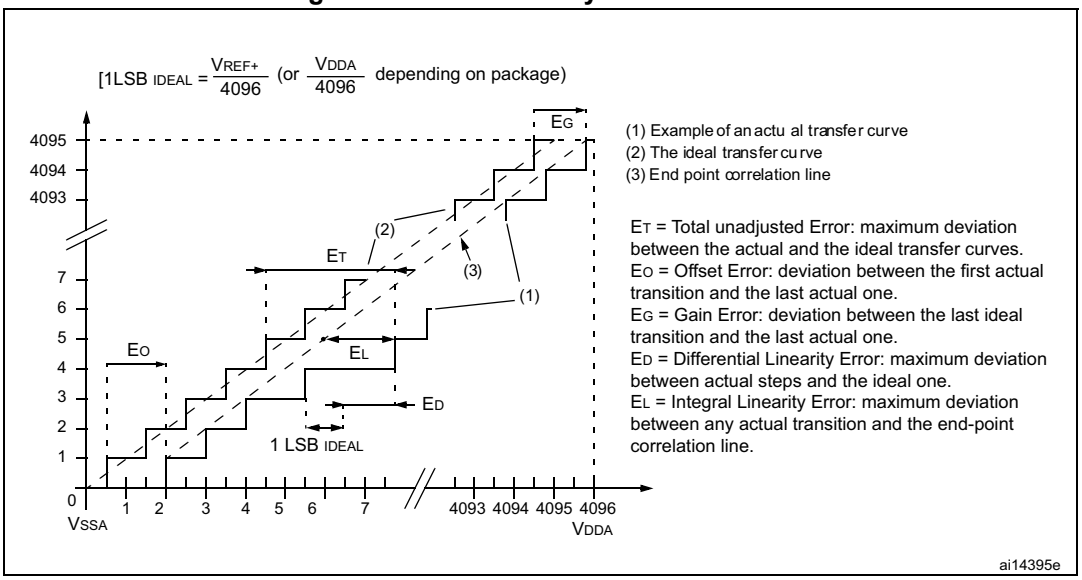
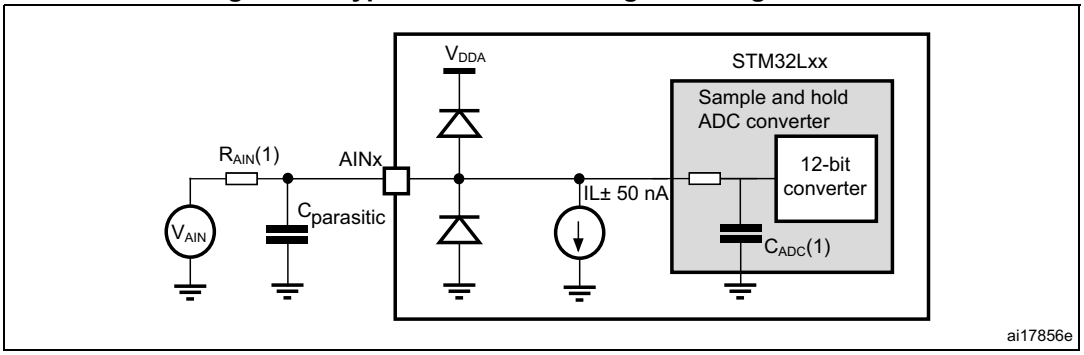


Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 58: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 56: ADC characteristics* for the value of C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.22 LCD controller

The device embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

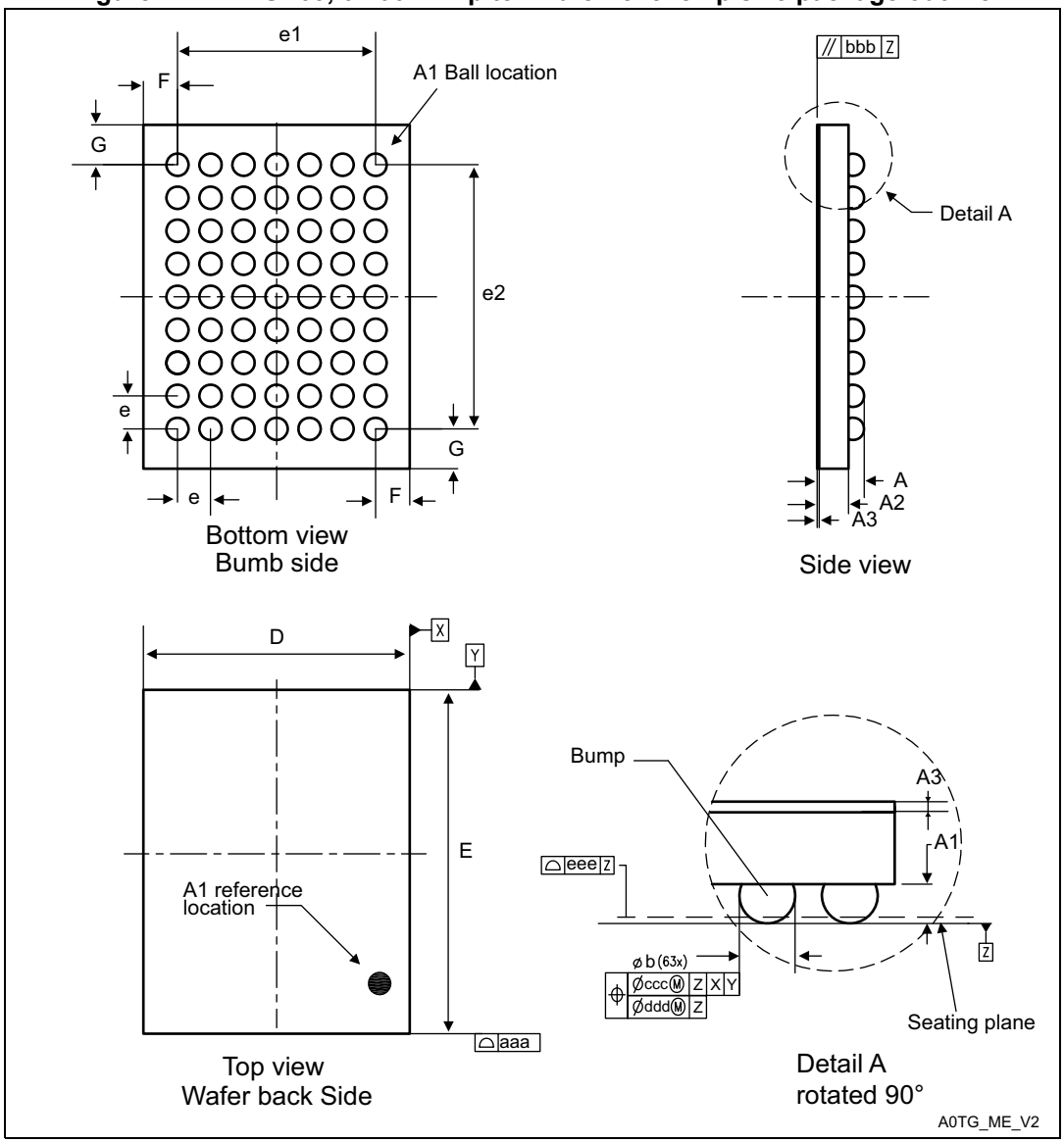
Table 65. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(3)	Segment/Common level voltage error T_A = -40 to 105 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

7.6 WLCSP63, 0.400 mm pitch wafer level chip size package information

Figure 47. WLCSP63, 0.400 mm pitch wafer level chip size package outline



1. Drawing is not to scale.

Table 72. WLCSP63, 0.400 mm pitch wafer level chip size package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0213	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
Øb	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	3.193	3.228	3.263	0.1257	0.1271	0.1285
E	4.129	4.164	4.199	0.1626	0.1639	0.1653
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	3.200	-	-	0.1260	-
F	-	0.414	-	-	0.0163	-
G	-	0.482	-		0.0190	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

9 Revision History

Table 75. Document revision history

Date	Revision	Changes
21-Feb-2012	1	Initial release.
12-Oct-2012	2	Added WLCSP63 package. Updated *Figure 1: Ultra-low-power STM32L162xC block diagram*. Changed maximum number of touch sensing channels to 34, and updated *Table 2: Ultralow power STM32L15xxC device features and peripheral counts*. Added *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*, and *Table 3: ange depending on dynamic voltage scaling*. Updated *Section 3.10: ADC (analog-to-digital converter)* to add *Section 3.10.1: Temperature sensor* and *Section 3.10.2: Internal voltage reference (VREFINT)*. Updated *Figure 3: STM32L162VC LQFP100 pinout*. *Table 10: STM32L15xxC pin definitions*: updated name of reference manual in footnote *5.* Changed I2C1_SMBAI into I2C1_SMBA in *Table 10: STM32L15xxC pin definitions*. Modified PB10/11/12 for AFIO4 alternate function, and replaced LBAR by NADV for AFIO12 in *Table 10: Alternate function input/output*. Removed caution note below *Figure 8: Power supply scheme*. Added *Note 2* in *Table 15: Embedded reset and power control block characteristics*. Updated *Table 14: General operating conditions*. Updated *Table 22: Typical and maximum current consumptions in Stop mode* and added *Note 6*. Updated *Table 23: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table :* . Updated *Table 26: Peripheral current consumption*. Updated *Table 60: SPI characteristics*, added *Note 1* and *Note 3*, and applied *Note 2* to $t_{r(SCK)}$, $t_{f(SCK)}$, $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{su(MI)}$, $t_{su(SI)}$, $t_{h(MI)}$, and $t_{h(SI)}$. Added *Table 61: I2S characteristics*, *Figure 29: I2S slave timing diagram (Philips protocol)(1)* and *Figure 30: I2S master timing diagram (Philips protocol)(1)*. Updated *Table 72: Temperature sensor characteristics*. Added *Figure 40: Thermal resistance*.