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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152cct6d

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer the user needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, the old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All the families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

3.1 Low-power modes

The ultra-low-power STM32L151xC and STM32L152xC devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V - 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep** mode

  This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xC and STM32L152xC devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xC and STM32L152xC devices embed a nested vectored interrupt controller able to handle up to 53 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1, USART2 or USB. See Application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

3.7 Memories

The STM32L151xC and STM32L152xC devices have the following features:

- 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 256 Kbytes of embedded Flash program memory
  - 8 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

  The user area of the Flash memory can be protected against Dbus read access by PCROP feature (see RM0038 for details).

3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART interfaces can be served by the DMA controller.

3.17.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

3.17.4 Inter-integrated sound (I^2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

3.17.5 Universal serial bus (USB)

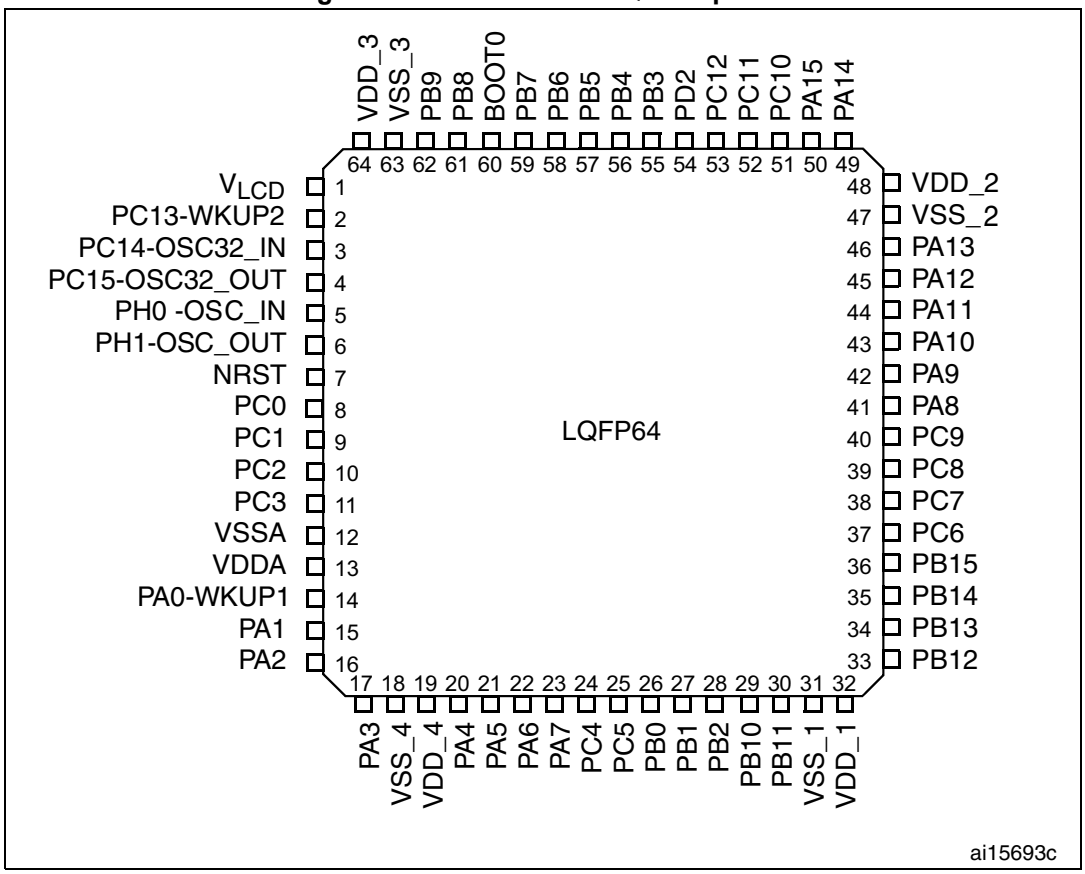
The STM32L151xC and STM32L152xC devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.18 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Figure 5. STM32L15xRC LQFP64 pinout



1. This figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151xC and STM32L152xC pin definitions

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT	PE2	TIM3_ETR/LCD_SEG38 /TRACECLK	-
A1	2	-	-	-	PE3	I/O	FT	PE3	TIM3_CH1/LCD_SEG39 /TRACED0	-
B1	3	-	-	-	PE4	I/O	FT	PE4	TIM3_CH2/TRACED1	-
C2	4	-	-	-	PE5	I/O	FT	PE5	TIM9_CH1/TRACED2	-
D2	5	-	-	-	PE6-WKUP3	I/O	FT	PE6	TIM9_CH2/ TRACED3	WKUP3/ RTC_TAMP3
E2	6	1	C7	1	V_{LCD}(3)	S	-	V_{LCD}	-	-

4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD}(2)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	I/O input voltage	FT pins; 2.0 V ≤V_{DD}	-0.3	5.5(3)	V
		FT pins; V_{DD} < 2.0 V	-0.3	5.25(3)	
		BOOT0 pin	0	5.5	
		Any other pin	-0.3	V_{DD}+0.3	
P_D	Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4)	LQFP48 package	-	364	mW
		LQFP100 package	-	465	
		LQFP64 package	-	435	
		UFQFPN48 package	-	625	
		UFBGA100	-	339	
		WLCSP63 package	-	408	

Table 22. Current consumption in Low-power sleep mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	4.4	-	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	14	16	
				T_A = 85 °C	19	23	
				T_A = 105 °C	27	33	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	15	17	
				T_A = 85 °C	20	23	
				T_A = 105 °C	28	33	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	18	21	
				T_A = 85 °C	22	25	
				T_A = 105 °C	30	35	
		TIM9 and USART1 enabled, Flash ON, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	14	16	
				T_A = 85 °C	19	22	
				T_A = 105 °C	27	32	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	15	17	
				T_A = 85 °C	20	23	
				T_A = 105 °C	28	33	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	18	21	
				T_A = 85 °C	22	25	
				T_A = 105 °C	30	36	
I_{DD} max (LP Sleep)	Max allowed current in Low-power sleep mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Multi-speed internal (MSI) RC oscillator

Table 33. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤105 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 44*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (3)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Guaranteed by test in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Table 53. USB: full speed electrical characteristics (continued)

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

I2S characteristics

Table 54. I2S characteristics

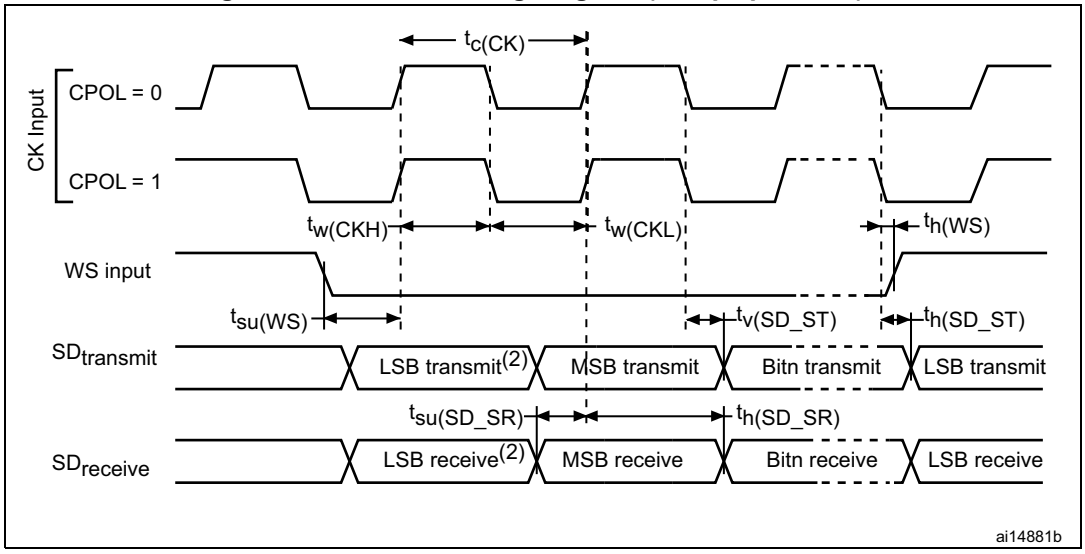
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main Clock Output		256 x 8K	256xFs [1]	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver, 48KHz	30	70	%
$t_{r(CK)}$	I2S clock rise time	Capacitive load CL=30pF	-	8	ns
$t_{f(CK)}$	I2S clock fall time			8	
$t_{v(WS)}$	WS valid time	Master mode	4	24	
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	15	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	8	-	
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	9	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	4	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	64	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	22	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	12	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8	-	

1. The maximum for 256xFs is 8 MHz

Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the

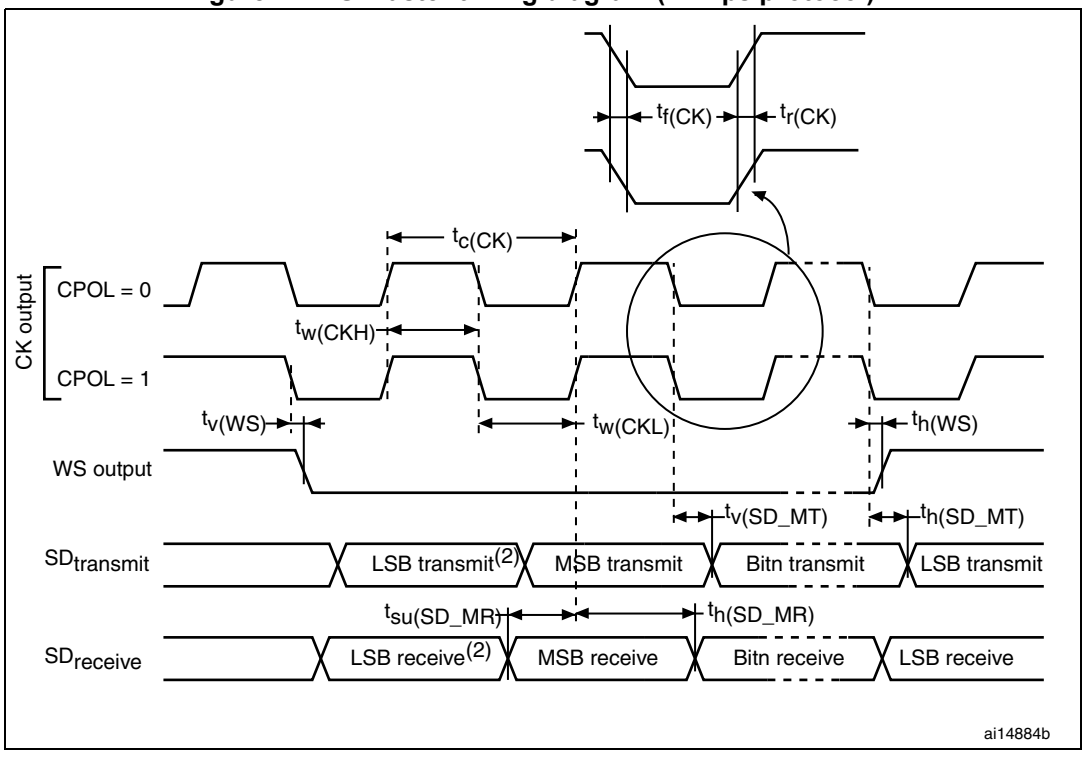
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 26. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 28. ADC accuracy characteristics

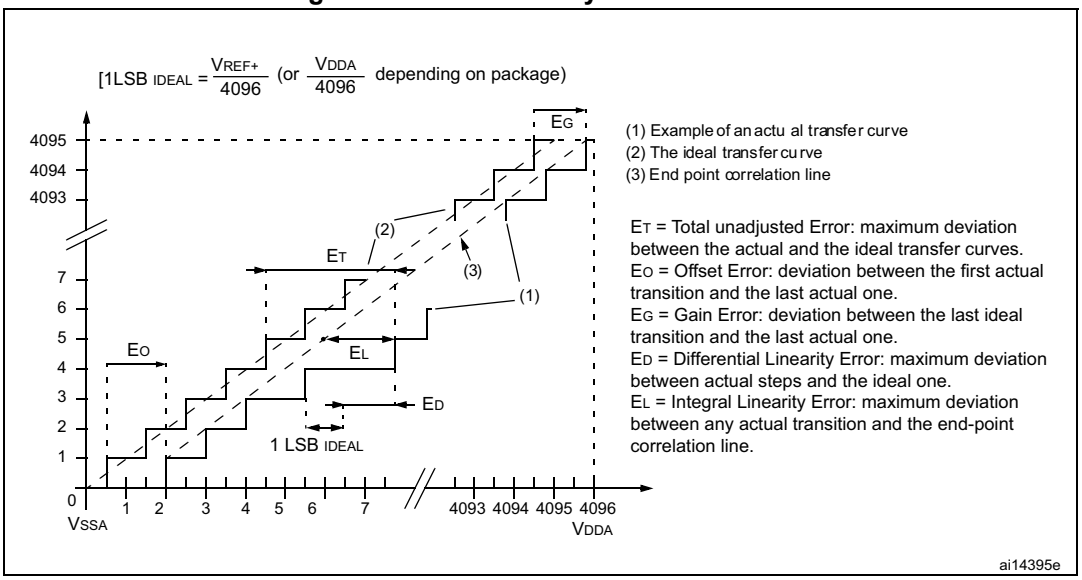
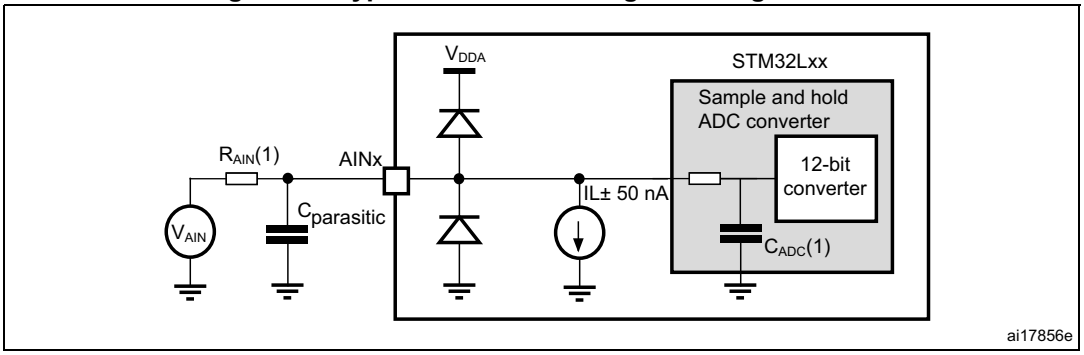


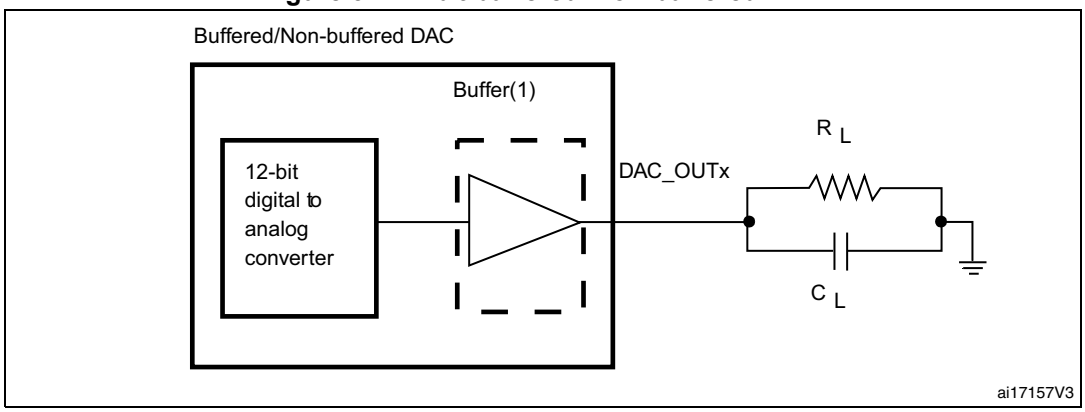
Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 58: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 56: ADC characteristics* for the value of C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
5. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
8. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 31. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Operational amplifier characteristics

Table 60. Operational amplifier characteristics

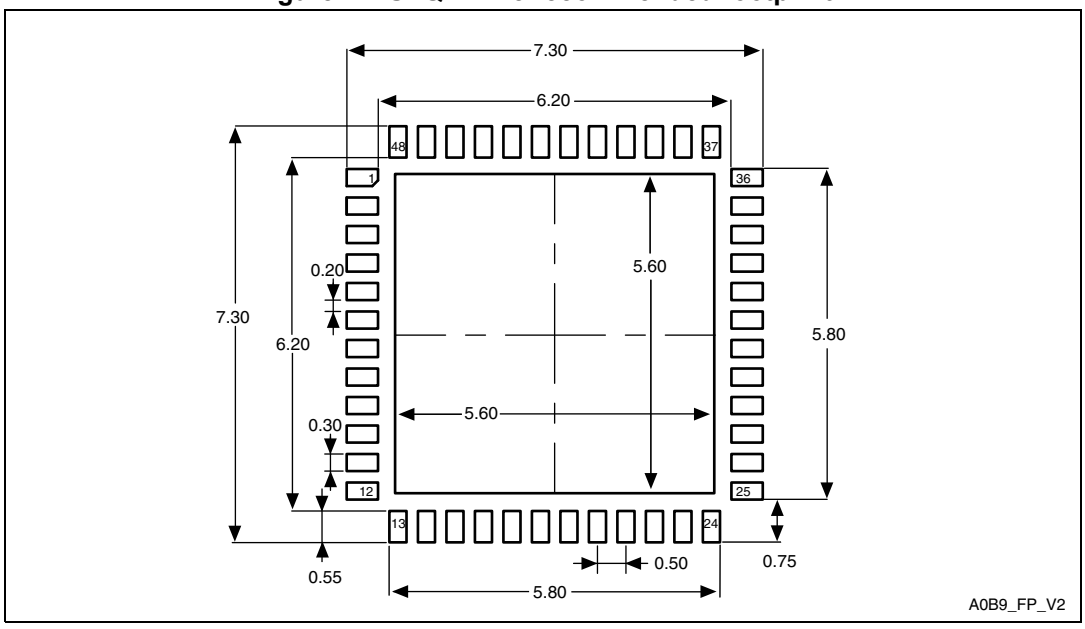
Symbol	Parameter		Condition(1)	Min(2)	Typ	Max(2)	Unit
CMIR	Common mode input range		-	0	-	V_{DD}	
VI_{OFFSET}	Input offset voltage	Maximum calibration range	-	-	-	±15	mV
		After offset calibration	-	-	-	±1.5	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	-	-	±40	µV/°C
		Low-power mode	-	-	-	±80	
I_{IB}	Input current bias	Dedicated input	75 °C	-	-	1	nA
		General purpose input		-	-	10	
I_{LOAD}	Drive current	Normal mode	-	-	-	500	µA
		Low-power mode	-	-	-	100	
I_{DD}	Consumption	Normal mode	No load, quiescent mode	-	100	220	µA
		Low-power mode		-	30	60	
CMRR	Common mode rejection ration	Normal mode	-	-	-85	-	dB
		Low-power mode	-	-	-90	-	

Table 69. UFQFPN48 – ultra thin fine pitch quad flat pack no-lead 7 × 7 mm, 0.5 mm pitch package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. UFQFPN48 recommended footprint

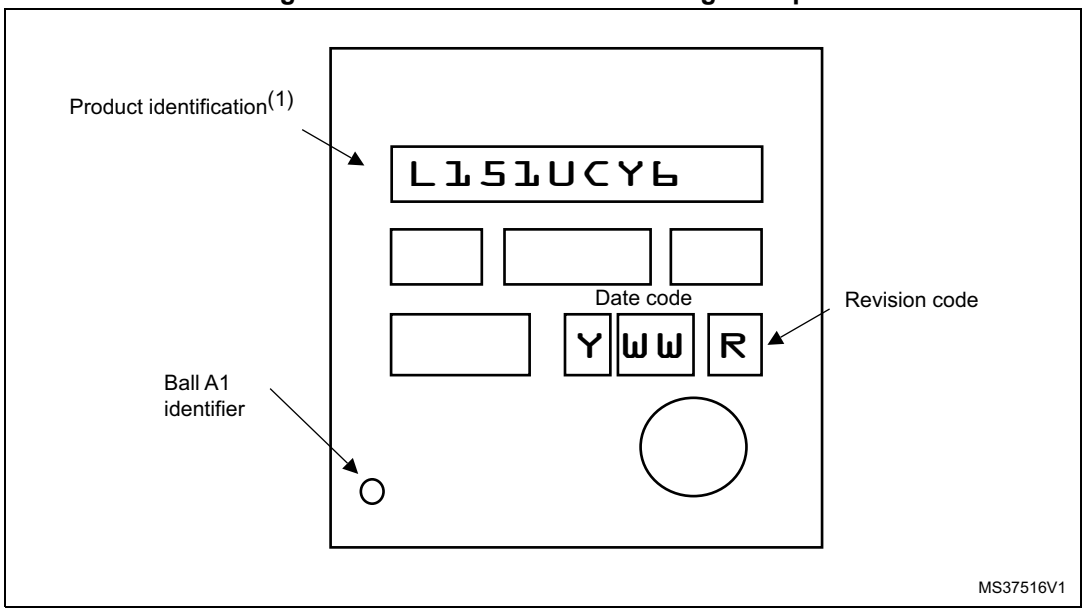


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 48. WLCSP63 device marking example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

9 Revision History

Table 75. Document revision history

Date	Revision	Changes
21-Feb-2012	1	Initial release.
12-Oct-2012	2	Added WLCSP63 package. Updated *Figure 1: Ultra-low-power STM32L162xC block diagram*. Changed maximum number of touch sensing channels to 34, and updated *Table 2: Ultralow power STM32L15xxC device features and peripheral counts*. Added *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*, and *Table 3: ange depending on dynamic voltage scaling*. Updated *Section 3.10: ADC (analog-to-digital converter)* to add *Section 3.10.1: Temperature sensor* and *Section 3.10.2: Internal voltage reference (VREFINT)*. Updated *Figure 3: STM32L162VC LQFP100 pinout*. *Table 10: STM32L15xxC pin definitions*: updated name of reference manual in footnote *5.* Changed I2C1_SMBAI into I2C1_SMBA in *Table 10: STM32L15xxC pin definitions*. Modified PB10/11/12 for AFIO4 alternate function, and replaced LBAR by NADV for AFIO12 in *Table 10: Alternate function input/output*. Removed caution note below *Figure 8: Power supply scheme*. Added *Note 2* in *Table 15: Embedded reset and power control block characteristics*. Updated *Table 14: General operating conditions*. Updated *Table 22: Typical and maximum current consumptions in Stop mode* and added *Note 6*. Updated *Table 23: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table :* . Updated *Table 26: Peripheral current consumption*. Updated *Table 60: SPI characteristics*, added *Note 1* and *Note 3*, and applied *Note 2* to $t_{r(SCK)}$, $t_{f(SCK)}$, $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{su(MI)}$, $t_{su(SI)}$, $t_{h(MI)}$, and $t_{h(SI)}$. Added *Table 61: I2S characteristics*, *Figure 29: I2S slave timing diagram (Philips protocol)(1)* and *Figure 30: I2S master timing diagram (Philips protocol)(1)*. Updated *Table 72: Temperature sensor characteristics*. Added *Figure 40: Thermal resistance*.