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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rct6

3.12 Operational amplifier

The STM32L151xC and STM32L152xC devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.13 Ultra-low-power comparators and reference voltage

The STM32L151xC and STM32L152xC devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.15 Touch sensing

The STM32L151xC and STM32L152xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation

introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.16 Timers and watchdogs

The ultra-low-power STM32L151xC and STM32L152xC devices include seven general-purpose timers, two basic timers, and two watchdog timers.

Table 7 compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xC and STM32L152xC devices (see *Table 7* for differences).

TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
M6	36	27	H3	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
L6	37	28	G3	20	PB2	I/O	FT	PB2 /BOOT1	BOOT1	VLCDRAIL1/ ADCIN0b
M7	38	-	-	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
L7	39	-	-	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
M8	40	-	-	-	PE9	-	TC	PE9	TIM2_CH1_ETR/ TIM5_ETR	ADC_IN24/ COMP1_INP
L8	41	-	-	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
M9	42	-	-	-	PE11	I/O	FT	PE11	TIM2_CH3	VLCDRAIL2
L9	43	-	-	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	VLCDRAIL3
M10	44	-	-	-	PE13	I/O	FT	PE13	SPI1_SCK	-
M11	45	-	-	-	PE14	I/O	FT	PE14	SPI1_MISO	-
M12	46	-	-	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
L10	47	29	J2	21	PB10	I/O	FT	PB10	TIM2_CH3/I2C2_SCL/ USART3_TX/ LCD_SEG10	-
L11	48	30	H2	22	PB11	I/O	FT	PB11	TIM2_CH4/I2C2_SDA/ USART3_RX/ LCD_SEG11	-
-	-	-	H5	-	V_{SS}	S	-	V_{SS}	-	-
F12	49	31	J1	23	V_{SS_1}	S	-	V_{SS_1}	-	-
G12	50	32	H1	24	V_{DD_1}	S	-	V_{DD_1}	-	-

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation(5)	–40	85	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	110	

1. When the ADC is used, refer to *Table 56: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and up to 140 mV in operation.
3. To sustain a voltage higher than VDD+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 73: Thermal characteristics on page 128*).
5. In low-power dissipation state, T_A can be extended to -40°C to 105°C temperature range as long as T_J does not exceed T_J max (see *Table 73: Thermal characteristics on page 128*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the conditions summarized in *Table 14*.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

6.3.3 Embedded internal reference voltage

The parameters given in *Table 17* are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$ (1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3) (4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current (5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.

Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	185	240	µA
				2 MHz	345	410	
				4 MHz	645	880(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.755	1.4	mA
				8 MHz	1.5	2.1	
				16 MHz	3	3.5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.8	2.8	
				16 MHz	3.6	4.1	
				32 MHz	7.15	8.3	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	2.95	3.5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.15	8.4	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	38.5	85	µA
		MSI clock, 524 kHz		524 kHz	110	160	
		MSI clock, 4.2 MHz		4.2 MHz	690	810	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).
3. Guaranteed by test in production.

Table 21. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	8.6	12	µA
				T_A = 85 °C	19	25	
				T_A = 105 °C	35	47	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	14	16	
				T_A = 85 °C	24	29	
				T_A = 105 °C	40	51	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	26	29	
				T_A = 55 °C	28	31	
				T_A = 85 °C	36	42	
				T_A = 105 °C	52	64	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	20	24	
				T_A = 85 °C	32	37	
				T_A = 105 °C	49	61	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	26	30	
				T_A = 85 °C	38	44	
				T_A = 105 °C	55	67	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	41	46	
				T_A = 55 °C	44	50	
				T_A = 85 °C	56	87	
				T_A = 105 °C	73	110	
I_{DD} max (LP Run)	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.8	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.435	1	
			T_A = 55°C	0.99	3	
			T_A= 85°C	2.4	9	
			T_A = 105°C	5.5	22(5)	
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	MSI = 4.2 MHz	T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(6)		1.45	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
3. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Guaranteed by test in production.
6. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining part of the wakeup period, the current corresponds the Run mode current.

Table 33. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.13 I/O port characteristics

General input/output characteristics

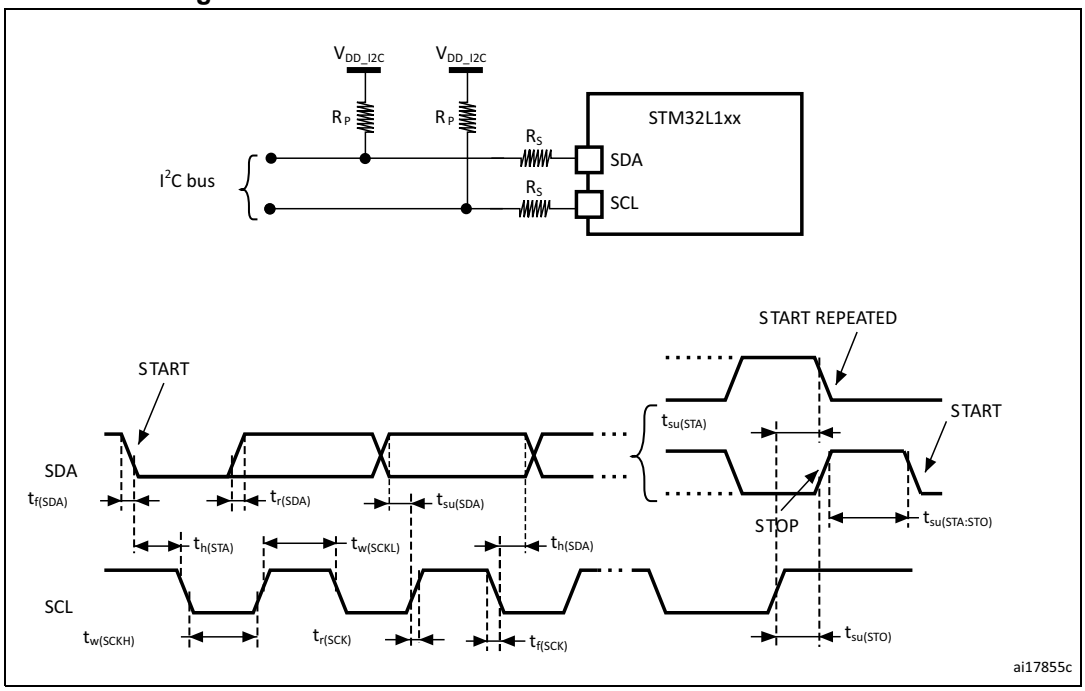
Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-	-	0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/Os	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	µA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 21. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 14*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Figure 28. ADC accuracy characteristics

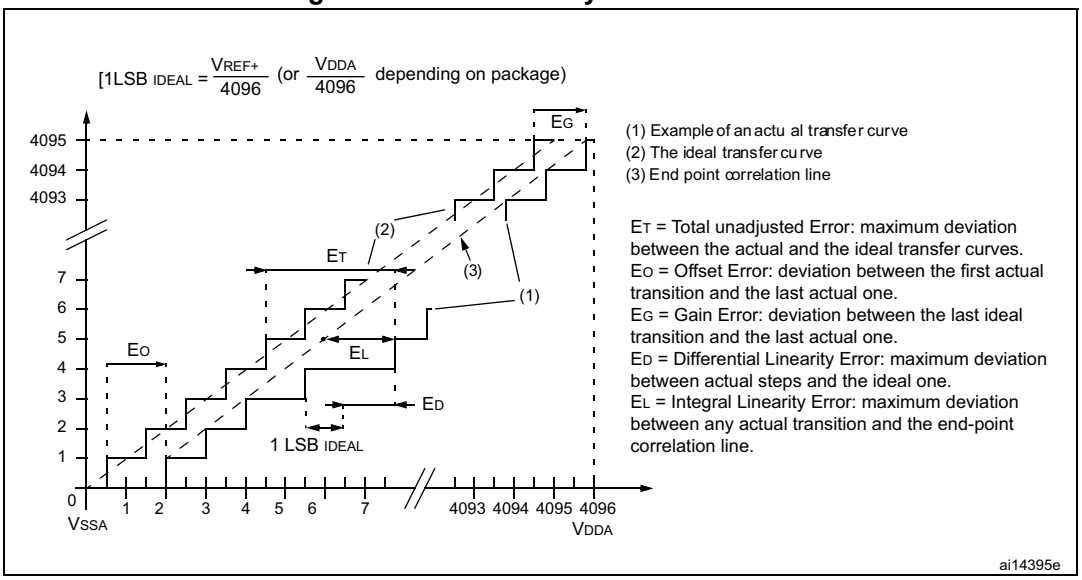
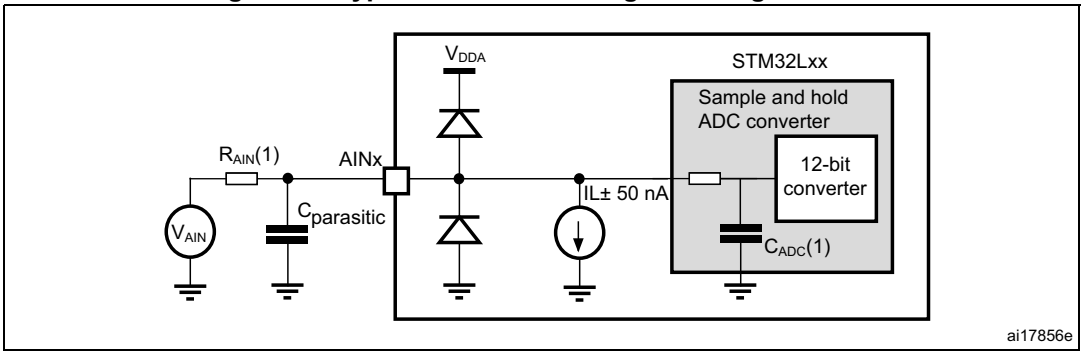


Figure 29. Typical connection diagram using the ADC

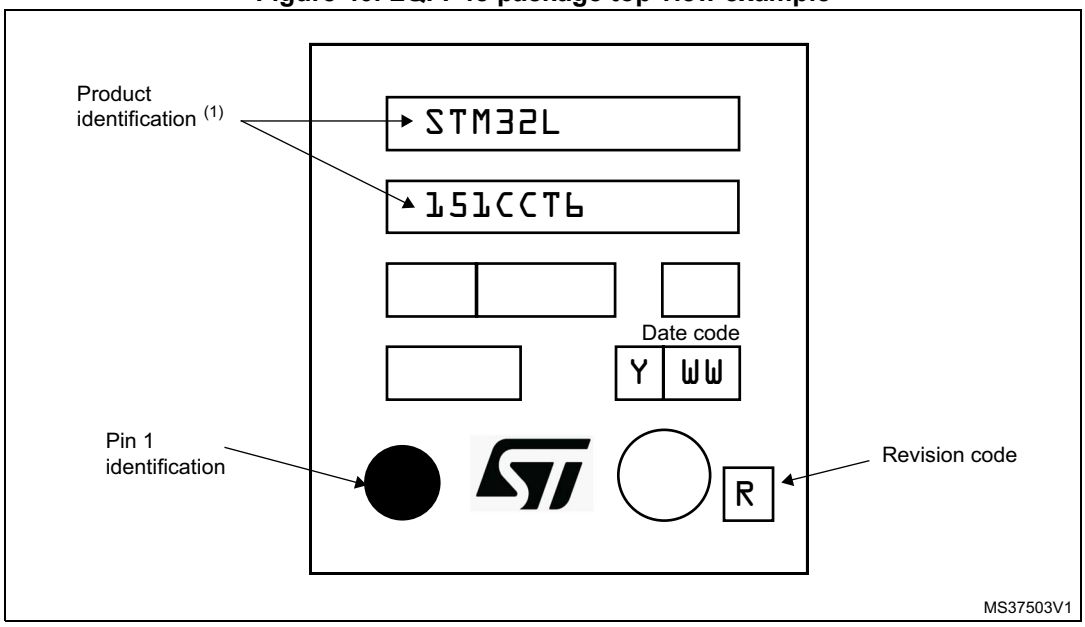


1. Refer to *Table 58: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 56: ADC characteristics* for the value of C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

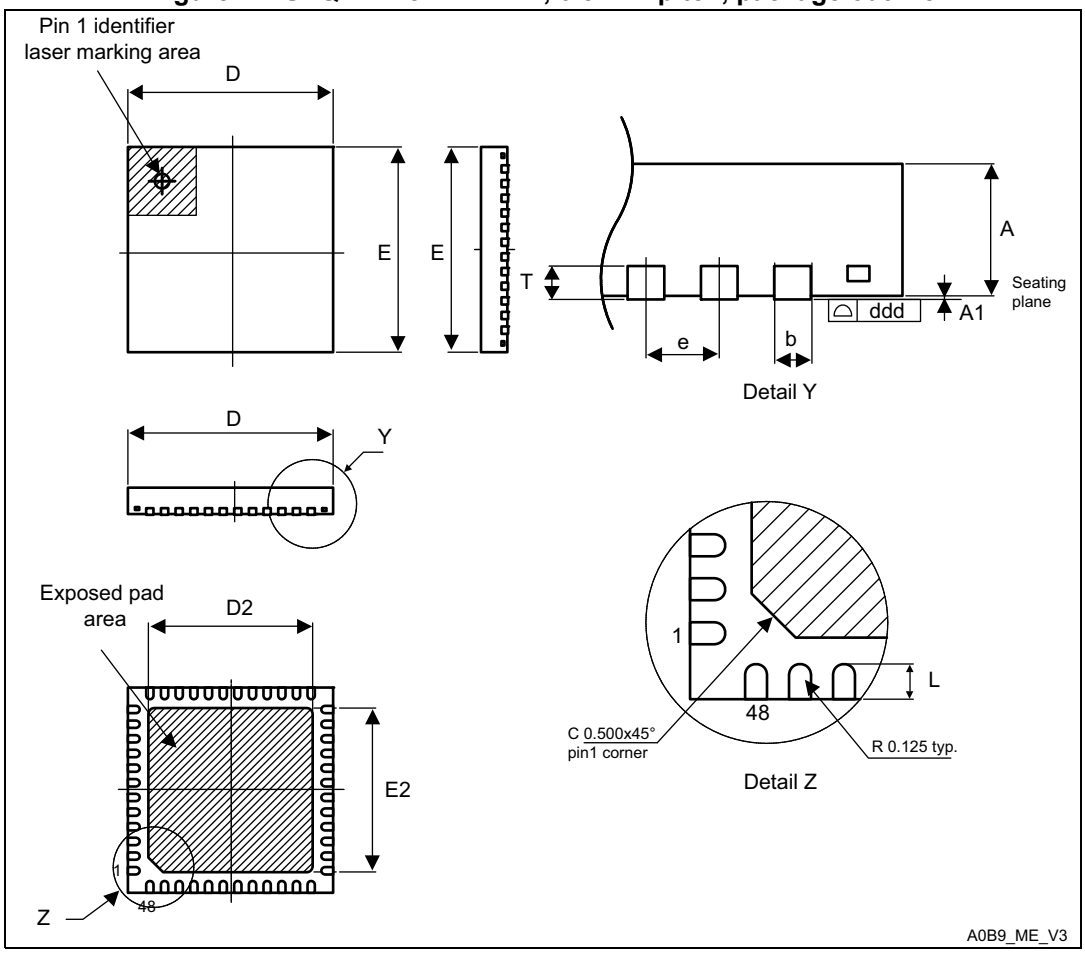
Figure 40. LQFP48 package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline



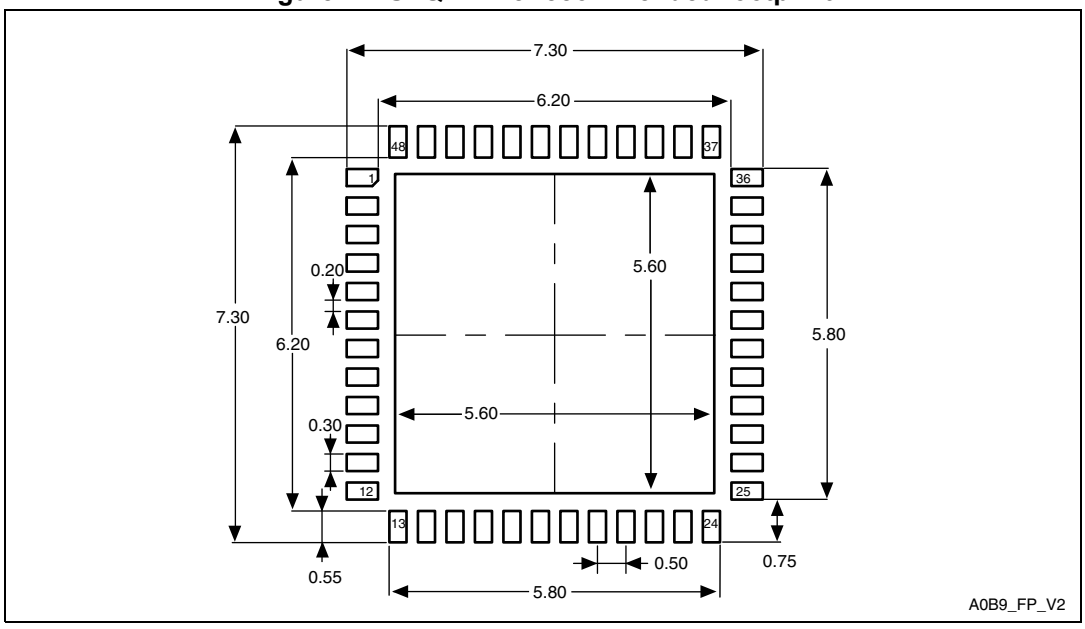
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 69. UFQFPN48 – ultra thin fine pitch quad flat pack no-lead 7 × 7 mm, 0.5 mm pitch package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

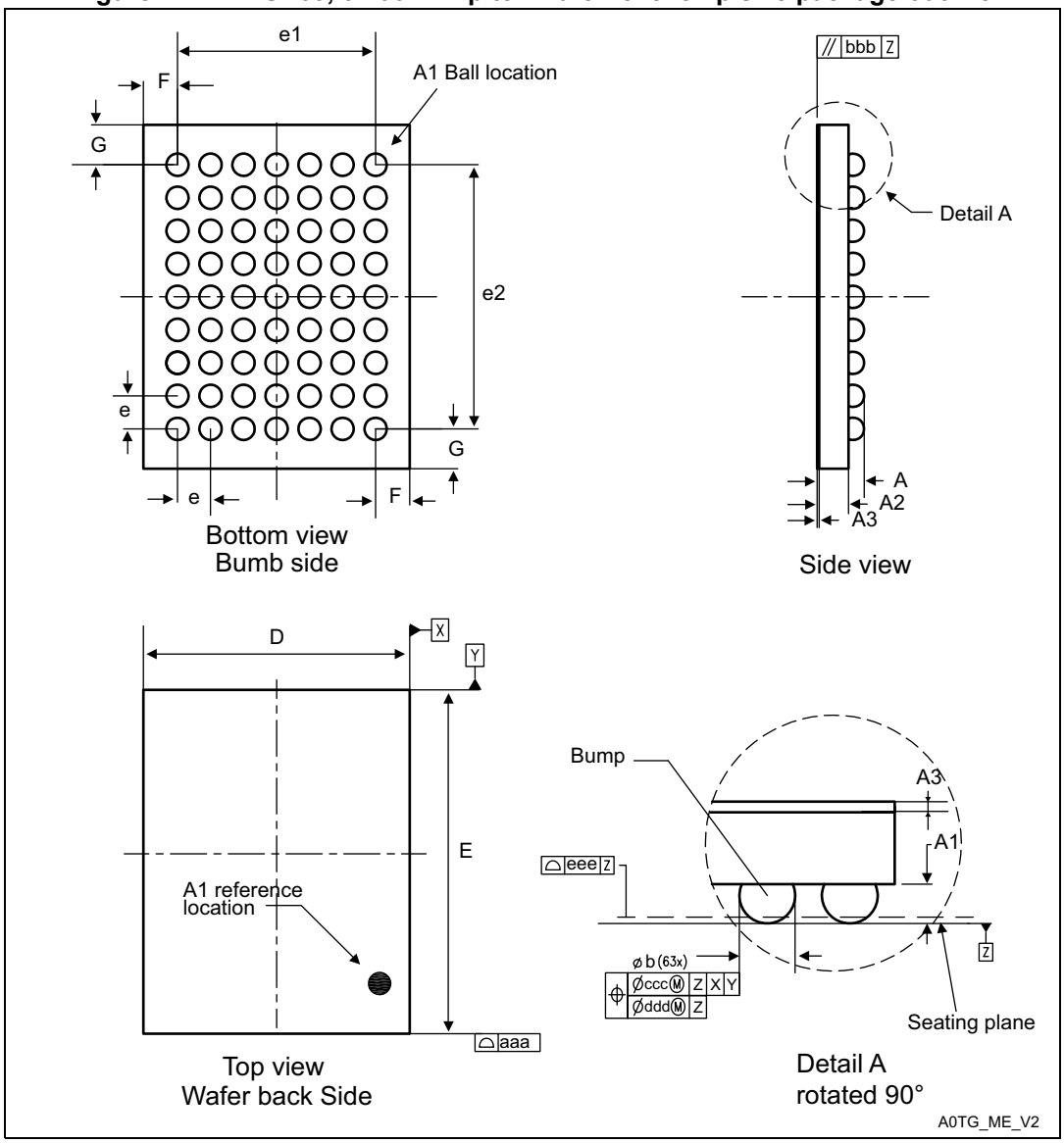
Figure 42. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

7.6 WLCSP63, 0.400 mm pitch wafer level chip size package information

Figure 47. WLCSP63, 0.400 mm pitch wafer level chip size package outline



1. Drawing is not to scale.