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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rct6d

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

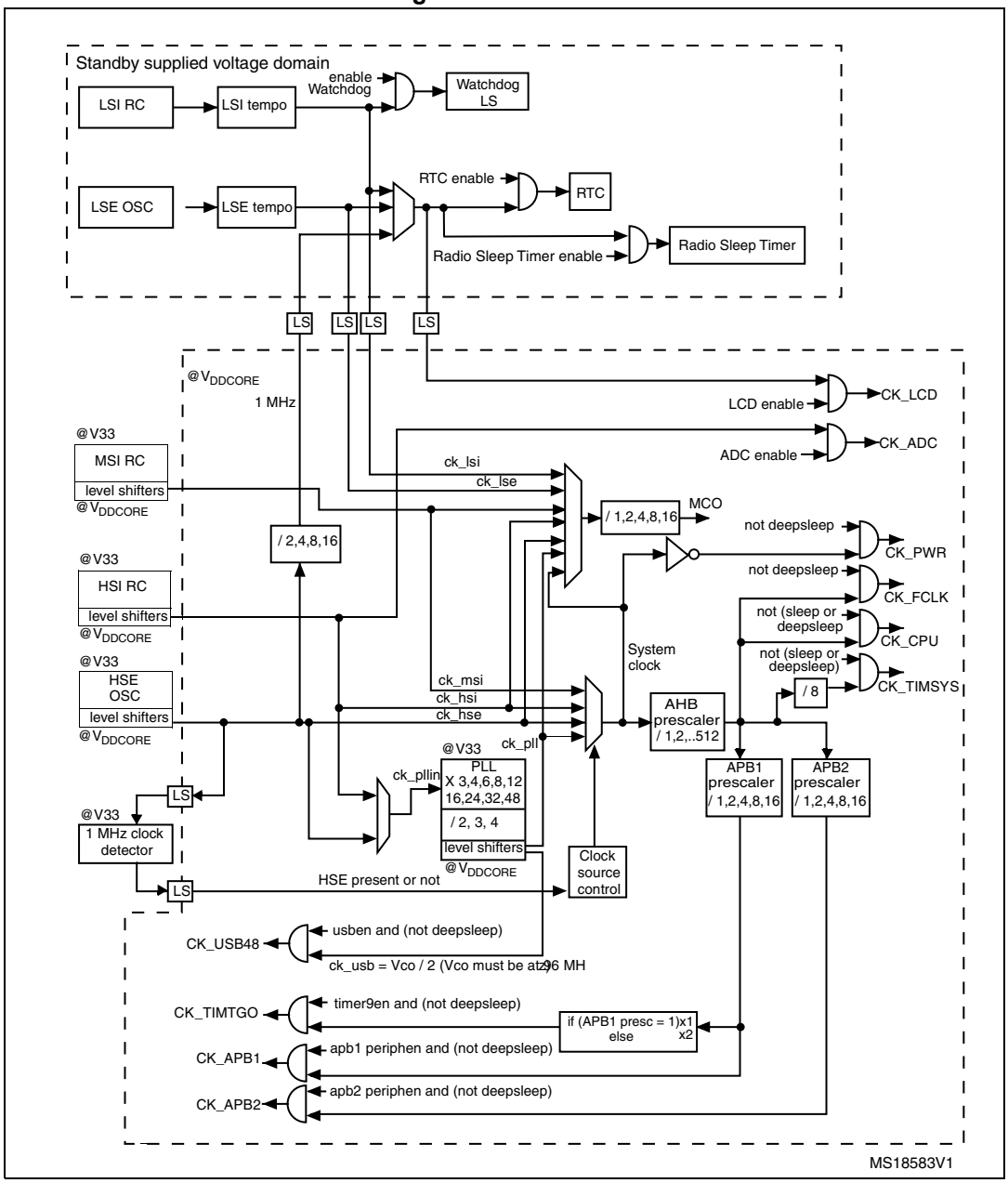
  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Figure 2. Clock tree



TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.16.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.16.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17 Communication interfaces

3.17.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART interfaces can be served by the DMA controller.

3.17.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

3.17.4 Inter-integrated sound (I^2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

3.17.5 Universal serial bus (USB)

The STM32L151xC and STM32L152xC devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.18 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Table 8. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151xC and STM32L152xC pin definitions

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT	PE2	TIM3_ETR/LCD_SEG38 /TRACECLK	-
A1	2	-	-	-	PE3	I/O	FT	PE3	TIM3_CH1/LCD_SEG39 /TRACED0	-
B1	3	-	-	-	PE4	I/O	FT	PE4	TIM3_CH2/TRACED1	-
C2	4	-	-	-	PE5	I/O	FT	PE5	TIM9_CH1/TRACED2	-
D2	5	-	-	-	PE6-WKUP3	I/O	FT	PE6	TIM9_CH2/ TRACED3	WKUP3/ RTC_TAMP3
E2	6	1	C7	1	V_{LCD}(3)	S	-	V_{LCD}	-	-

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type[1]	I / O Structure	Main function[2] (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
E11	64	38	E1	-	PC7	I/O	FT	PC7	TIM3_CH2/I2S3_MCK/ LCD_SEG25	-
E10	65	39	D1	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
D12	66	40	E2	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
D11	67	41	E3	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
D10	68	42	C1	30	PA9	I/O	FT	PA9	USART1_TX/ LCD_COM1	-
C12	69	43	D2	31	PA10	I/O	FT	PA10	USART1_RX/ LCD_COM2	-
B12	70	44	B1	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM
A12	71	45	D3	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
A11	72	46	C2	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
C11	73	-	-	-	PH2	I/O	FT	PH2	-	-
F11	74	47	A1	35	V_{SS_2}	S	-	V_{SS_2}	-	-
G11	75	48	B2	36	V_{DD_2}	S	-	V_{DD_2}	-	-
A10	76	49	C3	37	PA14	I/O	FT	JTCK-SWCLK	JTCK-SWCLK	-
A9	77	50	A2	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/ SPI1_NSS/ SPI3_NSS/I2S3_WS/ LCD_SEG17/JTDI	-
B11	78	51	B3	-	PC10	I/O	FT	PC10	SPI3_SCK/I2S3_CK/ USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4	-

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number								. .		. .		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7		AFIO11		AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
PC4	-	-	-	-	-	-	-	-		SEG22		TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-		SEG23		TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-		SEG24		TIMx_IC3	EVENT OUT
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-		SEG25		TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-		SEG26		TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-		SEG27		TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX		COM4/ SEG28/ SEG40		TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX		COM5/ SEG29 /SEG41		TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK		COM6/ SEG30/ SEG42		TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-		-		TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-		-		TIMx_IC3	EVENT OUT
PC15 OSC32_ OUT	-	-	-	-	-	-	-	-		-		TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-		-		TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-		-		TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-		COM7/ SEG31/ SEG43		TIMx_IC3	EVENT OUT

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

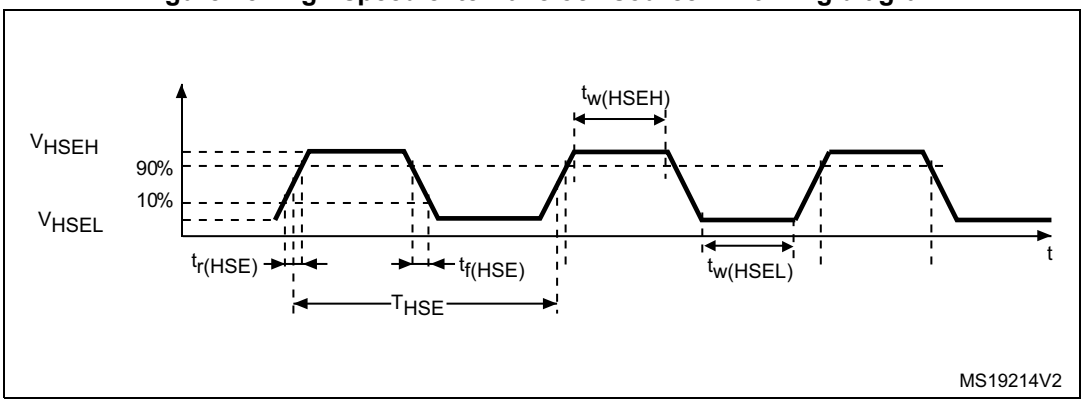
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 27. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram



Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation, LCD levels).

The test results are given in the *Table 42*.

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all 5 V tolerant (FT) pins	-5 (1)	NA	mA
	Injected current on BOOT0	-0	NA	
	Injected current on any other pin	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

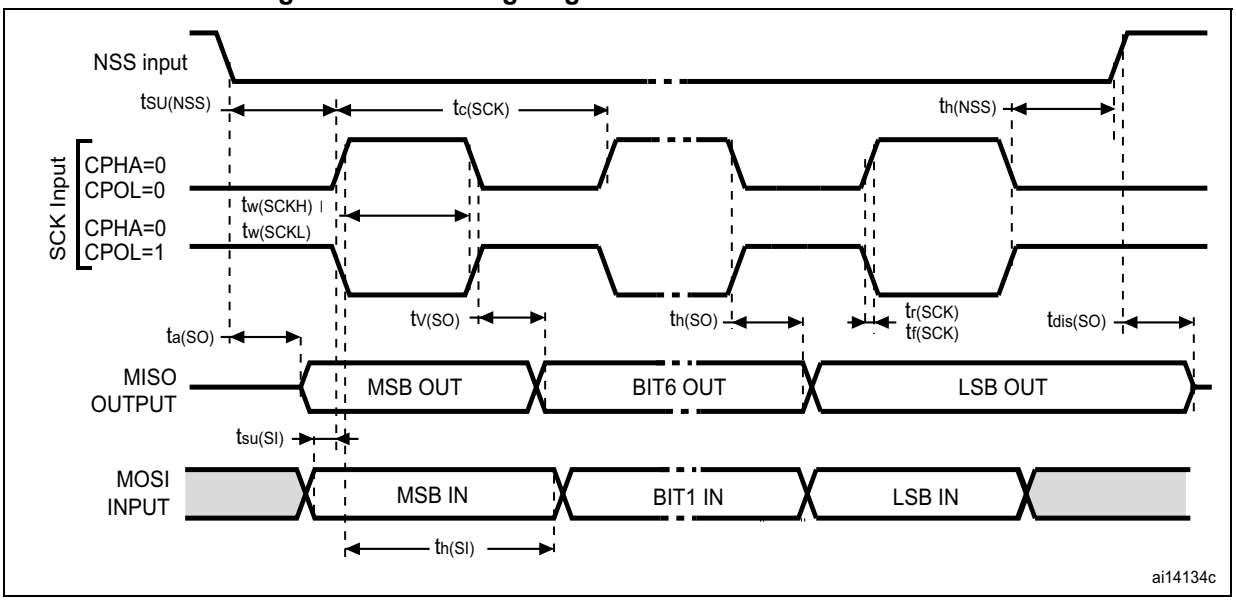
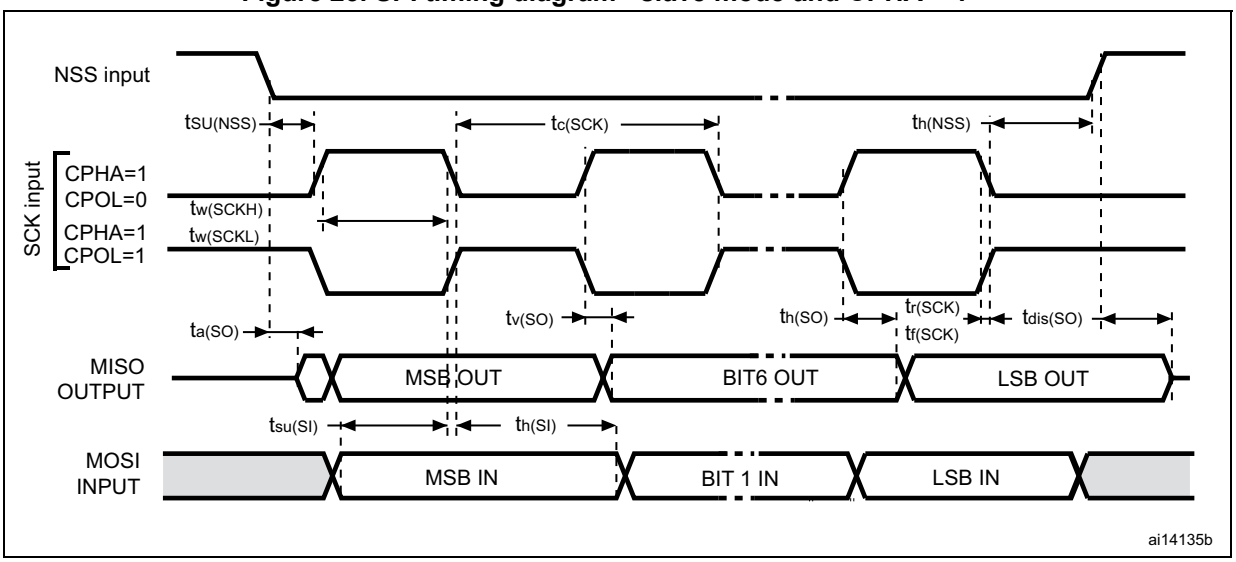


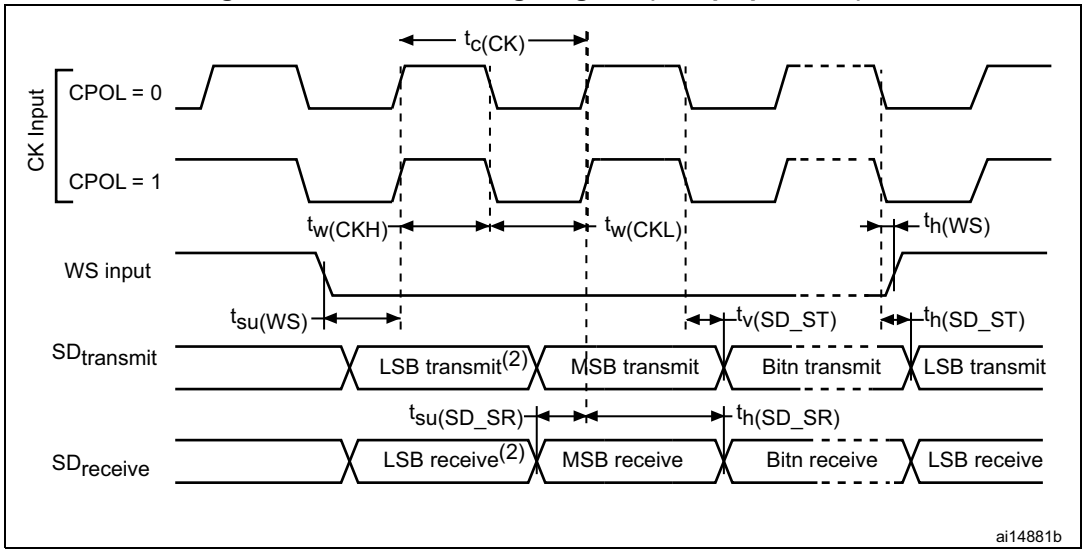
Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

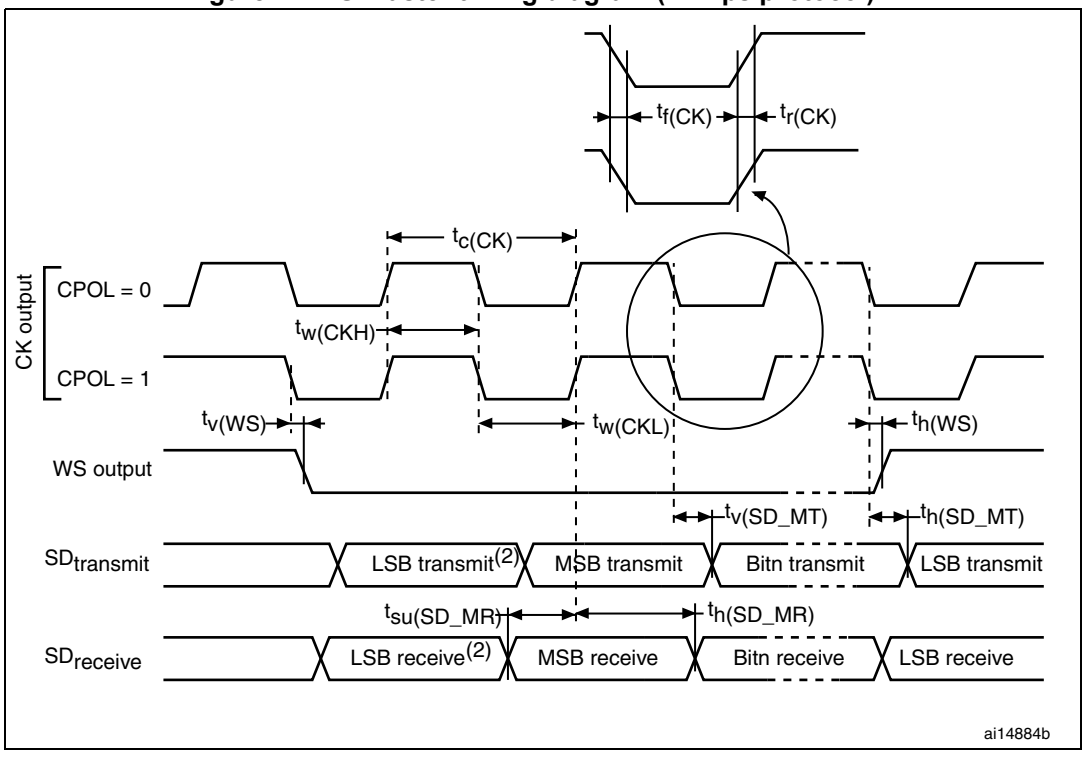
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 26. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 60. Operational amplifier characteristics (continued)

Symbol	Parameter		Condition(1)	Min(2)	Typ	Max(2)	Unit
PSRR	Power supply rejection ratio	Normal mode	DC	-	-85	-	dB
		Low-power mode		-	-90	-	
GBW	Bandwidth	Normal mode	V_{DD}>2.4 V	400	1000	3000	kHZ
		Low-power mode		150	300	800	
		Normal mode	V_{DD}<2.4 V	200	500	2200	
		Low-power mode		70	150	800	
SR	Slew rate	Normal mode	V_{DD}>2.4 V (between 0.1 V and V_{DD}-0.1 V)	-	700	-	V/ms
		Low-power mode	V_{DD}>2.4 V	-	100	-	
		Normal mode	V_{DD}<2.4 V	-	300	-	
		Low-power mode		-	50	-	
AO	Open loop gain	Normal mode		55	100	-	dB
		Low-power mode		65	110	-	
R_L	Resistive load	Normal mode	V_{DD}<2.4 V	4	-	-	kΩ
		Low-power mode		20	-	-	
C_L	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage	Normal mode	I_{LOAD} = max or R_L = min	V_{DD}-100	-	-	mV
		Low-power mode		V_{DD}-50	-	-	
VOL_{SAT}	Low saturation voltage	Normal mode		-	-	100	
		Low-power mode		-	-	50	
φm	Phase margin		-	-	60	-	°
GM	Gain margin		-	-	-12	-	dB
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	1	-	ms
t_{WAKEUP}	Wakeup time	Normal mode	C_L ≤50 pf, R_L ≥ 4 kΩ	-	10	-	µs
		Low-power mode	C_L ≤50 pf, R_L ≥ 20 kΩ	-	30	-	

1. Operating conditions are limited to junction temperature (0 °C to 105 °C) when V_{DD} is below 2 V. Otherwise to the full ambient temperature range (-40 °C to 85 °C, -40 °C to 105 °C).
2. Guaranteed by characterization results.

6.3.20 Temperature sensor characteristics

Table 61. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FA - 0x1FF8 00FB
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FE - 0x1FF8 00FF

Table 62. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	4	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.

6.3.21 Comparator

Table 63. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}$/dt	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

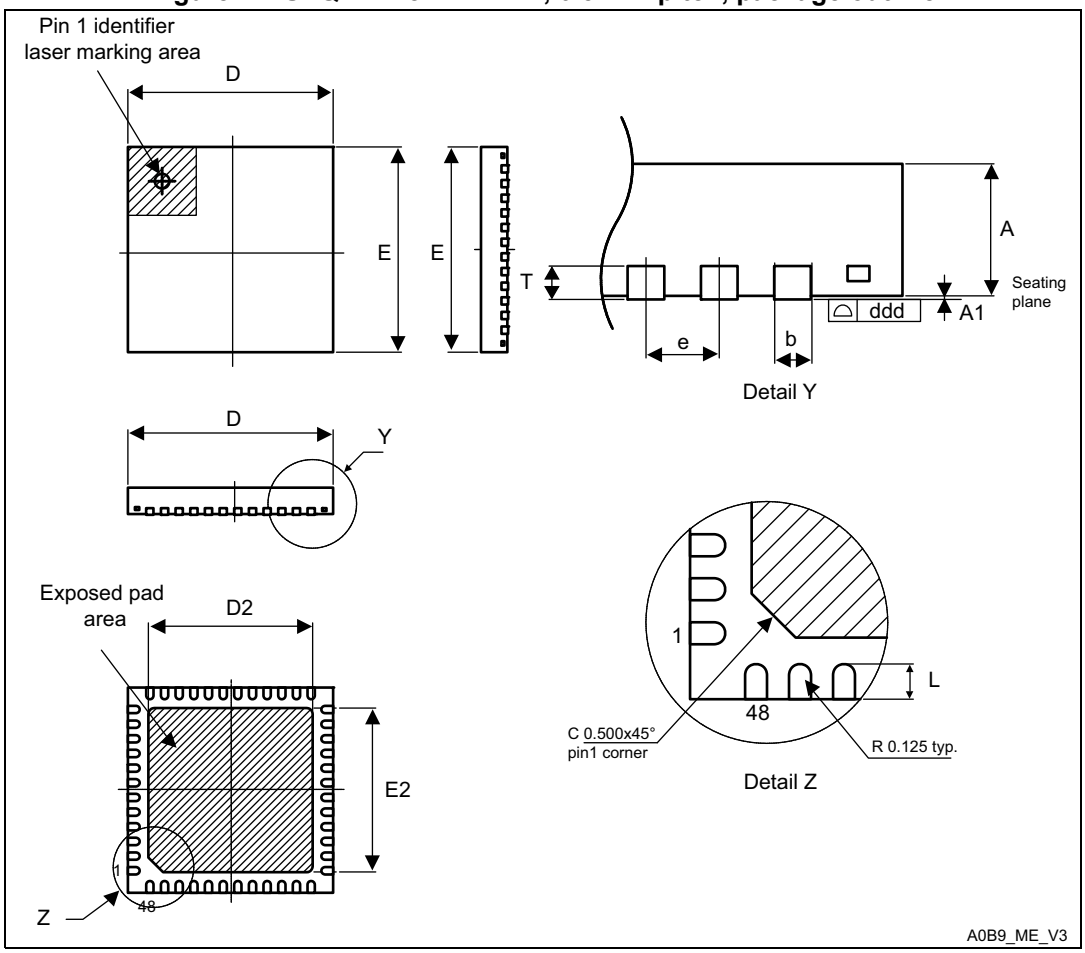
Table 64. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤V_{DDA} ≤2.7 V	-	1.8	3.5	
		2.7 V ≤V_{DDA} ≤3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤V_{DDA} ≤2.7 V	-	0.8	2	
		2.7 V ≤V_{DDA} ≤3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- =V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	100	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 70. UFBGA100, 7 x 7 mm, 0.5 mm pitch package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFBGA100, 7 x 7 mm, 0.5 mm pitch, package recommended footprint

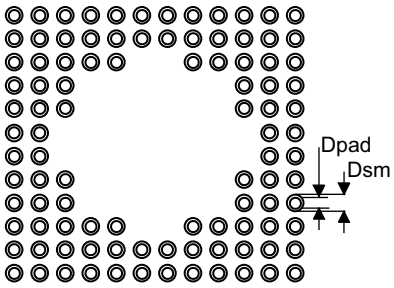


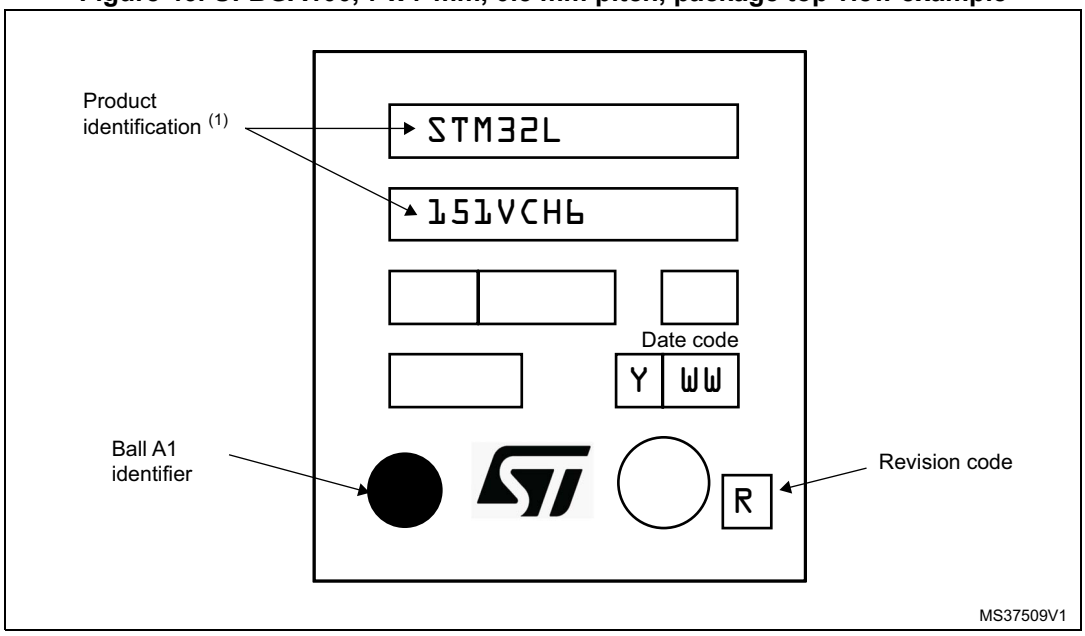
Table 71. UFBGA100, 7 x 7 mm, 0.50 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 46. UFBGA100, 7 x 7 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Table 75. Document revision history (continued)

Date	Revision	Changes
01-Feb-2013	3	Removed AHB1/AHB2 and corrected typo on APB1/APB2 in:*Figure 1: Ultra-low-power STM32L162xC block diagram-low-power STM32L162xC block diagram* Updated “OP amp” line in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Added IWDG and WWDG rows in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Updated address range in *Table 7: Internal voltage reference measured values* The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)” in table *Table 27: Current consumption in Sleep mode* replaced pin names D7,C7,C6,C8,B8,A8 respectively by D11,D10,C12,B12,A12,A11 in column UFBGA100 of *Table 9: STM32L15xxC pin definitions*Added more alternate functions supported on pin K3 and M4 for UFBGA100 package in *Table 9: STM32L15xxC pin definitions* Added part number STM32L151CC in *Table 1: Device summary* Updated Stop mode current to 1.5 µA in *Ultra-low-power platform* Updated entire *Section 7: Package information*
02-Sep-2013	4	Removed UFBGA132 and LQFP144 packages Removed first sentence in *Section : I2C interface characteristics* Added *Section Table 5.: V_{LCD} rail decoupling* Added VRAIL functions in *Table 9: STM32L15xxC pin definitions* Updated PH0-OSC_IN and PH1-OSC_OUT type in *Table 9: STM32L15xxC pin definitions*. Added *Table 6.1.7: Optional LCD power supply scheme*. Updated consumption data in *Table 6.3.4: Supply current characteristics* Updated *Table 7: Pin loading conditions* Updated *Table 8: Pin input voltage* Updated *Table 15: Typical application with a 32.768 kHz crystal* Updated *Table 25: Recommended NRST pin protection* *Table 26: I^2C bus AC waveforms and measurement circuit*Updated *Table 35: Typical connection diagram using the ADC* and definition of symbol “RAIN” in *Table 77: ADC characteristics* Updated dThreshold/dt conditions in *Table 85: Comparator 2 characteristics*. Updated *Table 49: Thermal resistance suffix 6*. Added D2 and E2 in *Table 69: UFQFPN48 – ultra thin fine pitch quad flat pack no-lead 7 × 7 mm, 0.5 mm pitch package mechanical data* Fixed columns inversion in *Table 67: LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data* and *Table 70: UFBGA100, 7 x 7 mm, 0.5 mm pitch package mechanical data*

Table 75. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	5	Updated *Section 3.15: Touch sensing*. Added V_{DD}= 1.71 to 1.8 V operating power supply range in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Renamed "I/O Level" to "I/O structure" in *Table 9: STM32L15xxC pin definitions*, added the I/O structure for PC14, PC15, PC3, PH0, PH1, PA3, PA4, PA5, PB0, PE7, PE8, PE9, PE10, NRST and BOOT0 Updated *Table 10: Voltage characteristics* added row Updated *Table 11: Current characteristics* replaced with the one inside STM32L15xxBxxA datasheet. Updated *Table 13: General operating conditions*, footnote and added row. Updated *Table 15: Embedded internal reference voltage calibration values* and moved inside *Section 6.3.3: Embedded internal reference voltage* Updated *Section 6.3.4: Supply current characteristics*. Updated *Table 19: Current consumption in Run mode, code with data processing running from Flash*. Updated *Table 22: Current consumption in Run mode, code with data processing running from RAM*. Created *Section 6.3.5: Wakeup time from low-power mode*.. Updated *Table 38: High-speed external user clock characteristics*. Moved *Figure 12: High-speed external clock source AC timing diagram* after *Table 38: High-speed external user clock characteristics*. Updated *Table 40: HSE oscillator characteristics*. Updated *Section 6.3.12: Electrical sensitivity characteristics* (title). Updated *Section 6.3.13: I/O current injection characteristics*. Updated *Table 61: I/O current injection susceptibility* and added footnote. Updated *Table 63: I/O static characteristics* Updated *Section 6.3.15: NRST pin characteristics*. Updated *Table 77: ADC characteristics*. Added footnote(5) and (6) in *Table 77: ADC characteristics* Updated THD values and added 4 more rows ENOB, SINAD, SNR, THD in *Table 78: ADC accuracy* Updated “SDA data hold time” and “SDA and SCL rise time” values and added “Pulse width of spikes that are suppressed by the analog filter” row in *Table 68: I^2C characteristics* Updated direct channels VDDA range in *Table 79: R_{AIN} max for f_{ADC} = 16 MHz* Moved *Table 82: Temperature sensor calibration values* and moved inside *Section 6.3.23: Temperature sensor characteristics* Updated I_{DD} (WU from Standby) unit in *Table 31: Typical and maximum current consumptions in Standby mode*. Updated *Table 67: LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data* Updated *Chapter 8: Part numbering* (title).

Table 75. Document revision history (continued)

Date	Revision	Changes
20-Aug-2015	11	Updated *Table 17: Embedded internal reference voltage* temperature coefficient at 100ppm/°C and table footnote 3: “guaranteed by design” changed by “guaranteed by characterization results”. Updated *Table 64: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C.
10-Mar-2016	12	Updated cover page putting eight SPIs in the peripheral communication interface list. Updated *Table 2: Ultra-low-power STM32L151xC and STM32L152xC device features and peripheral counts* SPI and I2S lines. Updated *Table 40: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated thermal resistance for UFQFPN48 to value of 33 °C/W. Updated *Table 11: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 5: Functionalities depending on the working mode (from Run/active down to standby)* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*.