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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

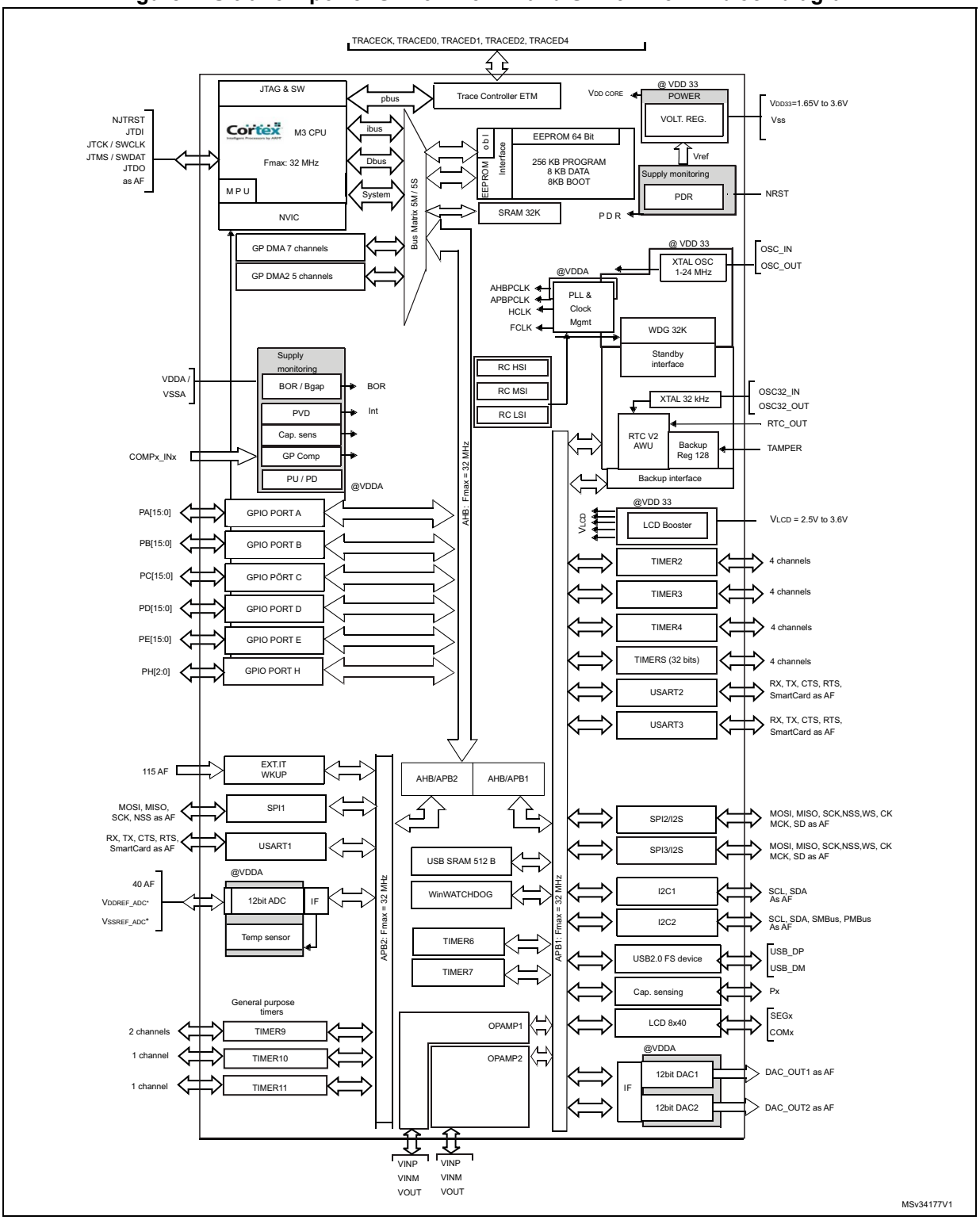
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rct6tr

List of tables

3 Functional overview

Figure 1. Ultra-low-power STM32L151xC and STM32L152xC block diagram



3.7 Memories

The STM32L151xC and STM32L152xC devices have the following features:

- 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 256 Kbytes of embedded Flash program memory
  - 8 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

  The user area of the Flash memory can be protected against Dbus read access by PCROP feature (see RM0038 for details).

3.8 DMA (direct memory access)

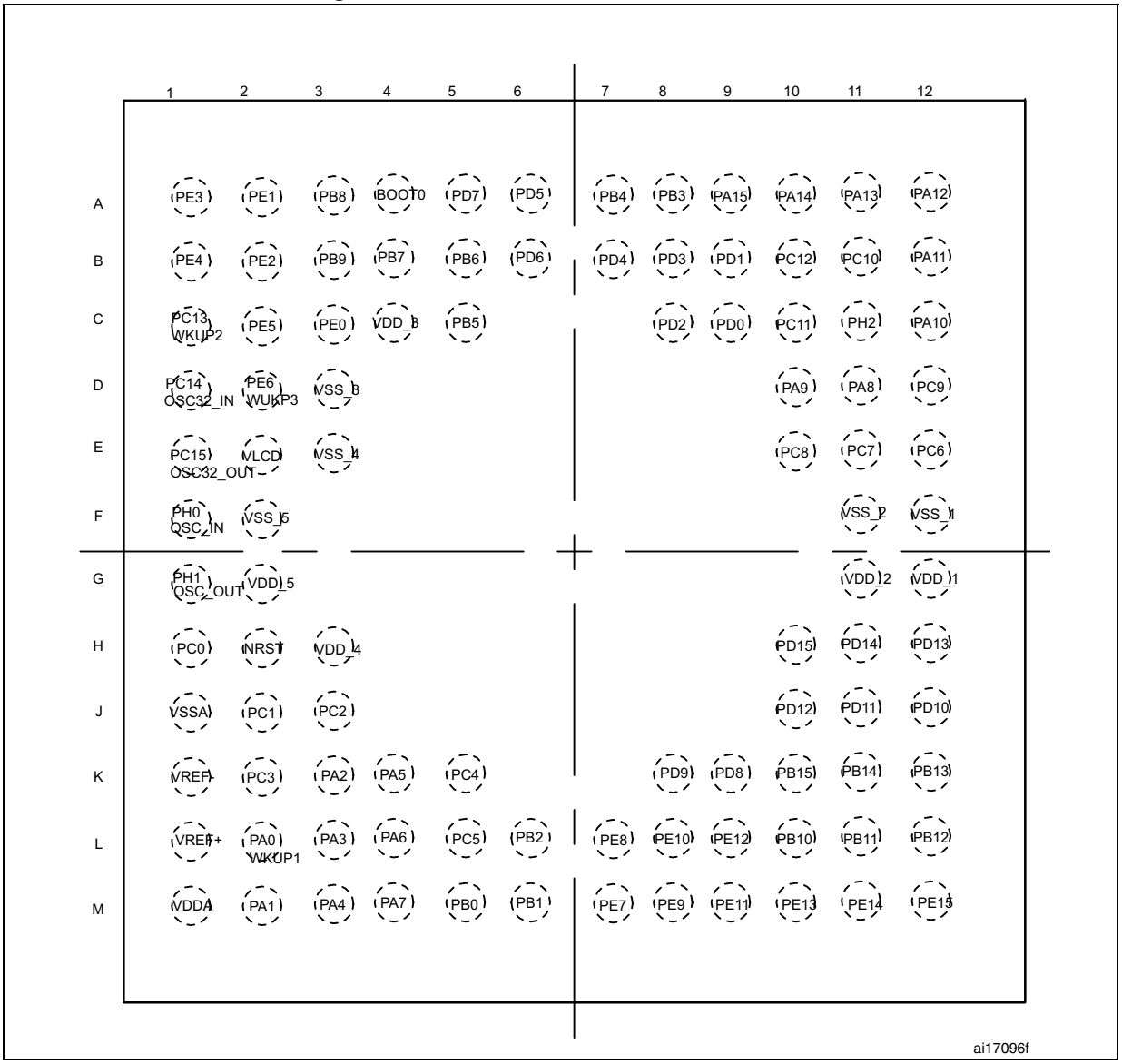
The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

4 Pin descriptions

Figure 3. STM32L15xVC UFBGA100 ballout



1. This figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151xC and STM32L152xC pin definitions

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
B2	1	-	-	-	PE2	I/O	FT	PE2	TIM3_ETR/LCD_SEG38 /TRACECLK	-
A1	2	-	-	-	PE3	I/O	FT	PE3	TIM3_CH1/LCD_SEG39 /TRACED0	-
B1	3	-	-	-	PE4	I/O	FT	PE4	TIM3_CH2/TRACED1	-
C2	4	-	-	-	PE5	I/O	FT	PE5	TIM9_CH1/TRACED2	-
D2	5	-	-	-	PE6-WKUP3	I/O	FT	PE6	TIM9_CH2/ TRACED3	WKUP3/ RTC_TAMP3
E2	6	1	C7	1	V_{LCD}(3)	S	-	V_{LCD}	-	-

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number								. .		. .		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7		AFIO11		AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
PC4	-	-	-	-	-	-	-	-		SEG22		TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-		SEG23		TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-		SEG24		TIMx_IC3	EVENT OUT
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-		SEG25		TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-		SEG26		TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-		SEG27		TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX		COM4/ SEG28/ SEG40		TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX		COM5/ SEG29 /SEG41		TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK		COM6/ SEG30/ SEG42		TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-		-		TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-		-		TIMx_IC3	EVENT OUT
PC15 OSC32_ OUT	-	-	-	-	-	-	-	-		-		TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-		-		TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-		-		TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-		COM7/ SEG31/ SEG43		TIMx_IC3	EVENT OUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number												
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
PE8	-	-	-	-	-	-	-	-		-		TIMx_IC1	EVENT OUT
PE9	-	TIM2_CH1_ETR	TIM5_ETR	-	-	-	-	-		-		TIMx_IC2	EVENT OUT
PE10	-	TIM2_CH2	-	-	-	-	-	-		-		TIMx_IC3	EVENT OUT
PE11	-	TIM2_CH3	-	-	-	-	-	-		-		TIMx_IC4	EVENT OUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-		-		TIMx_IC1	EVENT OUT
PE13	-	-	-	-	-	SPI1_SCK	-	-		-		TIMx_IC2	EVENT OUT
PE14	-	-	-	-	-	SPI1_MISO	-	-		-		TIMx_IC3	EVENT OUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-		-		TIMx_IC4	EVENT OUT
PH0OSC _IN	-	-	-	-	-	-	-	-		-		-	-
PH1OSC_ OUT	-	-	-	-	-	-	-	-		-		-	-
PH2	-	-	-	-	-	-	-	-		-		-	-

5. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to the Dhrystone 2.1 code, unless otherwise specified. The current consumption values are derived from tests performed under ambient temperature T_A = 25 °C and V_{DD} supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 27: High-speed external user clock characteristics*.
- For maximum current consumption $V_{DD} = V_{DDA}$ = 3.6 V is applied to all supply pins.
- For typical current consumption $V_{DD} = V_{DDA}$ = 3.0 V is applied to all supply pins if not specified otherwise.

Low-speed external user clock generated from an external source

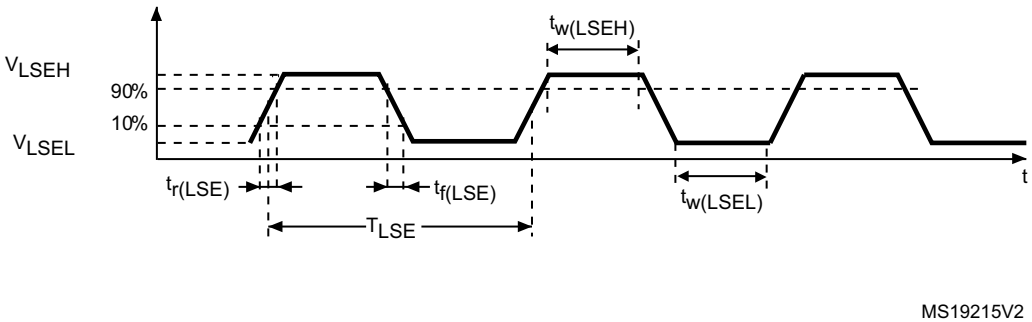
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under the conditions summarized in *Table 14*.

Table 28. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Table 33. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

Flash memory and data EEPROM

Table 36. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming/ erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	600	900	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 37. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

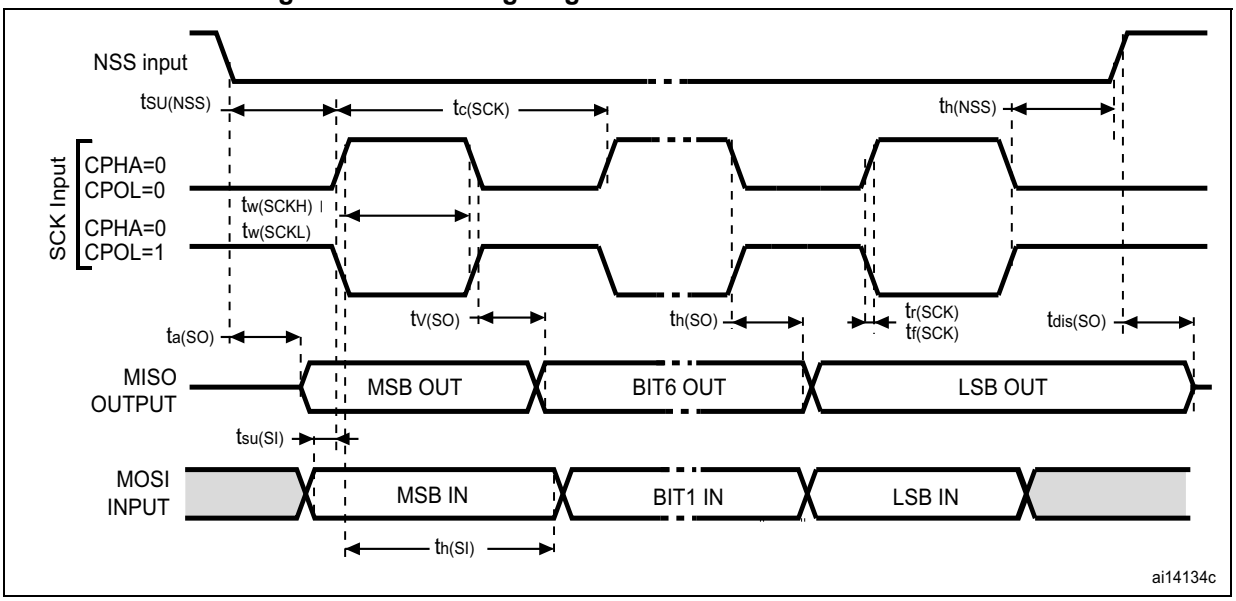
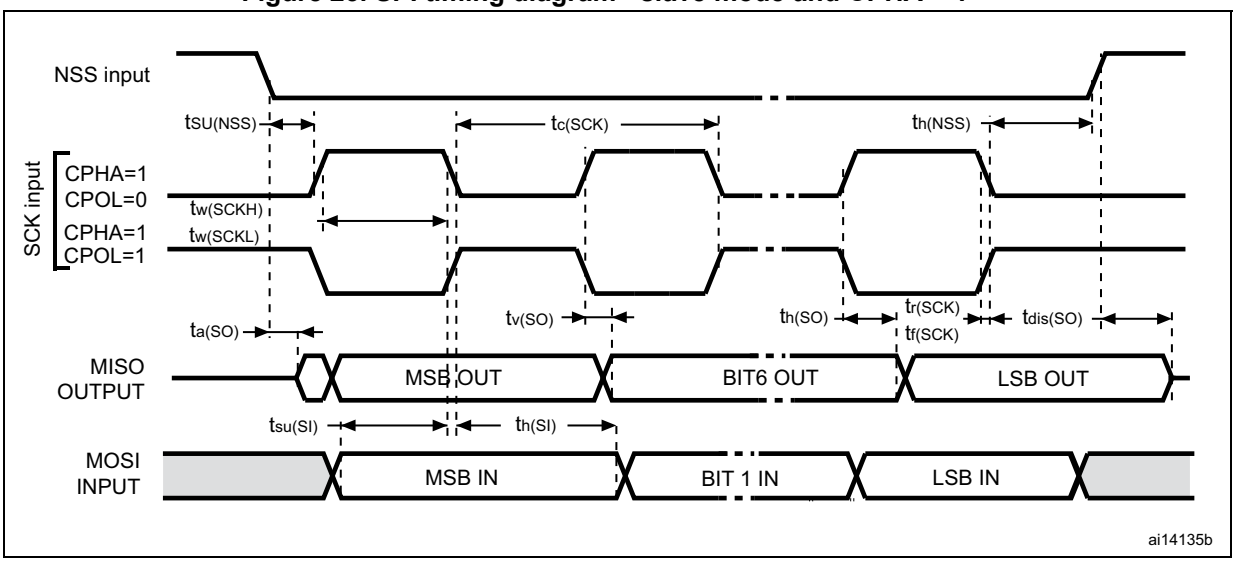


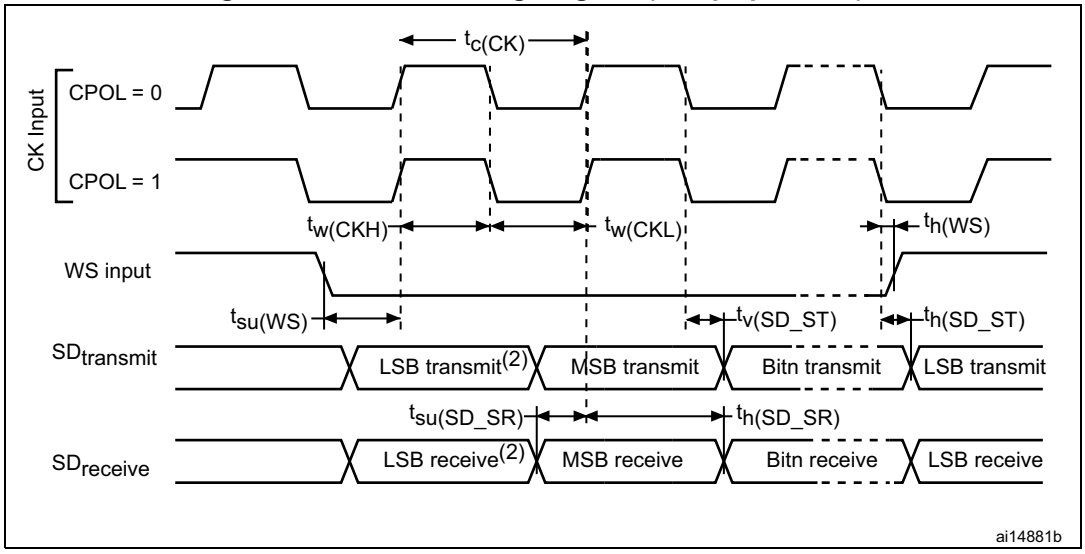
Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

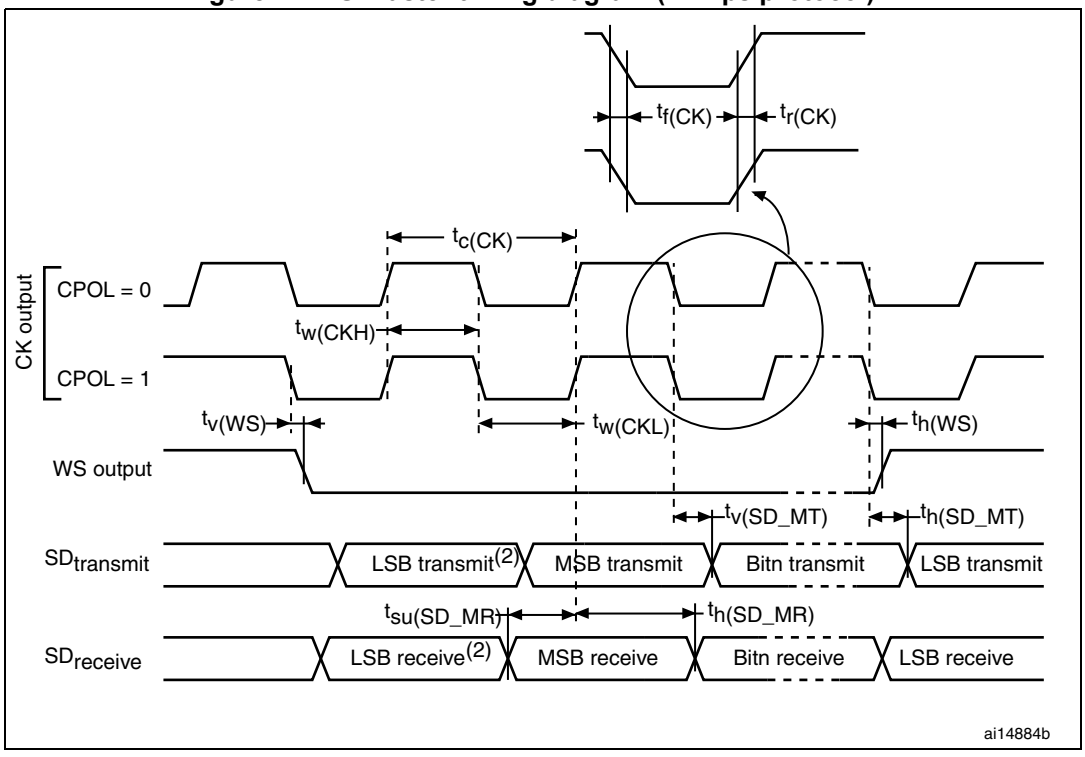
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 26. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



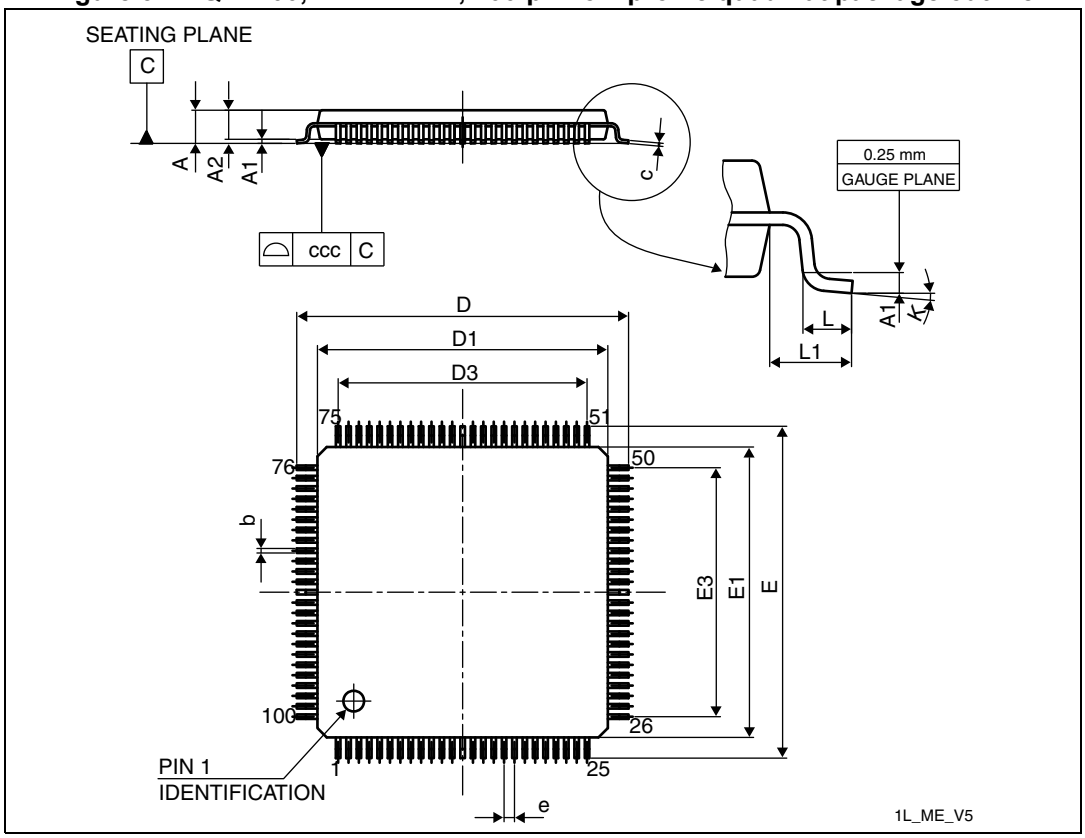
1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 32. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

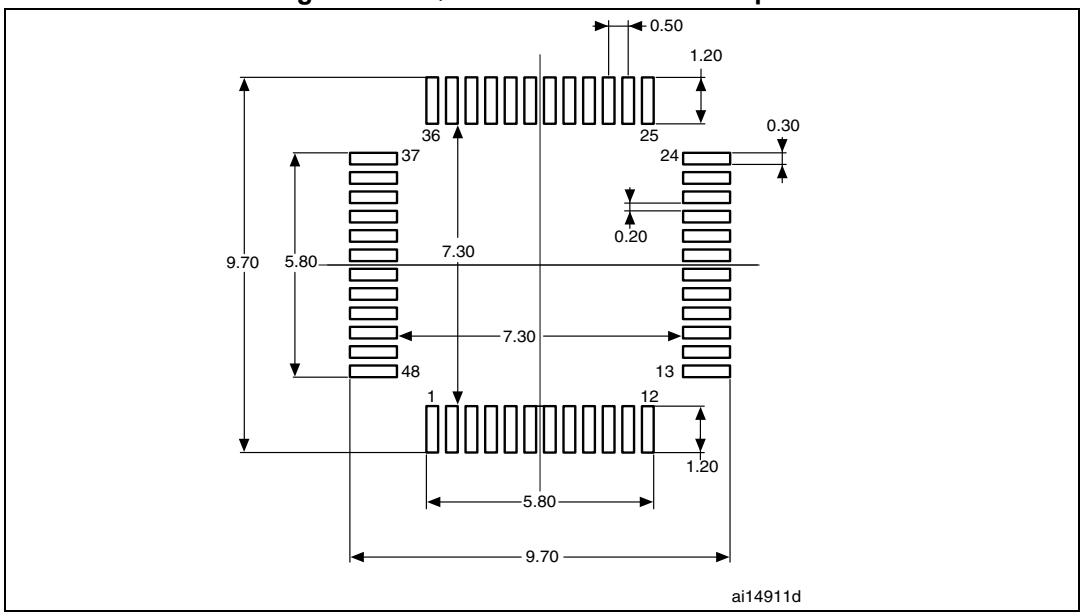
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 68. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP48 recommended footprint

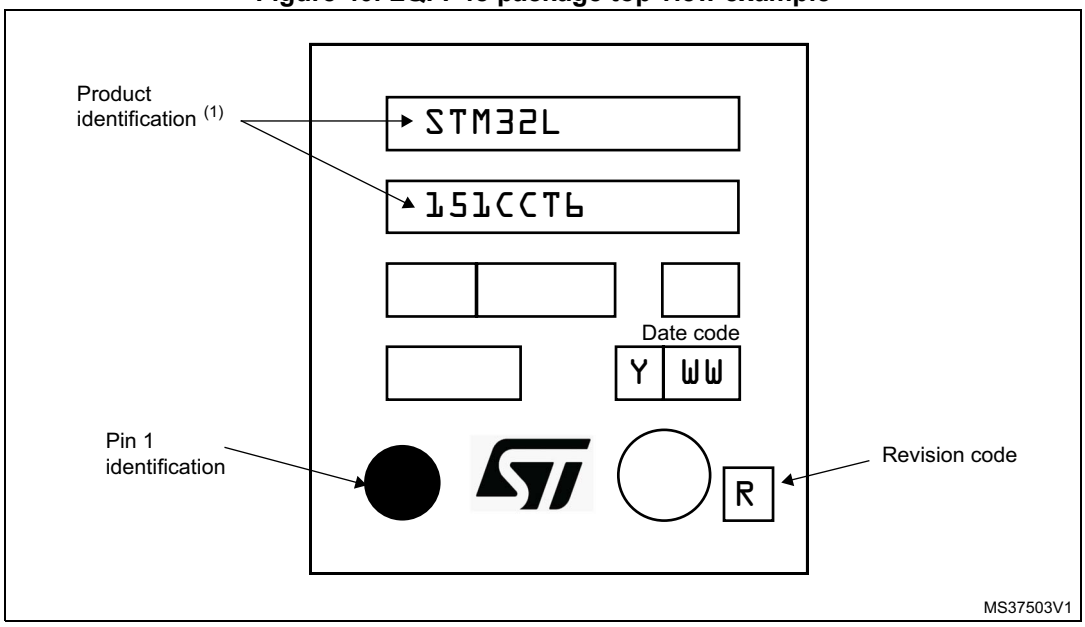


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

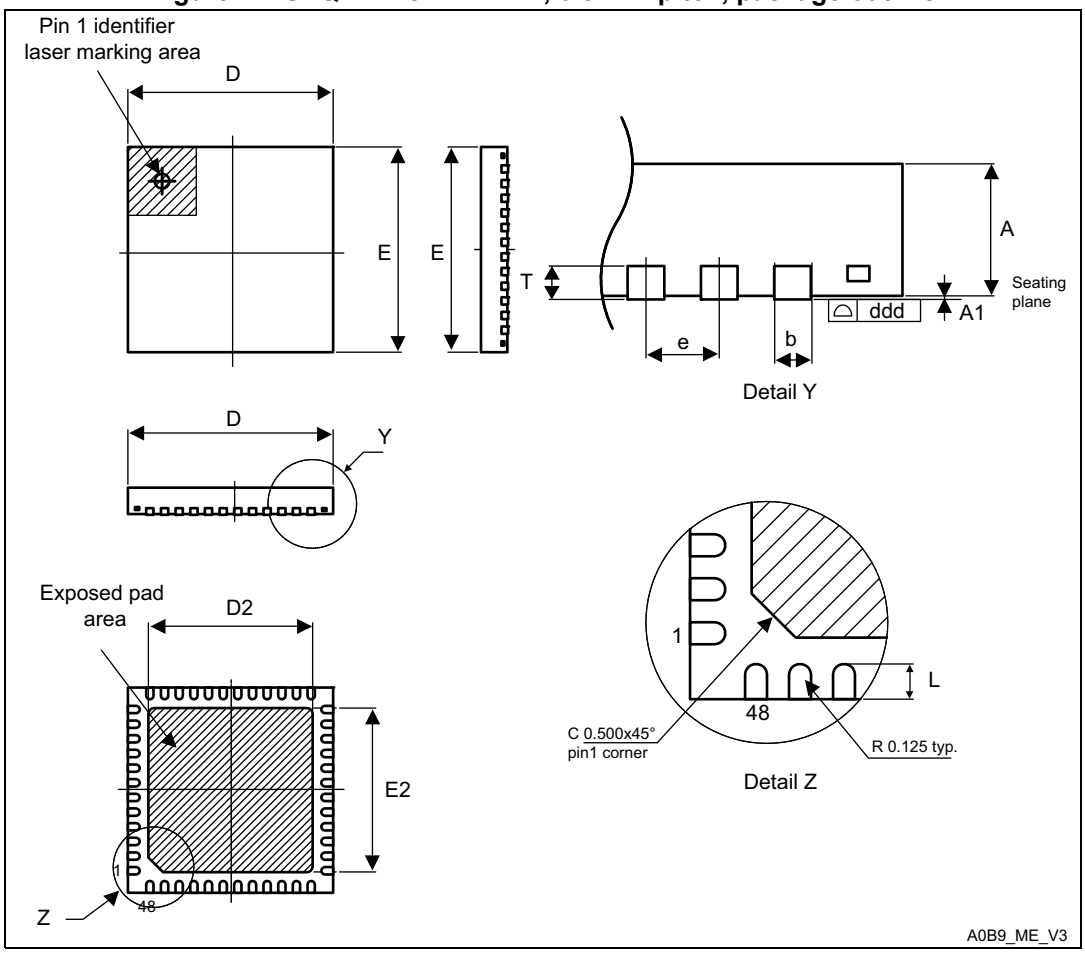
Figure 40. LQFP48 package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 75. Document revision history (continued)

Date	Revision	Changes
09-Dec-2013	6	Apply footnote 1 also to VDD= 1.8 to 2.0 V in *Table 2: Functionalities depending on the operating power supply range*. Updated I_{inj} pin in *Table 11: Current characteristics*. Added Input Voltage in *Table 13: General operating conditions*. Updated Input leakage current conditions in *Table 63: I/O static characteristics* Removed minimum value for $f_S$in *Table 77: ADC characteristics*. Removed Fi_{nput} for ENOB,SINAD,SNR,THD in *Table 78: ADC accuracy*. Added tolerance for TS_CAL1 and TS_CAL2 in *Table 82: Temperature sensor calibration values*.
13-Mar-2014	7	Updated *Section 3.7: Memories*, *Table 33: Peripheral current consumption* : updated Flash value, *Table 61: I/O current injection susceptibility*, *Table 63: I/O static characteristics*:added BOOT0 pin *Table 66: NRST pin characteristics*, *Chapter 2.2: Ultra-low-power device continuum*. removed figures “Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) and “Power supply and reference decoupling(V_{REF+} connected to V_{DDA}). Updated *Table 19: Current consumption in Run mode, code with data processing running from Flash* Updated *Section 6.3.1: General operating conditions*. Updated *Table 80: DAC characteristics* Added marking for LQFP48/UFQFPN48 packages Updated *Table 66: NRST pin characteristics* Updated *Table 63: I/O static characteristics*
16-May-2014	8	Updated I_{IO} in *Table 12: Current characteristics*. Updated conditions in *Table 44: Output voltage characteristics*. Removed note 4 in *Table 62: Temperature sensor characteristics* Updated the conditions in *Table 26: Low-power mode wakeup timings*. Removed ambiguity of “ambient temperature” in the electrical characteristics description.
13-Oct-2014	9	Updated *Section 3.17: Communication interfaces* putting I2S characteristics inside. Updated DMIPS features in cover page and *Section 2: Description*. Updated max temperature at 105°C instead of 85°C in the whole datasheet. Updated current consumption in *Table 20: Current consumption in Sleep mode*. Updated *Table 25: Peripheral current consumption* with new measured current values. Updated *Table 58: Maximum source impedance RAIN max* adding note 2.
06-Mar-2015	10	Updated *Section 7: Package information* with new package device marking. Updated *Figure 9: Memory map*.