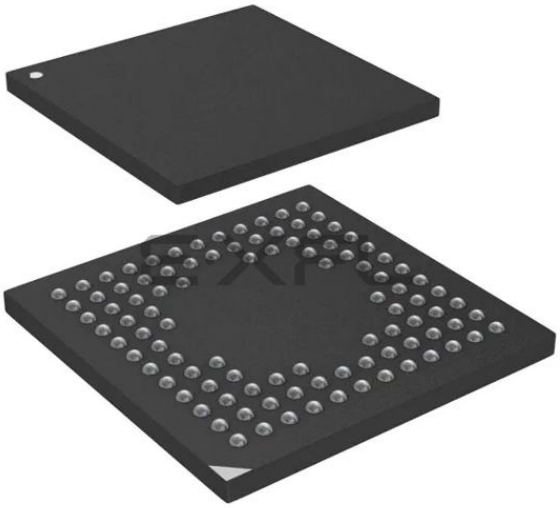

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152vch6d

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xC and STM32L152xC ultra-low-power ARM® Cortex®-M3 based microcontroller product line with a Flash memory of 256 Kbytes.

The ultra-low-power STM32L151xC and STM32L152xC family includes devices in 6 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xC and STM32L152xC microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xC and STM32L152xC datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note “Getting started with STM32L1xxxx hardware development” (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the ARM® Cortex®-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

3.1 Low-power modes

The ultra-low-power STM32L151xC and STM32L152xC devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V - 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep** mode

  This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}=V_{DDA} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD}=V_{DDA} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
ADC	Y	Y	--	--	--	--	--	--
DAC	Y	Y	Y	Y	Y	--	--	--
Tempsensor	Y	Y	Y	Y	Y	--	--	--
OP amp	Y	Y	Y	Y	Y	--	--	--
Comparators	Y	Y	Y	Y	Y	Y	--	--
16-bit and 32-bit Timers	Y	Y	Y	Y	--	--	--	--
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	--	--	--	--
Touch sensing	Y	Y	--	--	--	--	--	--
Systic Timer	Y	Y	Y	Y		--	--	--
GPIOs	Y	Y	Y	Y	Y	Y	--	3 pins
Wakeup time to Run mode	0 µs	0.4 µs	3 µs	46 µs	< 8 µs		58 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 185 µA/MHz (from Flash)	Down to 34.5 µA/MHz (from Flash)	Down to 8.6 µA	Down to 4.4 µA	0.43 µA (no RTC) V_{DD}=1.8V		0.29 µA (no RTC) V_{DD}=1.8V	
					1.15 µA (with RTC) V_{DD}=1.8V		0.9 µA (with RTC) V_{DD}=1.8V	
					0.44 µA (no RTC) V_{DD}=3.0V		0.29 µA (no RTC) V_{DD}=3.0V	
					1.4 µA (with RTC) V_{DD}=3.0V		1.15 µA (with RTC) V_{DD}=3.0V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.16.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.16.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17 Communication interfaces

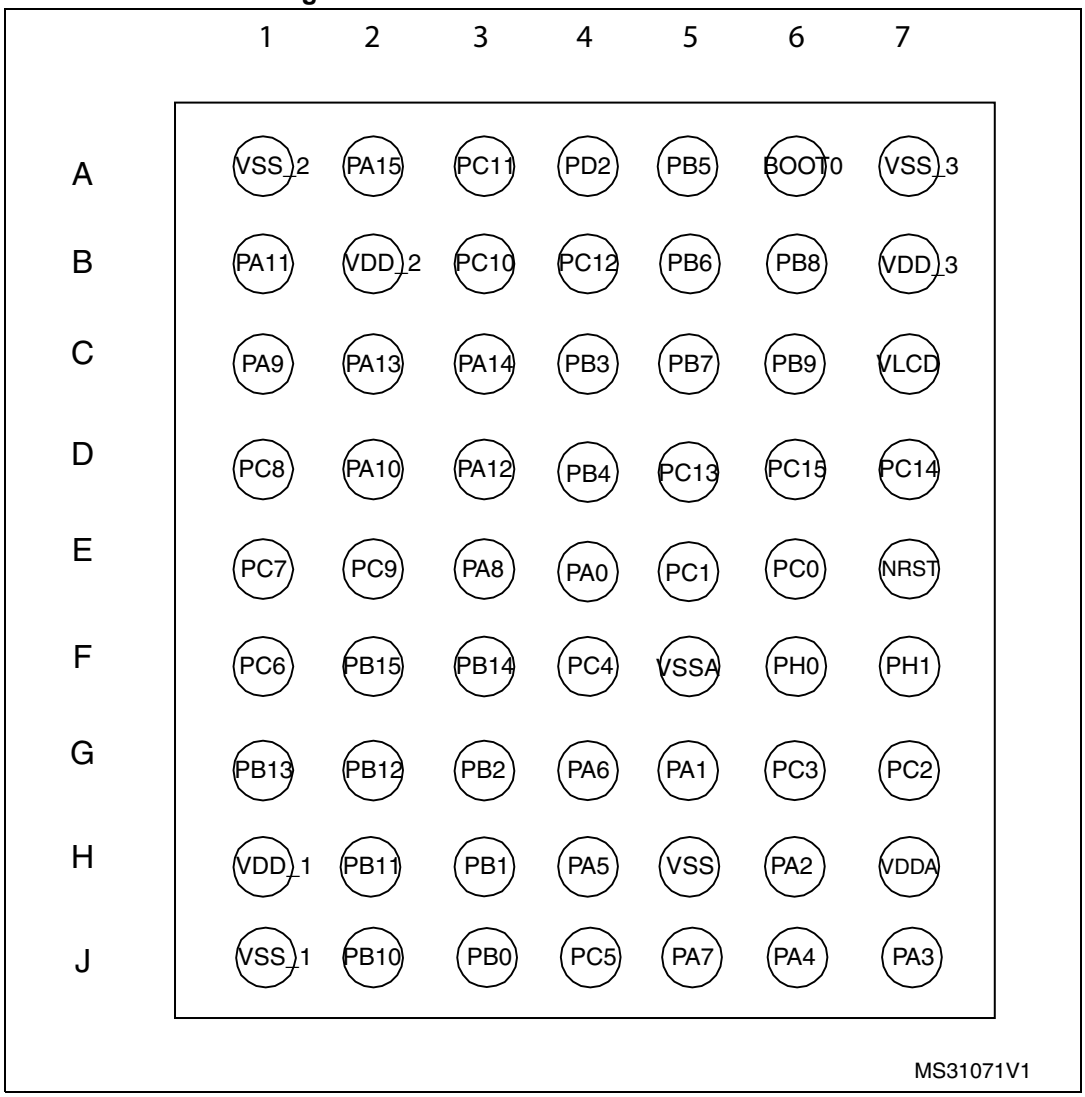
3.17.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Figure 6. STM32L15xUC WLCSP63 ballout



1. This figure shows the package top view.

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
C1	7	2	D5	2	PC13-WKUP2	I/O	FT	PC13	-	WKUP2/ RTC_TAMP1/ RTC_TS/RTC_OUT
D1	8	3	D7	3	PC14-OSC32_IN(4)	I/O	TC	PC14	-	OSC32_IN
E1	9	4	D6	4	PC15-OSC32_OUT	I/O	TC	PC15	-	OSC32_OUT
F2	10	-	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
G2	11	-	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
F1	12	5	F6	5	PH0-OSC_IN(5)	I/O	TC	PH0	-	OSC_IN
G1	13	6	F7	6	PH1-OSC_OUT(5)	I/O	TC	PH1	-	OSC_OUT
H2	14	7	E7	7	NRST	I/O	RST	NRST	-	-
H1	15	8	E6	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
J2	16	9	E5	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
J3	17	10	G7	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
K2	18	11	G6	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP
J1	19	12	F5	8	V_{SSA}	S	-	V_{SSA}	-	-
K1	20	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
L1	21	-	-	-	V_{REF+}	S	-	V_{REF+}	-	-
M1	22	13	H7	9	V_{DDA}	S	-	V_{DDA}	-	-
L2	23	14	E4	10	PA0-WKUP1	I/O	FT	PA0	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/ RTC_TAMP2/ ADC_IN0/ COMP1_INP

Table 9. STM32L151xC and STM32L152xC pin definitions (continued)

Pins					Pin name	Pin type(1)	I / O Structure	Main function(2) (after reset)	Pin functions	
UFBGA100	LQFP100	LQFP64	WLCSP63	LQFP48 or UFQFPN48					Alternate functions	Additional functions
M2	24	15	G5	11	PA1	I/O	FT	PA1	TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0	ADC_IN1/ COMP1_INP/ OPAMP1_VINP
K3	25	16	H6	12	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/USART2_TX /LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
L3	26	17	J7	13	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/USART2_RX /LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
E3	27	18	-	-	V_{SS_4}	S	-	V_{SS_4}	-	-
H3	28	19	-	-	V_{DD_4}	S	-	V_{DD_4}	-	-
M3	29	20	J6	14	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
K4	30	21	H4	15	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
L4	31	22	G4	16	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/ SPI1_MISO/LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
M4	32	23	J5	17	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM
K5	33	24	F4	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
L5	34	25	J4	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
M5	35	26	J3	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VLCDRAIL3/ VREF_OUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number								. .		. .		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7		AFIO11		AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
PC4	-	-	-	-	-	-	-	-		SEG22		TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-		SEG23		TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-		SEG24		TIMx_IC3	EVENT OUT
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-		SEG25		TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-		SEG26		TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-		SEG27		TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX		COM4/ SEG28/ SEG40		TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX		COM5/ SEG29 /SEG41		TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK		COM6/ SEG30/ SEG42		TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-		-		TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-		-		TIMx_IC3	EVENT OUT
PC15 OSC32_ OUT	-	-	-	-	-	-	-	-		-		TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-		-		TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-		-		TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-		COM7/ SEG31/ SEG43		TIMx_IC3	EVENT OUT

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	V
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option “D” in Ordering information scheme for more details.

Table 20. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	50	130	µA
				2 MHz	78.5	195	
				4 MHz	140	310	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	165	310	
				8 MHz	310	440	
				16 MHz	590	830	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	350	550	
				16 MHz	680	990	
				32 MHz	1600	2100	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	640	890	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2200	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	60	
		MSI clock, 524 kHz		524 kHz	33	99	
		MSI clock, 4.2 MHz		4.2 MHz	145	210	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	60.5	130	
				2 MHz	89.5	190	
				4 MHz	150	320	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	180	320	
				8 MHz	320	460	
				16 MHz	605	840	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	380	540	
				16 MHz	695	1000	
				32 MHz	1600	2100	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	650	910	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2200	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	30	90	
		MSI clock, 524 kHz		524 kHz	44	96	
		MSI clock, 4.2 MHz		4.2 MHz	155	220	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.8	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.435	1	
			T_A = 55°C	0.99	3	
			T_A= 85°C	2.4	9	
			T_A = 105°C	5.5	22(5)	
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	MSI = 4.2 MHz	T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(6)		1.45	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
3. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Guaranteed by test in production.
6. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining part of the wakeup period, the current corresponds the Run mode current.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 44*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (3)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Guaranteed by test in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

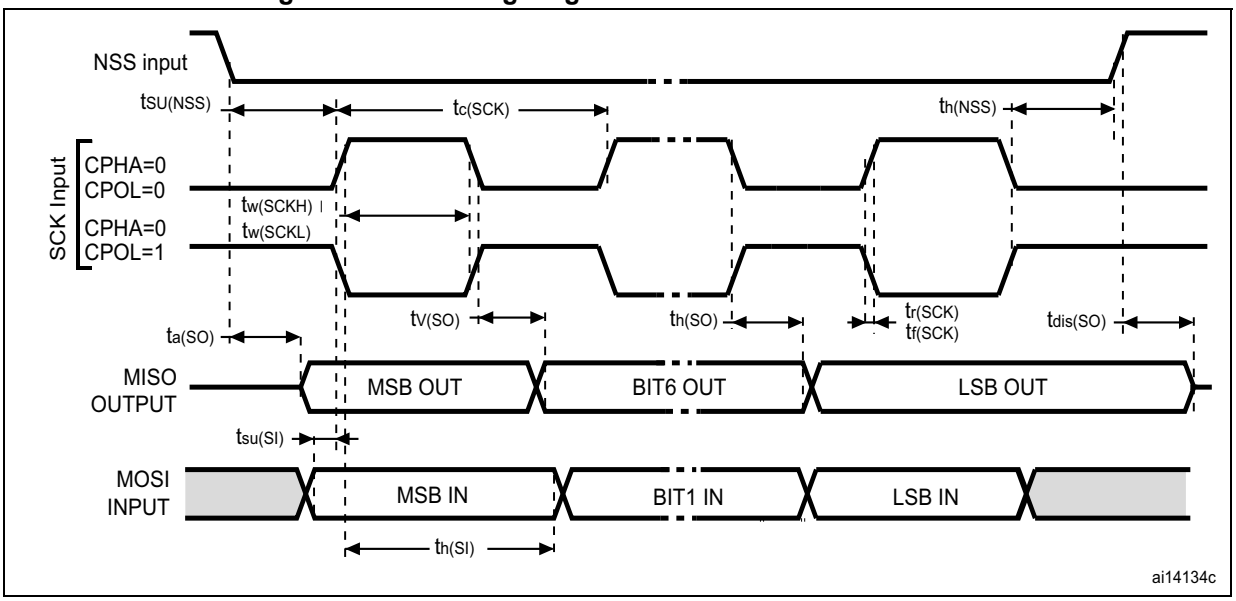
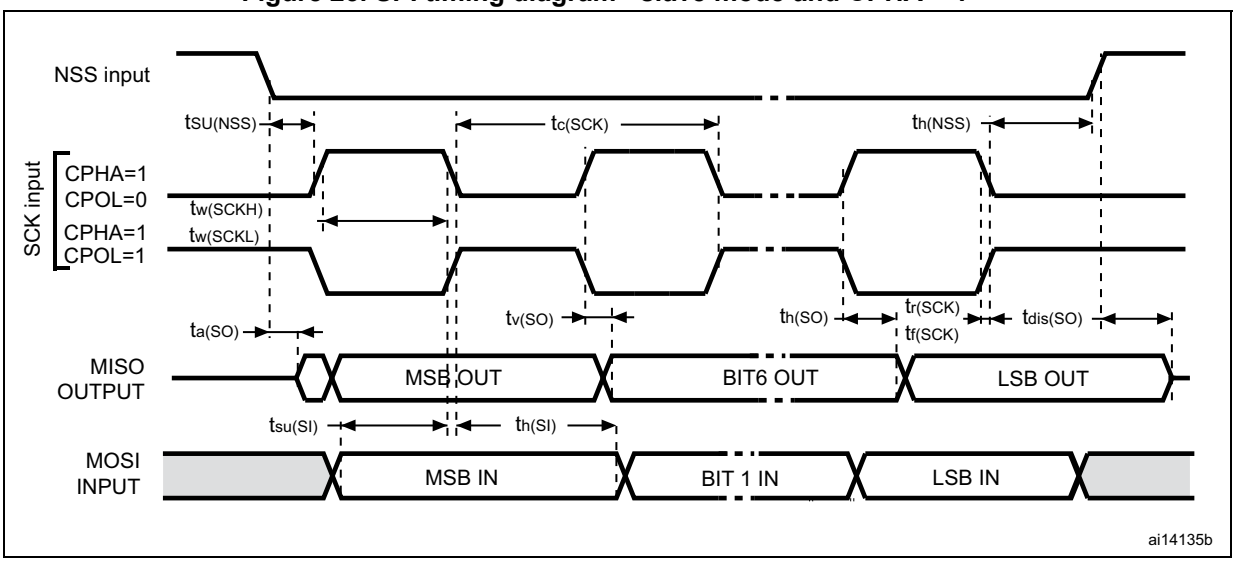


Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



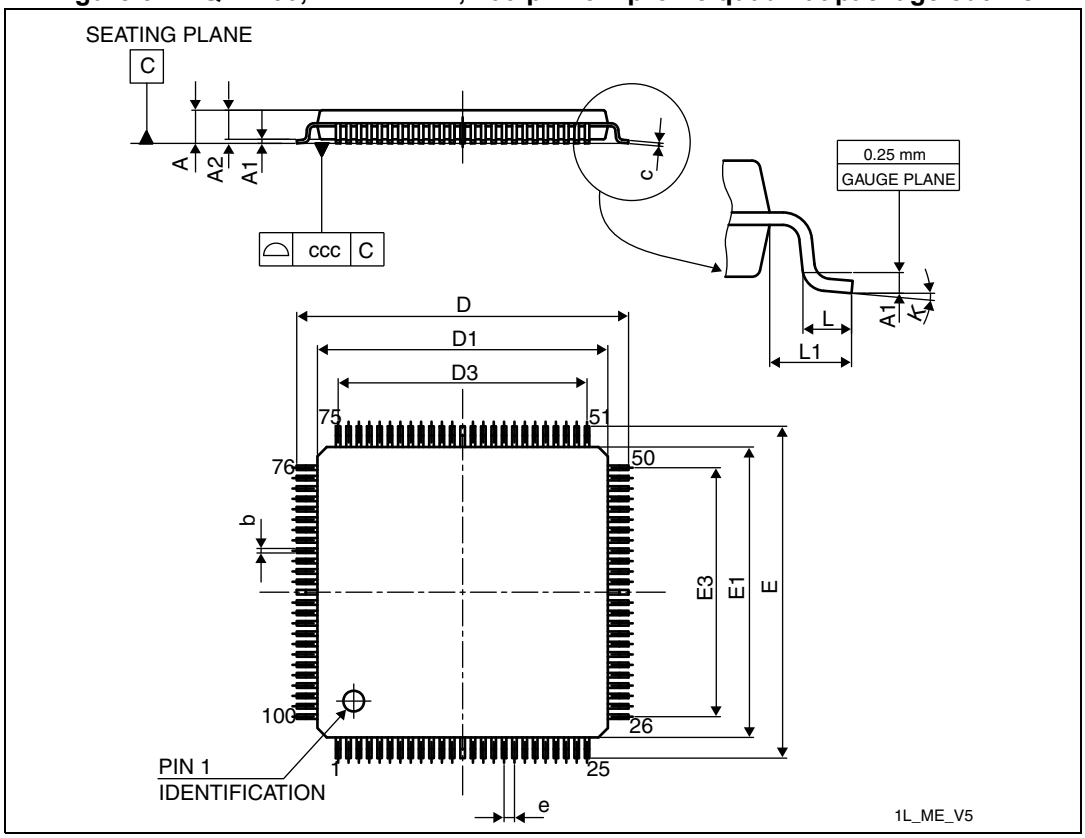
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 32. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



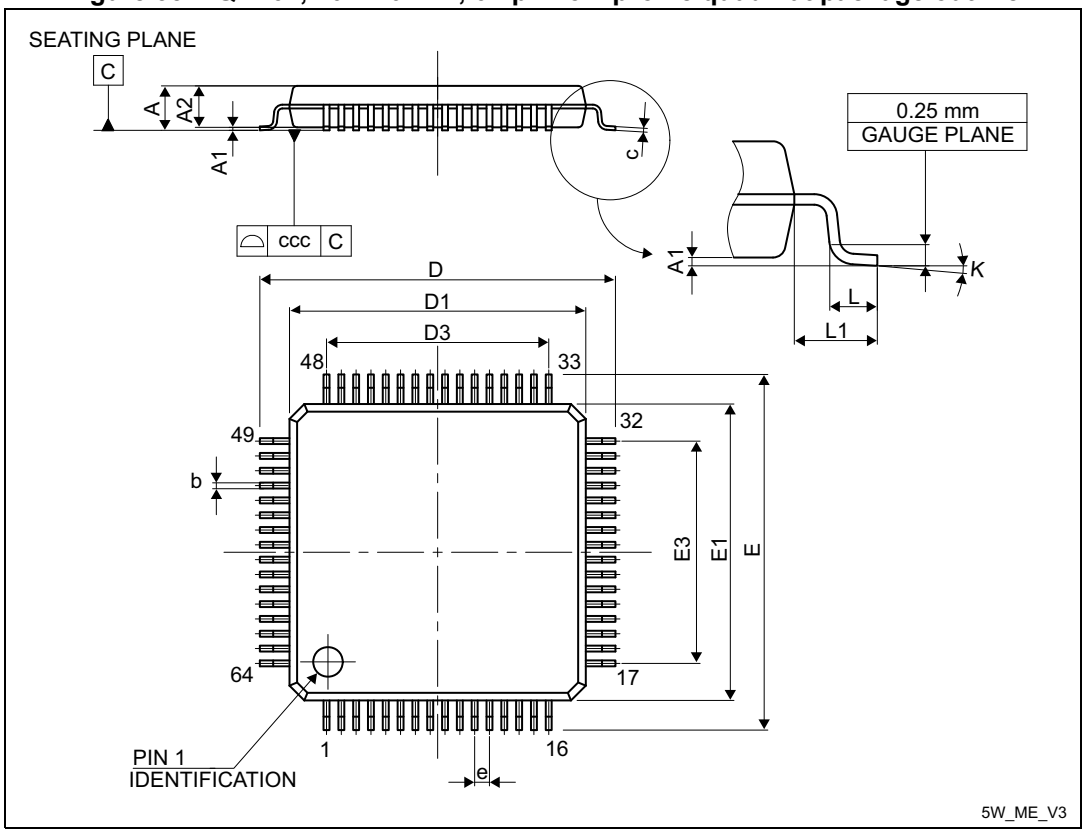
1. Drawing is not to scale.

Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

7.2 LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 35. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data

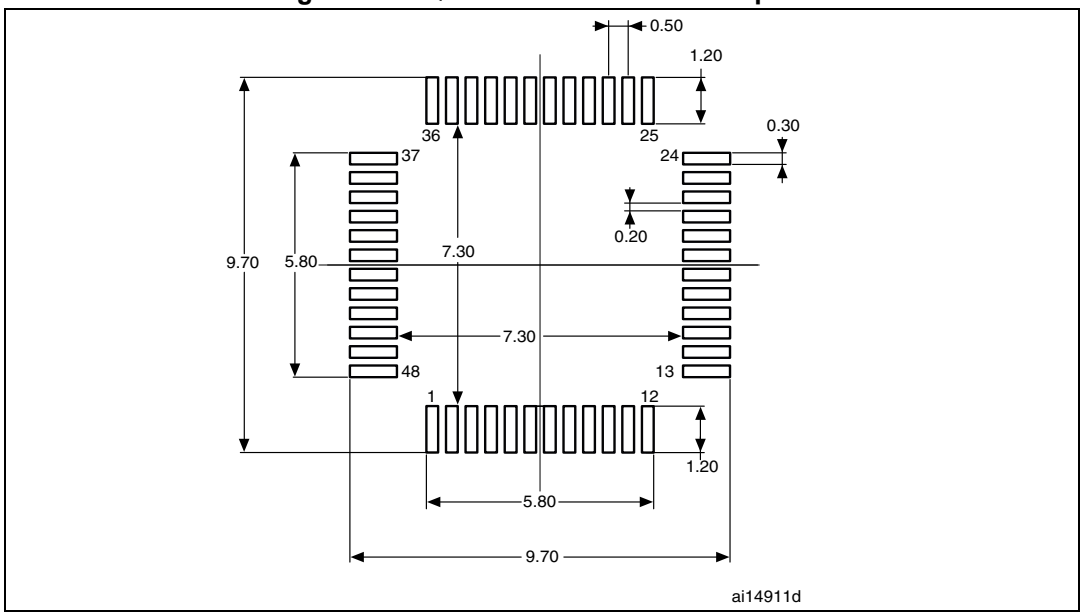
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 68. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

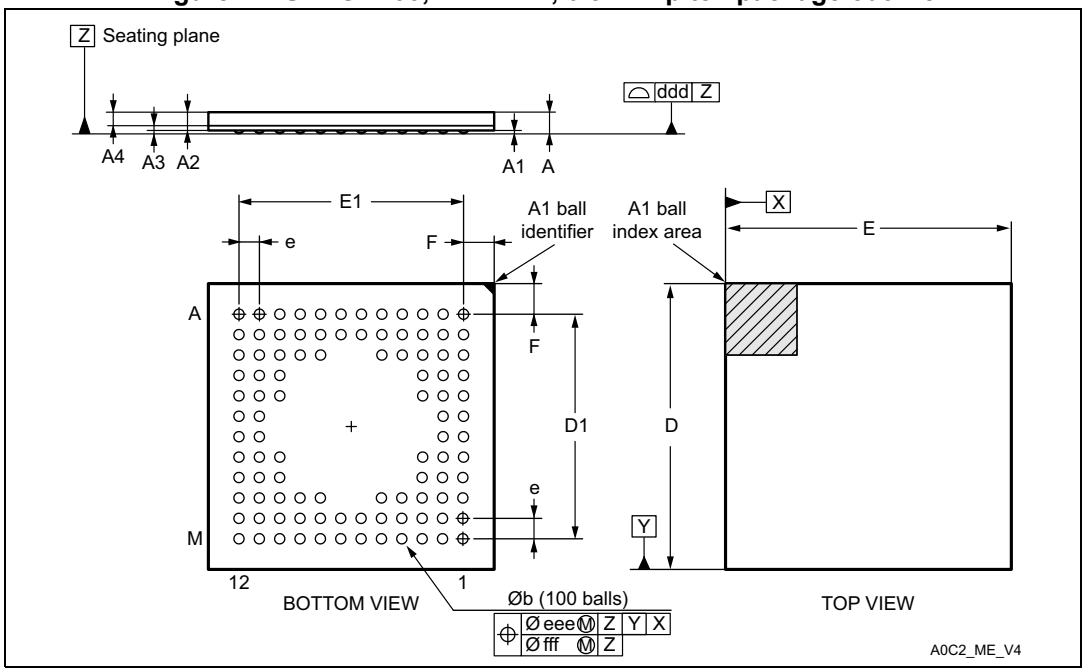
Figure 39. LQFP48 recommended footprint



1. Dimensions are in millimeters.

7.5 UFBGA100, 7 x 7 mm, 100-ball ultra thin, fine pitch ball grid array package information

Figure 44. UFBGA100, 7 x 7 mm, 0.5 mm pitch package outline



1. Drawing is not to scale.

Table 70. UFBGA100, 7 x 7 mm, 0.5 mm pitch package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 73. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm	59	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP63 - 0.400 mm pitch	49	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	