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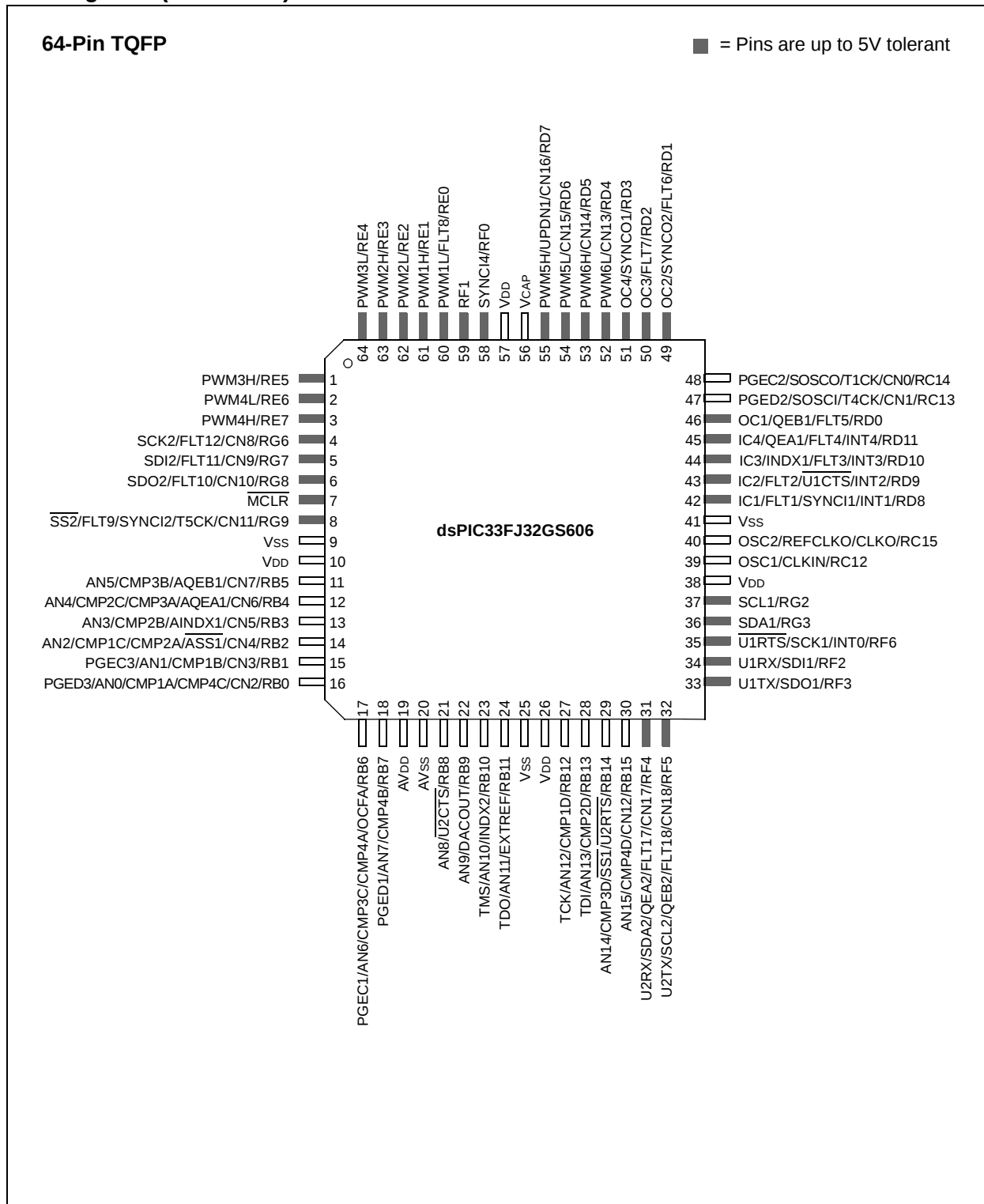
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, QEI, POR, PWM, WDT
Number of I/O	58
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gs606t-50i-mr

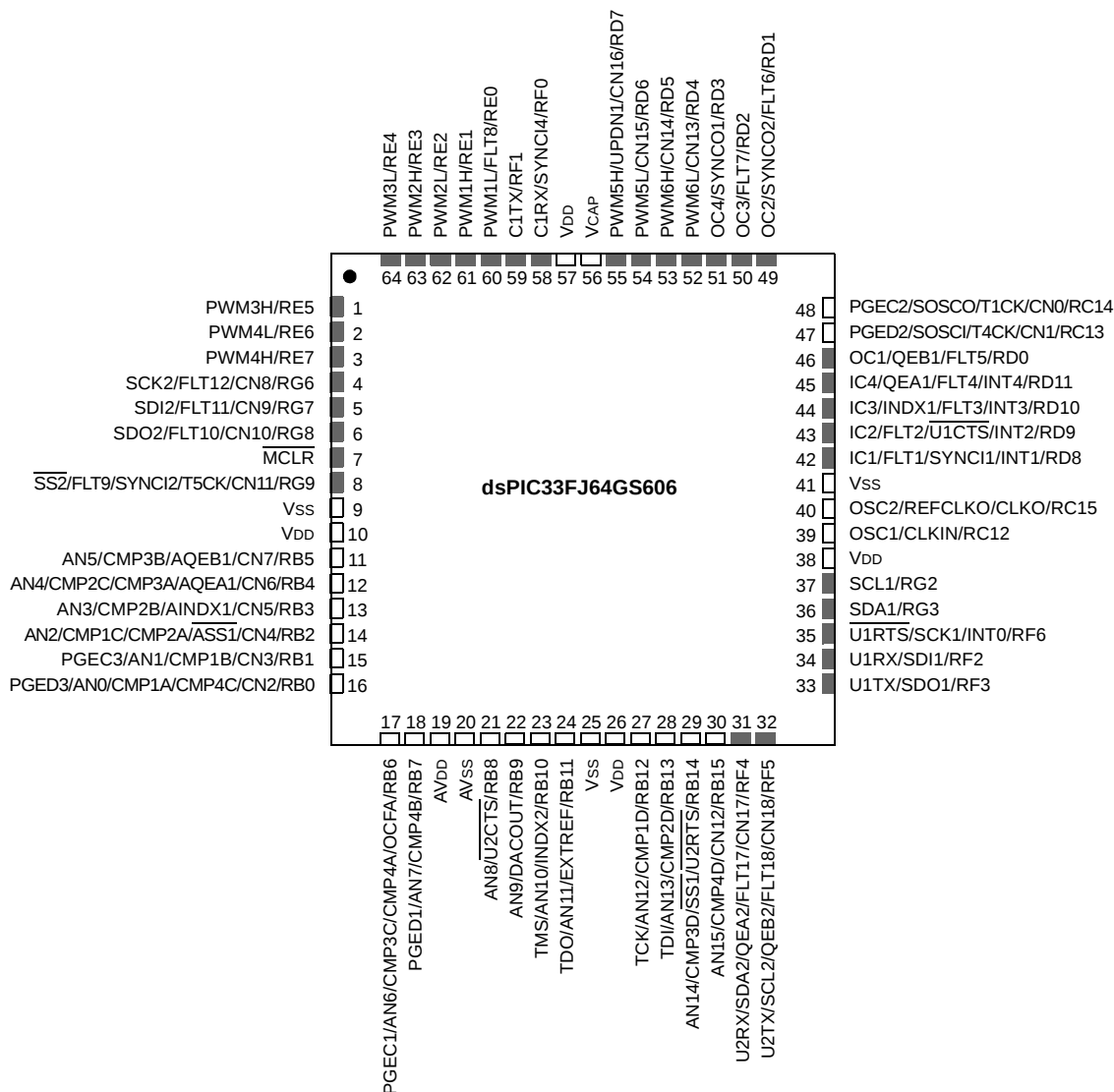
Pin Diagrams (Continued)



Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

Pin Diagrams (Continued)

80-Pin TQFP

■ = Pins are up to 5V tolerant

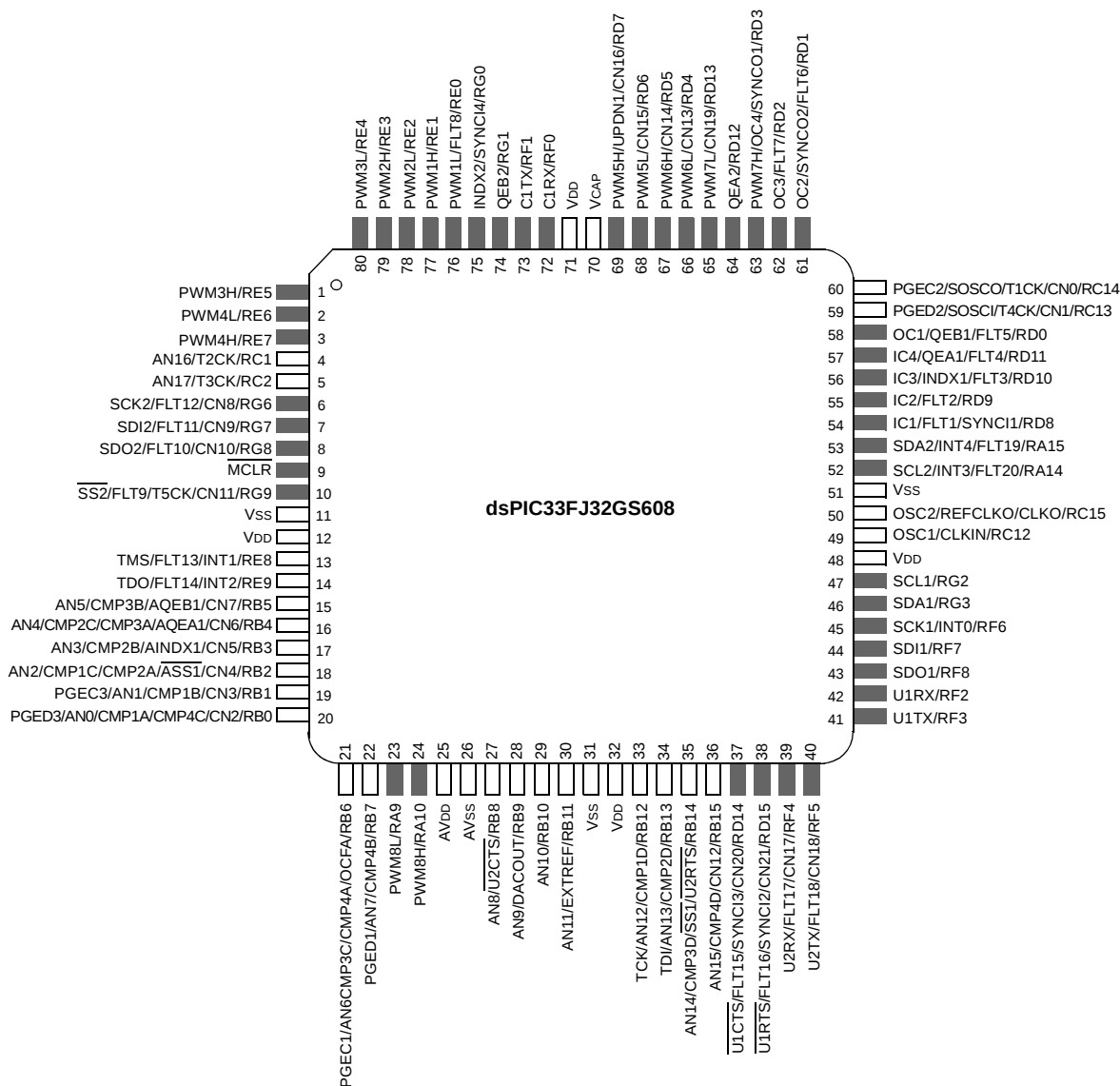
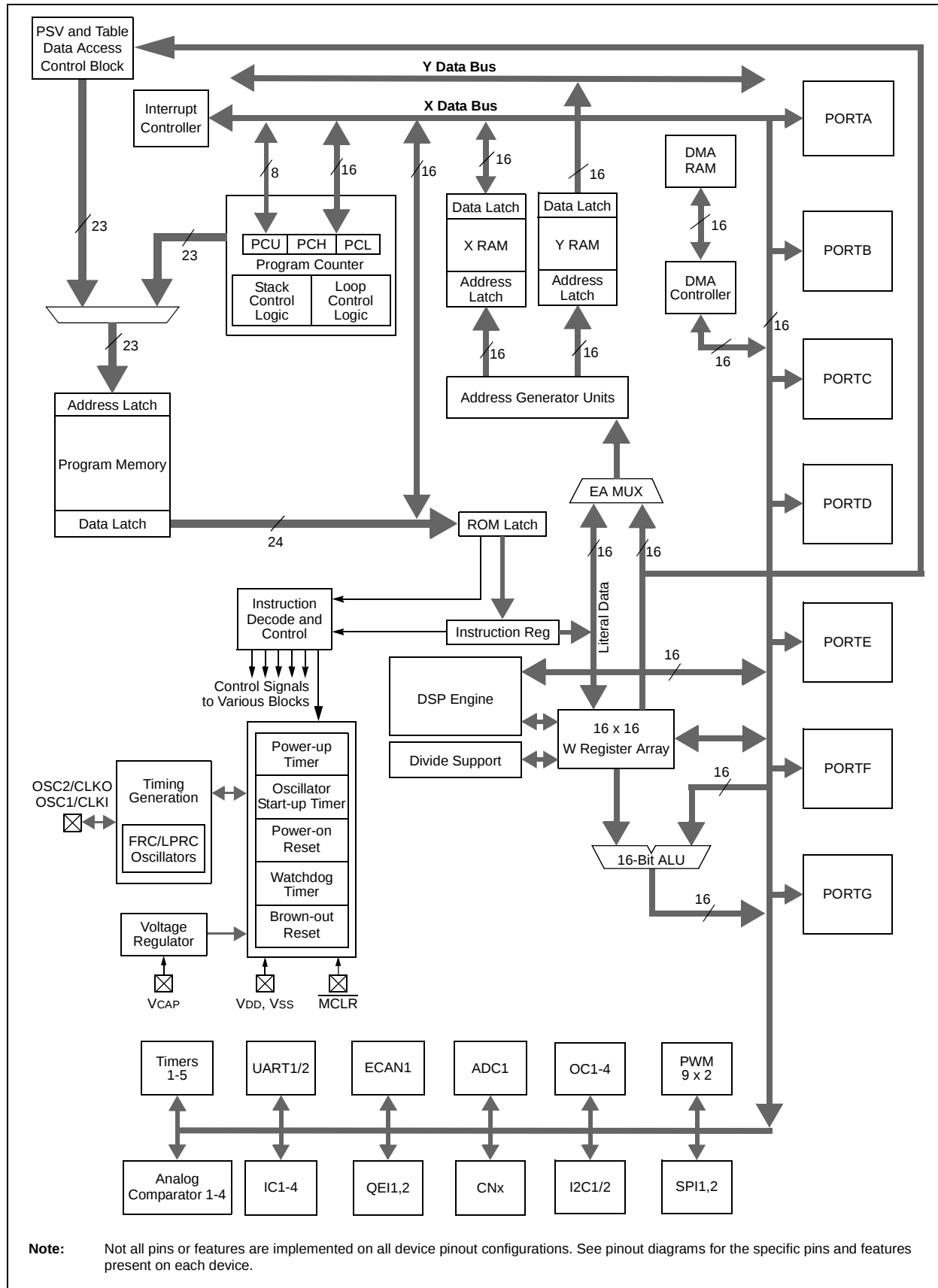


FIGURE 1-1: DEVICE BLOCK DIAGRAM



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

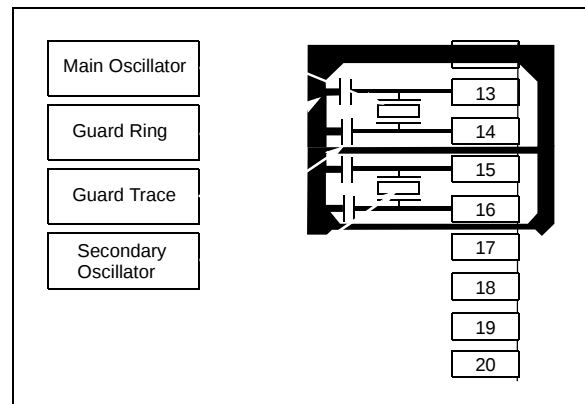
- “Using MPLAB® ICD 3” (poster) (DS51765)
- “MPLAB® ICD 3 Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Debugger User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™” (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 “Oscillator Configuration”** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



3.6.3.2 Data Space Write Saturation

In addition to adder/subtractor saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly:

- For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF.
- For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000.

The Most Significant bit of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

3.6.4 BARREL SHIFTER

The barrel shifter can perform up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either of the two DSP accumulators or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 and 31 for right shifts, and between bit positions 0 and 16 for left shifts.

TABLE 4-53: PORTF REGISTER MAP FOR dsPIC33FJ32GS406/606 AND dsPIC33FJ64GS406/606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	02E8	—	—	—	—	—	—	—	—	—	TRISF<6:0>							007F
PORTF	02EA	—	—	—	—	—	—	—	—	—	RF<6:0>							xxxx
LATF	02EC	—	—	—	—	—	—	—	—	—	LATF<6:0>							0000
ODCF	02EE	—	—	—	—	—	—	—	—	—	ODCF6	—	—	ODCF<3:1>			—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTG REGISTER MAP FOR dsPIC33FJ32GS610 AND dsPIC33FJ64GS610 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	02F0	TRISG<15:12>				—	—	TRISG<9:6>				—	—	TRISG<3:0>				F3CF
PORTG	02F2	RG<15:12>				—	—	RG<9:6>				—	—	RG<3:0>				xxxx
LATG	02F4	LATG<15:12>				—	—	LATG<9:6>				—	—	LATG<3:0>				0000
ODCG	02F6	ODCG<15:12>				—	—	ODCG<9:6>				—	—	ODCG<3:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTG REGISTER MAP FOR dsPIC33FJ32GS608 AND dsPIC33FJ64GS608 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	02F0	—	—	—	—	—	—	TRISG<9:6>				—	—	TRISG<3:0>				03CF
PORTG	02F2	—	—	—	—	—	—	RG<9:6>				—	—	RG<3:0>				xxxx
LATG	02F4	—	—	—	—	—	—	LATG<9:6>				—	—	LATG<3:0>				0000
ODCG	02F6	—	—	—	—	—	—	ODCG<9:6>				—	—	ODCG<3:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-56: PORTG REGISTER MAP FOR dsPIC33FJ32GS406/606 AND dsPIC33FJ64GS406/606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	02F0	—	—	—	—	—	—	TRISG<9:6>				—	—	TRISG<3:2>		—	—	03CC
PORTG	02F2	—	—	—	—	—	—	RG<9:6>				—	—	RG<3:2>		—	—	xxxx
LATG	02F4	—	—	—	—	—	—	LATG<9:6>				—	—	LATG<3:2>		—	—	0000
ODCG	02F6	—	—	—	—	—	—	ODCG<9:6>				—	—	ODCG<3:2>		—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.4 External Reset (EXTR)

The External Reset is generated by driving the $\overline{\text{MCLR}}$ pin low. The $\overline{\text{MCLR}}$ pin is a Schmitt Trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 27.0 “Electrical Characteristics”** for minimum pulse width specifications. The External Reset ($\overline{\text{MCLR}}$) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the $\overline{\text{MCLR}}$ Reset.

6.4.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This external Reset signal can be directly connected to the $\overline{\text{MCLR}}$ pin to reset the device when the rest of system is reset.

6.4.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the External Reset pin ($\overline{\text{MCLR}}$) should be tied directly or resistively to V_{DD} . In this case, the $\overline{\text{MCLR}}$ pin will not be used to generate a Reset. The External Reset pin ($\overline{\text{MCLR}}$) does not have an internal pull-up and must not be left unconnected.

6.5 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert $\overline{\text{SYSRST}}$, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will remain. $\overline{\text{SYSRST}}$ is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control (RCON<6>) register is set to indicate the Software Reset.

6.6 Watchdog Timer Time-out Reset (WDTO)

Whenever a Watchdog Timer Time-out Reset occurs, the device will asynchronously assert $\overline{\text{SYSRST}}$. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 24.4 “Watchdog Timer (WDT)”** for more information on the Watchdog Timer Reset.

6.7 Trap Conflict Reset

If a lower priority hard trap occurs while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Level 13 through Level 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 “Interrupt Controller”** for more information on Trap Conflict Resets.

6.8 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control (RCON<14>) register is set to indicate the illegal condition device Reset.

6.8.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

6.8.2 UNINITIALIZED W REGISTER RESET

Any attempt to use the Uninitialized W register as an Address Pointer will reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

6.8.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a Security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a call, jump, computed jump, return, return from subroutine or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an interrupt or trap vector.

Refer to **Section 24.8 “Code Protection and CodeGuard™ Security”** for more information on Security Reset.

REGISTER 7-13: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

bit 2	OC1IE: Output Compare Channel 1 Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 1	IC1IE: Input Capture Channel 1 Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 0	INT0IE: External Interrupt 0 Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled

10.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).
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11.0 I/O PORTS

- Note 1:** This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**I/O Ports**” (DS70193) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through”, in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

REGISTER 17-2: DFLT_xCON: DIGITAL FILTER x CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IMV1	IMV0	CEID
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
QEOUT	QECK2	QECK1	QECK0	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-9 **IMV<1:0>:** Index Match Value bits
 These bits allow the user application to specify the state of the QEAx and QEBx input pins during an index pulse when the POSxCNT register is to be reset.
In x4 Quadrature Count Mode:
 IMV1 = Required state of Phase B input signal for match on index pulse
 IMV0 = Required state of Phase A input signal for match on index pulse
In x2 Quadrature Count Mode:
 IMV1 = Selects phase input signal for index state match (0 = Phase A, 1 = Phase B)
 IMV0 = Required state of the selected phase input signal for match on index pulse
- bit 8 **CEID:** Count Error Interrupt Disable bit
 1 = Interrupts due to count errors are disabled
 0 = Interrupts due to count errors are enabled
- bit 7 **QEOUT:** QEAx/QEBx/INDXx Pin Digital Filter Output Enable bit
 1 = Digital filter outputs are enabled
 0 = Digital filter outputs are disabled (normal pin operation)
- bit 6-4 **QECK<2:0>:** QEAx/QEBx/INDXx Digital Filter Clock Divide Select Bits
 111 = 1:256 clock divide
 110 = 1:128 clock divide
 101 = 1:64 clock divide
 100 = 1:32 clock divide
 011 = 1:16 clock divide
 010 = 1:4 clock divide
 001 = 1:2 clock divide
 000 = 1:1 clock divide
- bit 3-0 **Unimplemented:** Read as '0'

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

- bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.
- bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware is set or clear after reception of an I²C device address byte.
- bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.
- bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of the data transmission.

REGISTER 22-9: ADCPC3: ADC CONVERT PAIR CONTROL REGISTER 3 (CONTINUED)

bit 4-0 **TRGSRC6<4:0>**: Trigger 6 Source Selection bits
Selects trigger source for conversion of Analog Channels AN13 and AN12.

11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

24.2 On-Chip Voltage Regulator

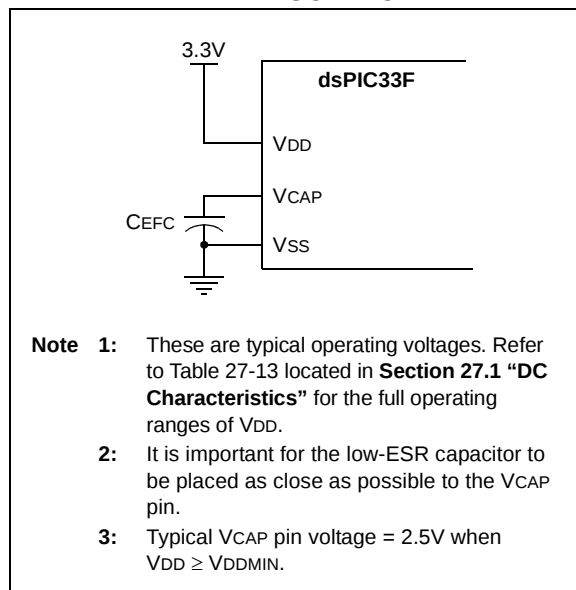
The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 24-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 27-13, located in Section 27.1 “DC Characteristics”.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 24-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



24.3 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is ‘1’.

Concurrently, the Power-up Timer (PWRT) Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

24.4 Watchdog Timer (WDT)

For dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

24.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32.767 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32.767 kHz input, the prescaler yields a nominal WDT Time-out (TWDT) period of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods, ranging from 1 ms to 131 seconds, can be achieved.

TABLE 27-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
Program Flash Memory							
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	V _{MIN}	—	3.6	V	V _{MIN} = Minimum operating voltage
D132B	VPEW	VDD for Self-Timed Write	V _{MIN}	—	3.6	V	V _{MIN} = Minimum operating voltage
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D136a	TRW	Row Write Time	1.488	—	1.518	ms	TRW = 11064 FRC cycles, TA = +85°C (See Note 2)
D136b	TRW	Row Write Time	1.473	—	1.533	ms	TRW = 11064 FRC cycles, TA = +125°C (See Note 2)
D137a	TPE	Page Erase Time	22.7	—	23.1	ms	TPE = 168517 FRC cycles, TA = +85°C (See Note 2)
D137b	TPE	Page Erase Time	22.4	—	23.3	ms	TPE = 168517 FRC cycles, TA = +125°C (See Note 2)
D138a	TWW	Word Write Cycle Time	47.7	—	48.7	μs	TWW = 355 FRC cycles, TA = +85°C (See Note 2)
D138b	TWW	Word Write Cycle Time	47.3	—	49.2	μs	TWW = 355 FRC cycles, TA = +125°C (See Note 2)

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

- Note 2:** Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min.), TUN<5:0> = b'100000 (for Max.). This parameter depends on the FRC accuracy (see Table 27-20) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the minimum and maximum time, see **Section 5.3 "Programming Operations"**.

TABLE 27-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
—	CEFC	External Filter Capacitor Value ⁽¹⁾	22	—	—	μF	Capacitor must be low series resistance (< 0.5 Ohms)

Note 1: Typical VCAP voltage = 2.5 volts when VDD ≥ VDDMIN.

TABLE 27-17: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	100	—	200	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-3	0.5	3	%	Measured over a 100 ms period

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

- 2:** These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks, use this formula:

$$\text{Peripheral Clock Jitter} = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{\text{Peripheral Bit Rate Clock}}\right)}}$$

For example: FOSC = 32 MHz, DCLK = 3%, SPI bit rate clock (i.e., SCK) is 2 MHz.

$$\text{SPI SCK Jitter} = \left[\frac{DCLK}{\sqrt{\left(\frac{32 \text{ MHz}}{2 \text{ MHz}}\right)}} \right] = \left[\frac{3\%}{\sqrt{16}} \right] = \left[\frac{3\%}{4} \right] = 0.75\%$$

TABLE 27-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS56	FHPOUT	On-Chip, 16x PLL CCO Frequency	112	118	120	MHz	
OS57	FHPIN	On-Chip, 16x PLL Phase Detector Input Frequency	7.0	7.37	7.5	MHz	
OS58	Tsu	Frequency Generator Lock Time	—	—	10	μs	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

TABLE 27-19: AC CHARACTERISTICS: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz ⁽¹⁾							
F20a	FRC	-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	—	+2	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN<5:0> bits can be used to compensate for temperature drift.

TABLE 27-20: AC CHARACTERISTICS: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
LPRC @ 32.768 kHz ⁽¹⁾						
F21a	LPRC	-40	—	+40	%	-40°C ≤ TA ≤ +85°C
F21b	LPRC	-50	—	+50	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 27-30: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 27-31	—	—	0,1	0,1	0,1
10 MHz	—	Table 27-32	—	1	0,1	1
10 MHz	—	Table 27-33	—	0	0,1	1
15 MHz	—	—	Table 27-34	1	0	0
11 MHz	—	—	Table 27-35	1	1	0
15 MHz	—	—	Table 27-36	0	1	0
11 MHz	—	—	Table 27-37	0	0	0

FIGURE 27-11: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS

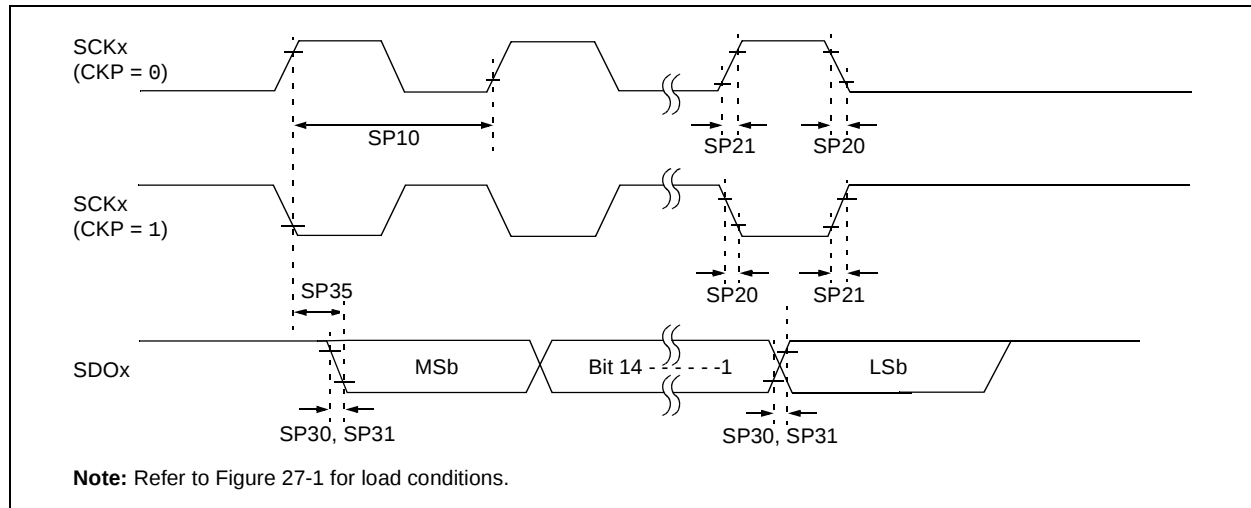
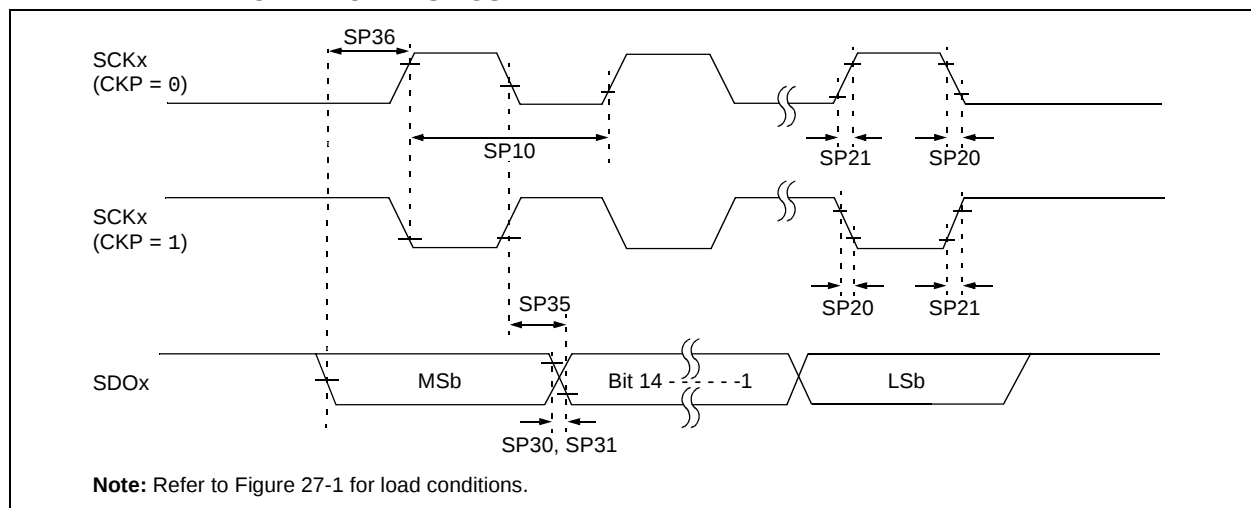
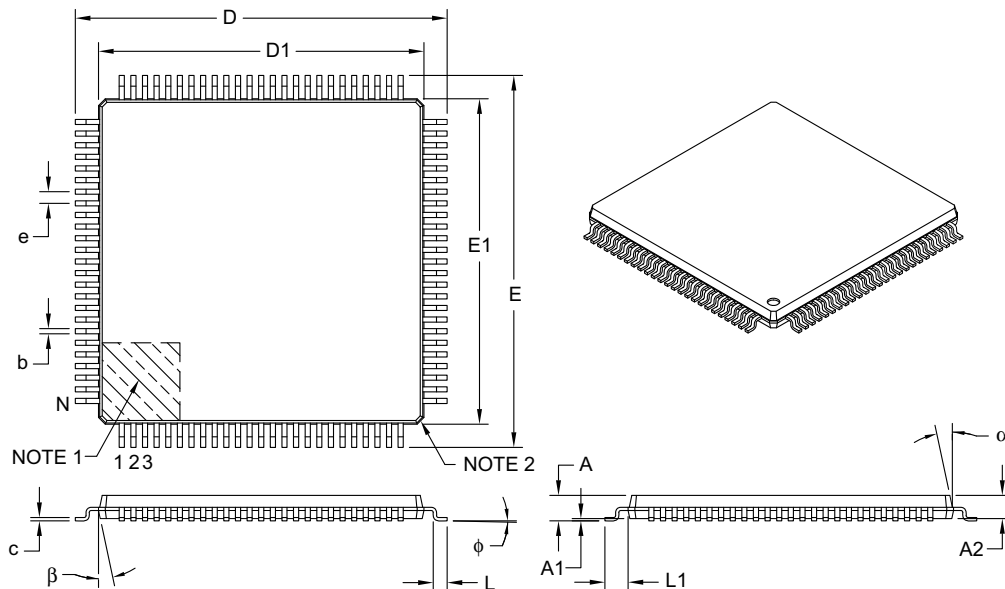


FIGURE 27-12: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	16.00 BSC		
Overall Length	D	16.00 BSC		
Molded Package Width	E1	14.00 BSC		
Molded Package Length	D1	14.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B