Microchip Technology - DSPIC33FJ32GS608-I/PT Datasheet

Welcome to E-XFL.COM

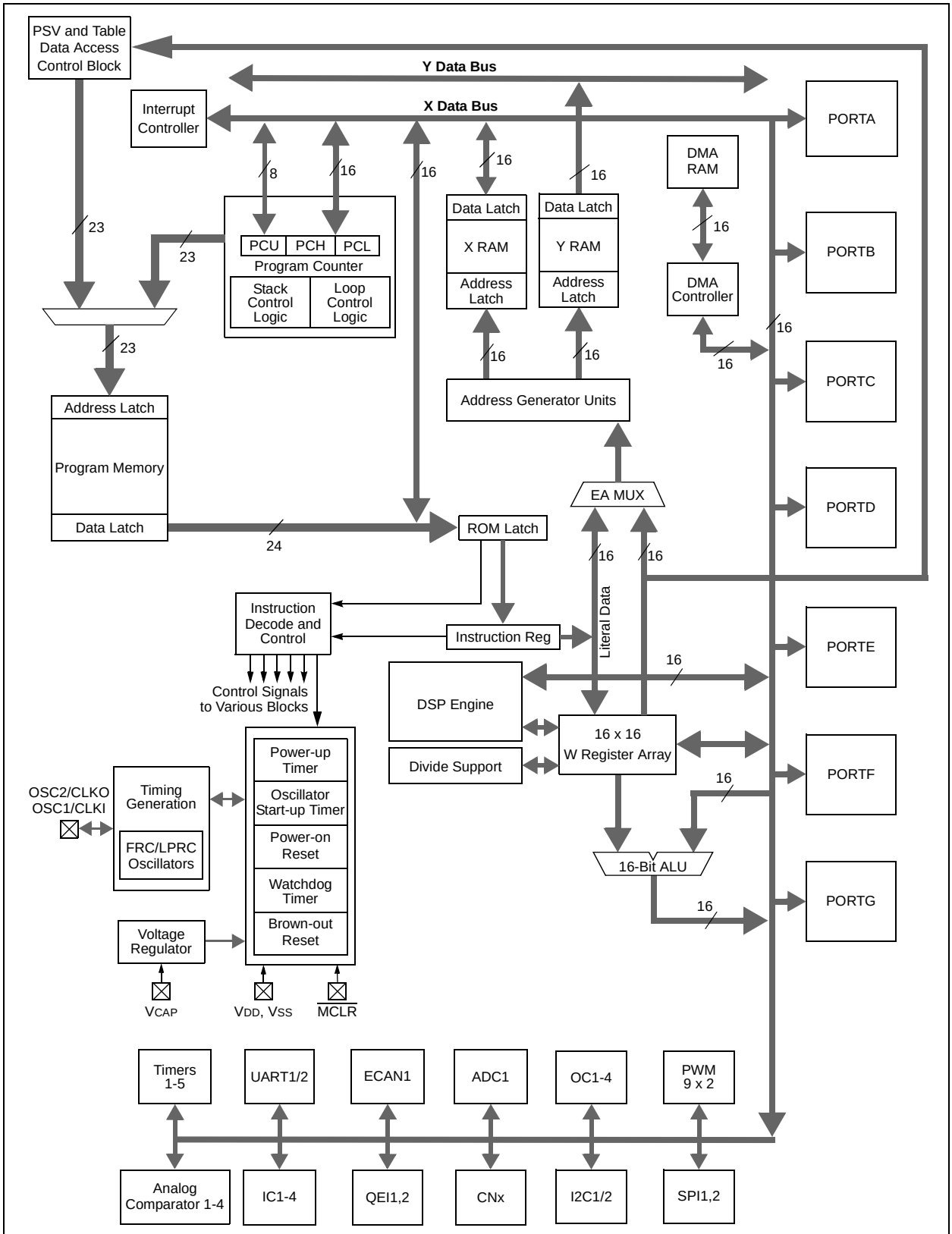
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, QEI, POR, PWM, WDT
Number of I/O	74
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gs608-i-pt

FIGURE 1-1: DEVICE BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

6.1 System Reset

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices have two types of Reset:

- Cold Reset
- Warm Reset

A Cold Reset is the result of a Power-on Reset (POR) or a Brown-out Reset (BOR). On a Cold Reset, the FNOSCx Configuration bits in the FOSC Configuration register select the device clock source.

A Warm Reset is the result of all the other Reset sources, including the RESET instruction. On Warm Reset, the device will continue to operate from the current clock source as indicated by the Current Oscillator Selection (COSC<2:0>) bits in the Oscillator Control (OSCCON<14:12>) register.

The device is kept in a Reset state until the system power supplies have stabilized at appropriate levels and the oscillator clock is ready. The sequence in which this occurs is described in Figure 6-2.

TABLE 6-1: OSCILLATOR DELAY

Oscillator Mode	Oscillator Start-up Delay	Oscillator Start-up Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	T_{OSCD}(1)	—	—	T_{OSCD}(1)
FRCPLL	T_{OSCD}(1)	—	T_{LOCK}(3)	T_{OSCD} + T_{LOCK}(1,3)
XT	T_{OSCD}(1)	T_{OST}(2)	—	T_{OSCD} + T_{OST}(1,2)
HS	T_{OSCD}(1)	T_{OST}(2)	—	T_{OSCD} + T_{OST}(1,2)
EC	—	—	—	—
XTPLL	T_{OSCD}(1)	T_{OST}(2)	T_{LOCK}(3)	T_{OSCD} + T_{OST} + T_{LOCK}(1,2,3)
HSPLL	T_{OSCD}(1)	T_{OST}(2)	T_{LOCK}(3)	T_{OSCD} + T_{OST} + T_{LOCK}(1,2,3)
ECPLL	—	—	T_{LOCK}(3)	T_{LOCK}(3)
LPRC	T_{OSCD}(1)	—	—	T_{OSCD}(1)

Note 1: T_{OSCD} = Oscillator start-up delay (1.1 μs max. for FRC, 70 μs max. for LPRC). Crystal oscillator start-up times vary with the crystal characteristics, load capacitance, etc.

2: T_{OST} = Oscillator Start-up Timer (OST) delay (1024 oscillator clock period). For example, T_{OST} = 102.4 μs for a 10 MHz crystal and T_{OST} = 32 ms for a 32 kHz crystal.

3: T_{LOCK} = PLL lock time (1.5 ms nominal) if PLL is enabled.

6.9 Using the RCON Status Bits

The user application can read the Reset Control (RCON) register after any device Reset to determine the cause of the Reset.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the Reset flag bit operation.

TABLE 6-3: RESET FLAG BIT OPERATION

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap Conflict Event	POR, BOR
IOPWR (RCON<14>)	Illegal Opcode or Uninitialized W register Access or Security Reset	POR, BOR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR, BOR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, CLRWDT Instruction, POR, BOR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR, BOR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR, BOR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits can be set or cleared by user software.

REGISTER 7-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	U-0
—	—	—	—	QEI2IF	—	PSESMIF	—
bit 15							bit 8

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	C1TXIF(1)	—	—	—	U2EIF	U1EIF	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **QEI2IF:** QEI2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **Unimplemented:** Read as '0'

bit 9 **PSESMIF:** PWM Special Event Secondary Match Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8-7 **Unimplemented:** Read as '0'

bit 6 **C1TXIF:** ECAN1 Transmit Data Request Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5-3 **Unimplemented:** Read as '0'

bit 2 **U2EIF:** UART2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U1EIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **Unimplemented:** Read as '0'

Note 1: Interrupts are disabled on devices without ECAN™ modules.

REGISTER 7-23: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **T3IP<2:0>:** Timer3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 7-27: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T4IP<2:0>:** Timer4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OC4IP<2:0>:** Output Compare Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **OC3IP<2:0>:** Output Compare Channel 3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DMA2IP<2:0>:** DMA Channel 2 Data Transfer Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70196) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. Devices can manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate. This includes the items such as the Input Change Notification on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device will wake-up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD(1)	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	ADCMD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **QEI1MD:** QEI1 Module Disable bit
1 = QEI1 module is disabled
0 = QEI1 module is enabled

bit 9 **PWMMD:** PWM Module Disable bit(1)
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

Note 1: Once the PWM module is re-enabled (PWMMD is set to '1' and then set to '0'), all PWM registers must be re-initialized.

The Timer2/3/4/5 modules can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous Counter mode, the input clock is derived from the external clock input at the TxCK pin.

The timer modes are determined by the following bits:

- TCS (TxCON<1>): Timer Clock Source Control bit
- TGATE (TxCON<6>): Timer Gate Control bit

Timer control bit settings for different operating modes are given in the Table 13-1.

TABLE 13-1: TIMER MODE SETTINGS

Mode	TCS	TGATE
Timer	0	0
Gated Timer	0	1
Synchronous Counter	1	x

13.1 16-Bit Operation

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit.

13.2 32-Bit Operation

A 32-bit timer module can be formed by combining a Type B and a Type C 16-bit timer module. For 32-bit timer operation, the T32 control bit in the Type B Timer Control (TxCON<3>) register must be set. The Type C timer holds the most significant word (msw) and the Type B timer holds the least significant word (lsw) for 32-bit operation.

When configured for 32-bit operation, only the Type B Timerx Control (TxCON) register bits are required for setup and control while the Type C Timer Control register bits are ignored (except the TSIDL bit).

For interrupt control, the combined 32-bit timer uses the interrupt enable, interrupt flag and interrupt priority control bits of the Type C timer. The interrupt control and status bits for the Type B timer are ignored during 32-bit timer operation.

The timers that can be combined to form a 32-bit timer are listed in Table 13-2.

TABLE 13-2: 32-BIT TIMER

Type B Timer (lsw)	Type C Timer (msw)
Timer2	Timer3
TImer4	Timer5

A block diagram representation of the 32-bit timer module is shown in Figure 13-3. The 32-timer module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

To configure the timer features for 32-bit operation:

1. Set the T32 control bit.
2. Select the prescaler ratio for Timer2 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
4. Load the timer period value. PR3 contains the most significant word of the value, while PR2 contains the least significant word.
5. If interrupts are required, set the interrupt enable bit, T3IE. Use the priority bits, T3IP<2:0>, to set the interrupt priority. While Timer2 controls the timer, the interrupt appears as a Timer3 interrupt.
6. Set the corresponding TON bit.

REGISTER 16-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(1)

1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event

•

•

•

0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event

0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 16-16: DTRx: PWM DEAD-TIME x REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Value for PWMx Dead-Time Unit bits

REGISTER 16-17: ALTDTRx: PWM ALTERNATE DEAD-TIME x REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Value for PWMx Dead-Time Unit bits

REGISTER 16-23: LEBCONx: LEADING-EDGE BLANKING CONTROL x REGISTER (CONTINUED)

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

22.0 HIGH-SPEED, 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed 10-Bit ADC"** (DS70000321) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices provide high-speed successive approximation Analog-to-Digital conversions to support applications, such as AC/DC and DC/DC power converters.

22.1 Features Overview

The ADC module incorporates the following features:

- 10-Bit Resolution
- Unipolar Inputs
- Up to Two Successive Approximation Registers (SARs)
- Up to 24 External Input Channels
- Two Internal Analog Inputs
- Dedicated Result Register for each Analog Input
- ±1 LSB Accuracy at 3.3V
- Single Supply Operation
- 4 Msps Conversion Rate at 3.3V (devices with two SARs)
- 2 Msps Conversion Rate at 3.3V (devices with one SAR)
- Low-Power CMOS Technology

22.2 Module Description

This ADC module is designed for applications that require low latency between the request for conversion and the resultant output data. Typical applications include:

- AC/DC Power Supplies
- DC/DC Converters
- Power Factor Correction (PFC)

This ADC works with the High-Speed PWM module in power control applications that require high-frequency control loops. This module can Sample-and-Convert two analog inputs in a 0.5 microsecond when two SARs are used. This small conversion delay reduces the "phase lag" between measurement and control system response.

Up to five inputs may be sampled at a time (four inputs from the dedicated Sample-and-Hold circuits and one from the shared Sample-and-Hold circuit). If multiple inputs request conversion, the ADC will convert them in a sequential manner, starting with the lowest order input.

This ADC design provides each pair of analog inputs (AN1, AN0), (AN3, AN2),..., the ability to specify its own trigger source out of a maximum of sixteen different trigger sources. This capability allows this ADC to Sample-and-Convert analog inputs that are associated with PWM generators operating on independent time bases.

The user application typically requires synchronization between analog data sampling and PWM output to the application circuit. The very high-speed operation of this ADC module allows "data on demand".

In addition, several hardware features have been added to the peripheral interface to improve real-time performance in a typical DSP-based application.

- Result Alignment Options
- Automated Sampling
- External Conversion Start Control
- Two Internal Inputs to Monitor the INTREF and EXTREF Input Signals

Block diagrams of the ADC module for the family devices are shown in Figure 22-1 through Figure 22-4.

REGISTER 22-7: ADCPC1: ADC CONVERT PAIR CONTROL REGISTER 1 (CONTINUED)

bit 12-8 **TRGSRC3<4:0>:** Trigger 3 Source Selection bits

Selects trigger source for conversion of analog channels AN7 and AN6.
11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger is selected
10101 = PWM Generator 8 secondary trigger is selected
10100 = PWM Generator 7 secondary trigger is selected
10011 = PWM Generator 6 secondary trigger is selected
10010 = PWM Generator 5 secondary trigger is selected
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = PWM secondary Special Event Trigger is selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger is selected
01010 = PWM Generator 7 primary trigger is selected
01001 = PWM Generator 6 primary trigger is selected
01000 = PWM Generator 5 primary trigger is selected
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

bit 7 **IRQEN2:** Interrupt Request Enable 2 bit

1 = Enables IRQ generation when requested conversion of Channels AN5 and AN4 is completed
0 = IRQ is not generated

bit 6 **PEND2:** Pending Conversion Status 2 bit

1 = Conversion of Channels AN5 and AN4 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5 **SWTRG2:** Software Trigger 2 bit

1 = Starts conversion of AN5 and AN4 (if selected by the TRGSRCx<4:0> bits)**(1)**
This bit is automatically cleared by hardware when the PEND2 bit is set.
0 = Conversion has not started

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

23.3 Module Applications

This module provides a means for the SMPS dsPIC® DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 10-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample-and-Convert Process
- Truncate the PWM Signal (current limit)
- Truncate the PWM Period (current minimum)
- Disable the PWM Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) generate an interrupt, 2) have the ADC take a sample and convert it, and 3) truncate the PWM output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

23.4 DAC

The range of the DAC is controlled via an analog multiplexer that selects either AVDD/2, an internal reference source, INTREF, or an external reference source, EXTREF. The full range of the DAC (AVDD/2) will typically be used when the chosen input source pin is shared with the ADC. The reduced range option (INTREF) will likely be used when monitoring current levels using a current sense resistor. Usually, the measured voltages in such applications are small (<1.25V); therefore the option of using a reduced reference range for the comparator extends the available DAC resolution in these applications. The use of an external reference enables the user to connect to a reference that better suits their application.

DACOUT, shown in Figure 23-1, can only be associated with a single comparator at a given time.

Note:	It should be ensured in software that multiple DACOE bits are not set. The output on the DACOUT pin will be indeterminate if multiple comparators enable the DAC output.

23.5 Interaction with I/O Buffers

If the comparator module is enabled and a pin has been selected as the source for the comparator, then the chosen I/O pad must disable the digital input buffer associated with the pad to prevent excessive currents in the digital buffer due to analog input voltages.

23.6 Digital Logic

The CMPCONx register (see Register 23-1) provides the control logic that configures the comparator module. The digital logic provides a glitch filter for the comparator output to mask transient signals in less than two instruction cycles. In Sleep or Idle mode, the glitch filter is bypassed to enable an asynchronous path from the comparator to the interrupt controller. This asynchronous path can be used to wake-up the processor from Sleep or Idle mode.

The comparator can be disabled while in Idle mode if the CMPSIDL bit is set. If a device has multiple comparators, if any CMPSIDL bit is set, then the entire group of comparators will be disabled while in Idle mode. This behavior reduces complexity in the design of the clock control logic for this module.

The digital logic also provides a one TCY width pulse generator for triggering the ADC and generating interrupt requests.

The CMPDACx (see Register 23-2) register provides the digital input value to the reference DAC.

If the module is disabled, the DAC and comparator are disabled to reduce power consumption.

23.7 Comparator Input Range

The comparator has a limitation for the input Common-Mode Range (CMR) of (AVDD – 1.5V), typical. This means that both inputs should not exceed this range. As long as one of the inputs is within the Common-Mode Range, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated.

If both inputs exceed the CMR, the comparator output will be indeterminate.

23.8 DAC Output Range

The DAC has a limitation for the maximum reference voltage input of (AVDD – 1.6) volts. An external reference voltage input should not exceed this value or the reference DAC output will become indeterminate.

23.9 Comparator Registers

The comparator module is controlled by the following registers:

- CMPCONx: Comparator Control x Register
- CMPDACx: Comparator DAC Control x Register

TABLE 27-42: COMPARATOR MODULE SPECIFICATIONS

AC and DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
CM10	VIOFF	Input Offset Voltage		±5	±15	mV	
CM11	VICM	Input Common-Mode Voltage Range(1)	0	—	AVDD – 1.5	V	
CM12	VGAIN	Open-Loop Gain(1)	90	—	—	db	
CM13	CMRR	Common-Mode Rejection Ratio(1)	70	—	—	db	
CM14	TRESP	Large Signal Response		20	30	ns	V+ input step of 100 mv while V- input held at AVDD/2. Delay measured from analog input pin to PWM output pin.

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 27-43: DAC MODULE SPECIFICATIONS

AC and DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DA01	EXTREF	External Reference Voltage(1)	0	—	AVDD – 1.6	V	
DA08	INTREF	Internal Reference Voltage(1)	1.25	1.32	1.41	V	
DA02	CVRES	Resolution	10 data bits			bits	
DA03	INL	Integral Nonlinearity Error	—	±1.0	—	—	AVDD = 3.3V, DACREF = (AVDD/2)V
DA04	DNL	Differential Nonlinearity Error	—	±0.8	—	LSB	
DA05	EOFF	Offset Error	—	±2.0	—	LSB	
DA06	EG	Gain Error	—	±2.0	—	LSB	
DA07	TSET	Settling Time(1)	—	—	650	nsec	Measured when range = 1 (high range) and CMREF<9:0> transitions from 0x1FF to 0x300.

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 28-3: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

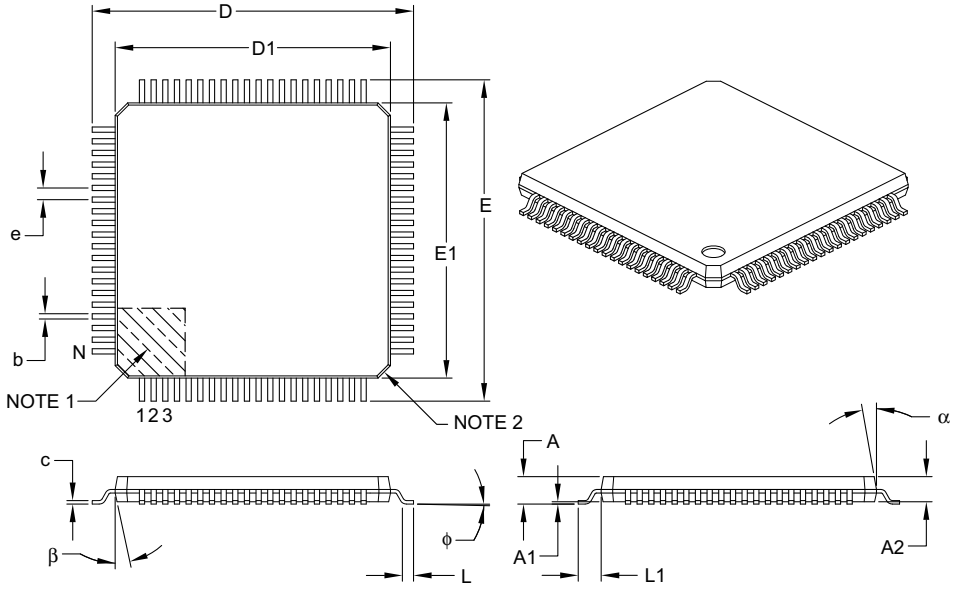
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off Clock On Base Current(1)						
MDC45d	40	50	mA	-40°C	3.3V	50 MIPS
MDC45a	40	50	mA	+25°C		
MDC45b	40	50	mA	+85°C		

Note 1: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are '0's)
- JTAG is disabled

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 27.0 "Electrical Characteristics" (Continued)	Updated the Timer1, Timer2, and Timer3 External Clock Timing Requirements (see Table 27-23, Table 27-24, and Table 27-25). Updated the Simple OC/PWM Mode Timing Requirements (see Table 27-28). Updated all SPI Timing specifications (see Figure 27-11-Figure 27-18 and Table 27-30-Table 27-37). Added Note 2 to the 10-bit High-Speed ADC Module Specifications (see Table 27-40). Added Note 2 to the 10-bit High-Speed ADC Module Timing Requirements (see Table 27-41). Added parameter DA08 to the DAC Module Specifications (see Table 27-43). Updated parameter DA16 in the DAC Output Buffer Specifications (see Table 27-44). Added DMA Read/Write Timing Requirements (see Table 27-49).
Section 28.0 "50 MIPS Electrical Characteristics"	Added new chapter with electrical specifications for 50 MIPS devices.
Section 29.0 "DC and AC Device Characteristics Graphs"	Added new chapter.

Revision E (October 2012)

This revision removes the Preliminary watermark and includes minor typographical and formatting changes throughout the data sheet.

Revision F (July 2014)

Changes CHOP bit to CHOPCLK in the High Speed PWM Register Map and CHOPCLK PWMCHOP Clock Generator Register (see Register 4-16 and Register 16-9).

Changes values in the Minimum Row Write Time and Maximum Row Write time equation examples (see Equation 5-2 and Equation 5-3).

Adds the Oscillator Delay table (see Table 6-2).

Updates TUN bit ranges in the OSCTUN: Oscillator Tuning Register (see Register 9-4).

Updates the Type C Timer Block Diagram (see Figure 13-2).

Adds Note 1 to the CxFCTRL: ECANx FIFO Control Register (see Register 21-4).

Adds Note 10 to the DC Characteristics: I/O Pin Input Specifications (see Table 27-9).

Updates values in the DC Characteristics: Program Memory Table (see Table 27-12).

Adds Register 29-7 through Register 29-12 to **Section 29.0 "DC and AC Device Characteristics Graphs"**

Also includes minor typographical and formatting changes throughout the data sheet.