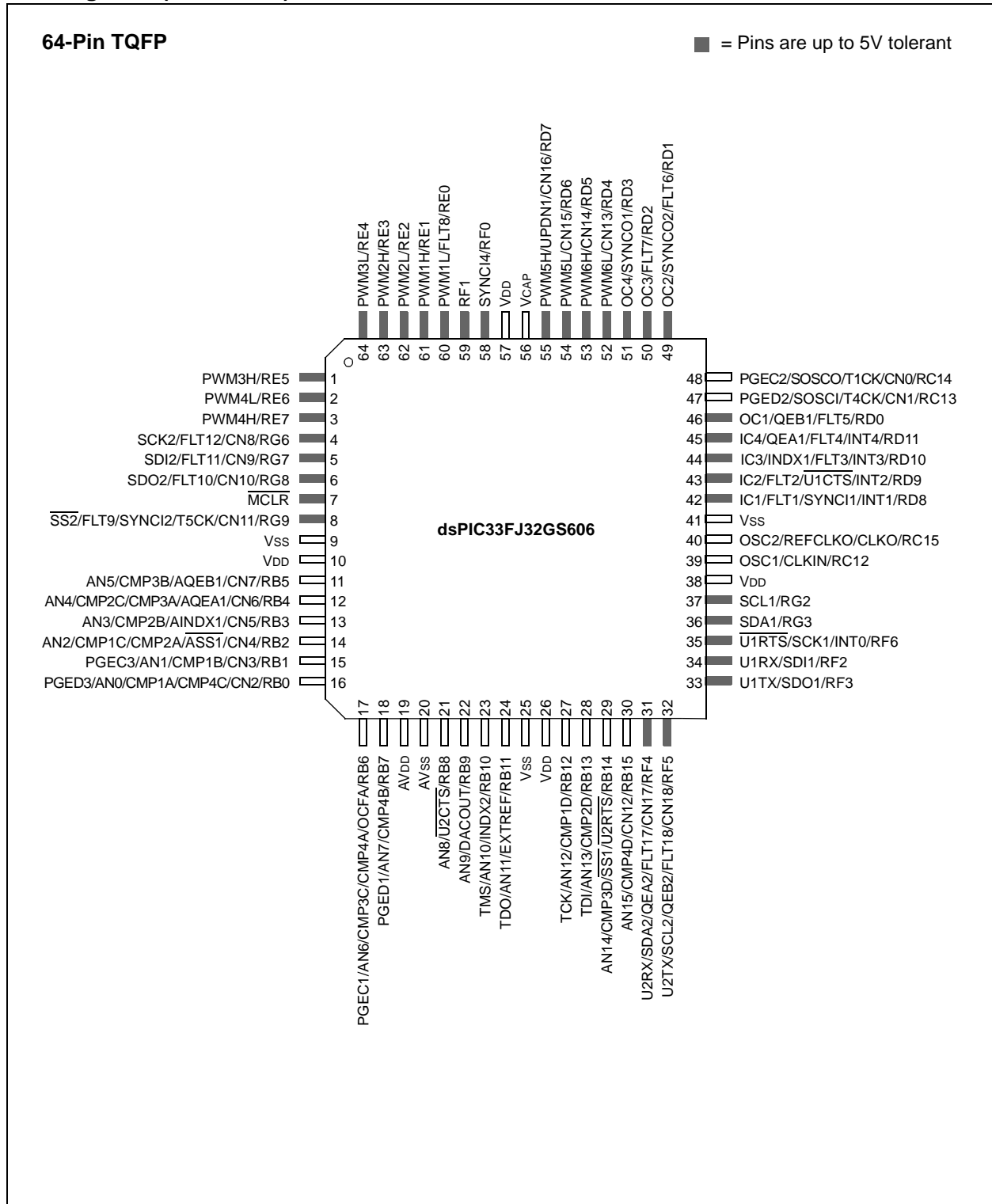**What is "[Embedded - Microcontrollers](#)"?**

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

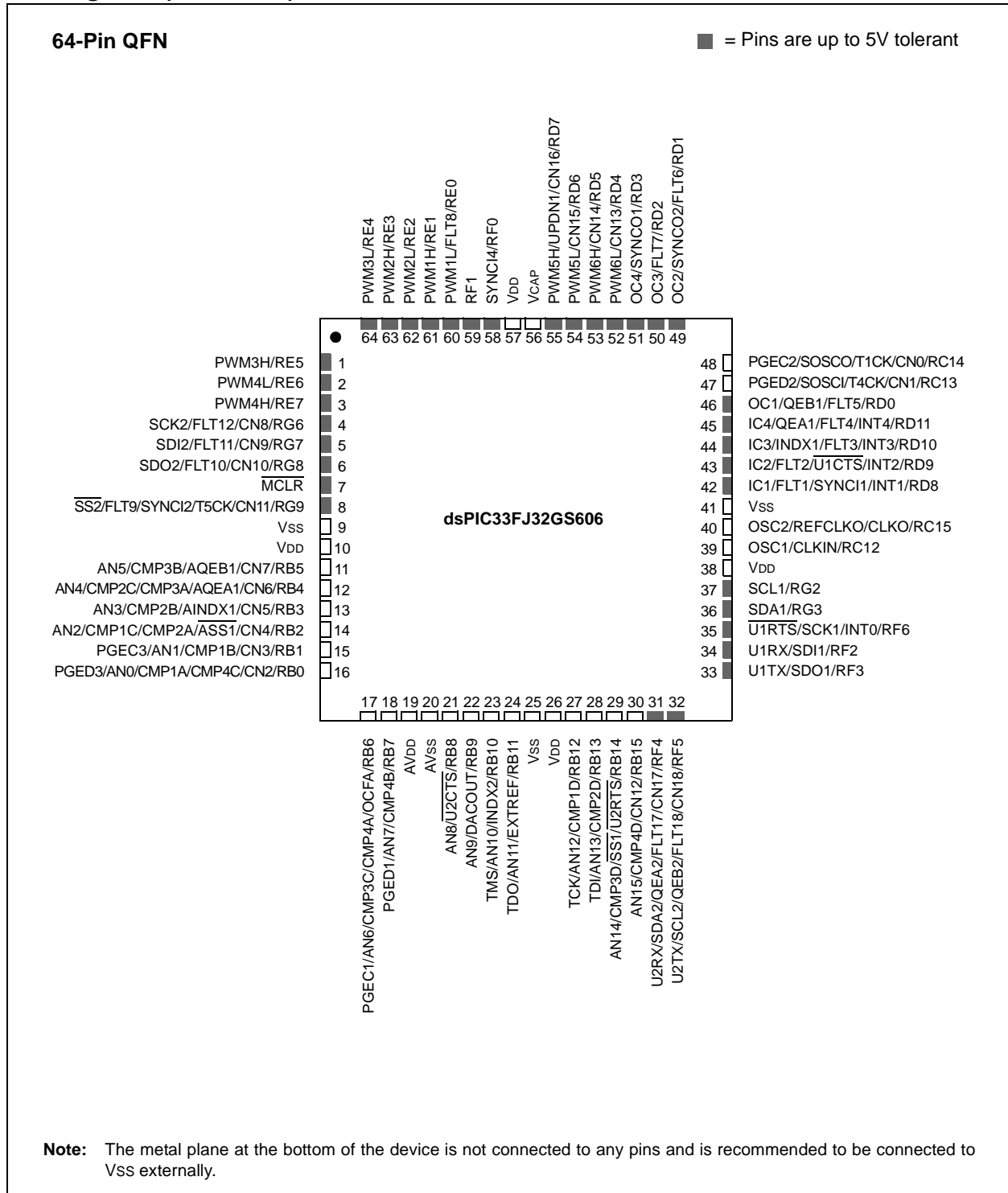**Applications of "[Embedded - Microcontrollers](#)"**

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, QEI, POR, PWM, WDT
Number of I/O	85
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gs610-i-pt

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant

dsPIC33FJ32GS606

Left side pins (1–16):
- 1 — PWM3H/RE5
- 2 — PWM4L/RE6
- 3 — PWM4H/RE7
- 4 — SCK2/FLT12/CN8/RG6
- 5 — SDI2/FLT11/CN9/RG7
- 6 — SDO2/FLT10/CN10/RG8
- 7 — MCLR
- 8 — SS2/FLT9/SYNCI2/T5CK/CN11/RG9
- 9 — VSS
- 10 — VDD
- 11 — AN5/CMP3B/AQEB1/CN7/RB5
- 12 — AN4/CMP2C/CMP3A/AQEA1/CN6/RB4
- 13 — AN3/CMP2B/AINDX1/CN5/RB3
- 14 — AN2/CMP1C/CMP2A/ASS1/CN4/RB2
- 15 — PGEC3/AN1/CMP1B/CN3/RB1
- 16 — PGED3/AN0/CMP1A/CMP4C/CN2/RB0

Top pins (64–49):
- 64 — PWM3L/RE4
- 63 — PWM2H/RE3
- 62 — PWM2L/RE2
- 61 — PWM1H/RE1
- 60 — PWM1L/FLT8/RE0
- 59 — RF1
- 58 — SYNCI4/RF0
- 57 — VDD
- 56 — VCAP
- 55 — PWM5H/UPDN1/CN16/RD7
- 54 — PWM5L/CN15/RD6
- 53 — PWM6H/CN14/RD5
- 52 — PWM6L/CN13/RD4
- 51 — OC4/SYNCO1/RD3
- 50 — OC3/FLT7/RD2
- 49 — OC2/SYNCO2/FLT6/RD1

Right side pins (48–33):
- 48 — PGEC2/SOSCO/T1CK/CN0/RC14
- 47 — PGED2/SOSCI/T4CK/CN1/RC13
- 46 — OC1/QEB1/FLT5/RD0
- 45 — IC4/QEA1/FLT4/INT4/RD11
- 44 — IC3/INDX1/FLT3/INT3/RD10
- 43 — IC2/FLT2/U1CTS/INT2/RD9
- 42 — IC1/FLT1/SYNCI1/INT1/RD8
- 41 — VSS
- 40 — OSC2/REFCLKO/CLKO/RC15
- 39 — OSC1/CLKIN/RC12
- 38 — VDD
- 37 — SCL1/RG2
- 36 — SDA1/RG3
- 35 — U1RTS/SCK1/INT0/RF6
- 34 — U1RX/SDI1/RF2
- 33 — U1TX/SDO1/RF3

Bottom pins (17–32):
- 17 — PGEC1/AN6/CMP3C/CMP4A/OCFA/RB6
- 18 — PGED1/AN7/CMP4B/RB7
- 19 — AVDD
- 20 — AVSS
- 21 — AN8/U2CTS/RB8
- 22 — AN9/DACOUT/RB9
- 23 — TMS/AN10/INDX2/RB10
- 24 — TDO/AN11/EXTREF/RB11
- 25 — VSS
- 26 — VDD
- 27 — TCK/AN12/CMP1D/RB12
- 28 — TDI/AN13/CMP2D/RB13
- 29 — AN14/CMP3D/SS1/U2RTS/RB14
- 30 — AN15/CMP4D/CN12/RB15
- 31 — U2RX/SDA2/QEA2/FLT17/CN17/RF4
- 32 — U2TX/SCL2/QEB2/FLT18/CN18/RF5

Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant

Top pins (64 to 49):
PWM3L/RE4 (64), PWM2H/RE3 (63), PWM2L/RE2 (62), PWM1H/RE1 (61), PWM1L/FLT8/RE0 (60), RF1 (59), SYNCI4/RF0 (58), VDD (57), VCAP (56), PWM5H/UPDN1/CN16/RD7 (55), PWM5L/CN15/RD6 (54), PWM6H/CN14/RD5 (53), PWM6L/CN13/RD4 (52), OC4/SYNCO1/RD3 (51), OC3/FLT7/RD2 (50), OC2/SYNCO2/FLT6/RD1 (49)

Left pins (1 to 16):
PWM3H/RE5 — 1
PWM4L/RE6 — 2
PWM4H/RE7 — 3
SCK2/FLT12/CN8/RG6 — 4
SDI2/FLT11/CN9/RG7 — 5
SDO2/FLT10/CN10/RG8 — 6
MCLR — 7
SS2/FLT9/SYNCI2/T5CK/CN11/RG9 — 8
VSS — 9
VDD — 10
AN5/CMP3B/AQEB1/CN7/RB5 — 11
AN4/CMP2C/CMP3A/AQEA1/CN6/RB4 — 12
AN3/CMP2B/AINDX1/CN5/RB3 — 13
AN2/CMP1C/CMP2A/ASS1/CN4/RB2 — 14
PGEC3/AN1/CMP1B/CN3/RB1 — 15
PGED3/AN0/CMP1A/CMP4C/CN2/RB0 — 16

Center: **dsPIC33FJ32GS606**

Right pins (48 to 33):
48 — PGEC2/SOSCO/T1CK/CN0/RC14
47 — PGED2/SOSCI/T4CK/CN1/RC13
46 — OC1/QEB1/FLT5/RD0
45 — IC4/QEA1/FLT4/INT4/RD11
44 — IC3/INDX1/FLT3/INT3/RD10
43 — IC2/FLT2/U1CTS/INT2/RD9
42 — IC1/FLT1/SYNCI1/INT1/RD8
41 — VSS
40 — OSC2/REFCLKO/CLKO/RC15
39 — OSC1/CLKIN/RC12
38 — VDD
37 — SCL1/RG2
36 — SDA1/RG3
35 — U1RTS/SCK1/INT0/RF6
34 — U1RX/SDI1/RF2
33 — U1TX/SDO1/RF3

Bottom pins (17 to 32):
PGEC1/AN6/CMP3C/CMP4A/OCFA/RB6 (17), PGED1/AN7/CMP4B/RB7 (18), AVDD (19), AVSS (20), AN8/U2CTS/RB8 (21), AN9/DACOUT/RB9 (22), TMS/AN10/INDX2/RB10 (23), TDO/AN11/EXTREF/RB11 (24), VSS (25), VDD (26), TCK/AN12/CMP1D/RB12 (27), TDI/AN13/CMP2D/RB13 (28), AN14/CMP3D/SS1/U2RTS/RB14 (29), AN15/CMP4D/CN12/RB15 (30), U2RX/SDA2/QEA2/FLT17/CN17/RF4 (31), U2TX/SCL2/QEB2/FLT18/CN18/RF5 (32)

Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant

dsPIC33FJ64GS610

Top pins (left to right, 100–76):
PWM3L/RE4, PWM2H/RE3, PWM2L/RE2, PWM9H/RG13, PWM9L/RG12, SYNCO1/FLT23/RG14, PWM1H/RE1, PWM1L/FLT8/RE0, AN23/CN23/RA7, AN22/CN22/RA6, INDX2/RG0, QEB2/RG1, C1TX/RF1, C1RX/RF0, VDD, VCAP, PWM5H/UPDN1/CN16/RD7, PWM5L/CN15/RD6, PWM6H/CN14/RD5, PWM6L/CN13/RD4, PWM7L/CN19/RD13, QEA2/RD12, PWM7H/OC4/RD3, OC3/FLT7/RD2, OC2/SYNCO2/FLT6/RD1

Left side pins (1–25):
1 SYNCI1/RG15
2 VDD
3 PWM3H/RE5
4 PWM4L/RE6
5 PWM4H/RE7
6 AN16/T2CK/RC1
7 AN17/T3CK/RC2
8 AN18/T4CK/RC3
9 AN19/T5CK/RC4
10 SCK2/FLT12/CN8/RG6
11 SDI2/FLT11/CN9/RG7
12 SDO2/FLT10/CN10/RG8
13 MCLR
14 SS2/FLT9/CN11/RG9
15 VSS
16 VDD
17 TMS/RA0
18 AN20/FLT13/INT1/RE8
19 AN21/FLT14/INT2/RE9
20 AN5/CMP3B/AQEB1/CN7/RB5
21 AN4/CMP2C/CMP3A/AQEA1/CN6/RB4
22 AN3/CMP2B/AINDX1/CN5/RB3
23 AN2/CMP1C/CMP2A/ASS1/CN4/RB2
24 PGEC3/AN1/CMP1B/CN3/RB1
25 PGED3/AN0/CMP1A/CMP4C/CN2/RB0

Right side pins (75–51):
75 VSS
74 PGEC2/SOSCO/T1CK/CN0/RC14
73 PGED2/SOSCI/CN1/RC13
72 OC1/QEB1/FLT5/RD0
71 IC4/QEA1/FLT4/RD11
70 IC3/INDX1/FLT3/RD10
69 IC2/FLT2/RD9
68 IC1/FLT1/RD8
67 INT4/FLT19/SYNCI4/RA15
66 INT3/FLT20/RA14
65 VSS
64 OSC2/REFCLKO/CLKO/RC15
63 OSC1/CLKIN/RC12
62 VDD
61 TDO/RA5
60 TDI/RA4
59 SDA2/FLT21/RA3
58 SCL2/FLT22/RA2
57 SCL1/RG2
56 SDA1/RG3
55 SCK1/INT0/RF6
54 SDI1/RF7
53 SDO1/RF8
52 U1RX/RF2
51 U1TX/RF3

Bottom pins (26–50):
26 PGEC1/AN6/CMP3C/CMP4A/OCFA/RB6
27 PGED1/AN7/CMP4B/RB7
28 PWM8L/RA9
29 PWM8H/RA10
30 AVDD
31 AVSS
32 AN8/RB8
33 AN9/DACOUT/RB9
34 AN10/RB10
35 AN11/EXTREF/RB11
36 VSS
37 VDD
38 TCK/RA1
39 U2RTS/RF13
40 U2CTS/RF12
41 AN12/CMP1D/RB12
42 AN13/CMP2D/RB13
43 AN14/CMP3D/SS1/RB14
44 AN15/CMP4D/CN12/RB15
45 VSS
46 VDD
47 U1CTS/FLT15/SYNCI3/CN20/RD14
48 U1RTS/FLT16/SYNCI2/CN21/RD15
49 U2RX/FLT17/CN17/RF4
50 U2TX/FLT18/CN18/RF5

TABLE 4-1: CPU CORE REGISTER MAP (CONTINUED)

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CORCON	0044	—	—	—	US	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0000
MODCON	0046	XMODEN	YMODEN	—	—	BWM3	BWM2	BWM1	BWM0	YWM3	YWM2	YWM1	YWM0	XWM3	XWM2	XWM1	XWM0	0000
XMODSRT	0048	XS<15:1>															0	xxxx
XMODEND	004A	XE<15:1>															1	xxxx
YMODSRT	004C	YS<15:1>															0	xxxx
YMODEND	004E	YE<15:1>															1	xxxx
XBREV	0050	BREN	XB14	XB13	XB12	XB11	XB10	XB9	XB8	XB7	XB6	XB5	XB4	XB3	XB2	XB1	XB0	xxxx
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610

TABLE 4-22: HIGH-SPEED PWM GENERATOR 6 REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON6	04C0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON6	04C2	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON6	04C4	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC6	04C6	PDC6<15:0>																0000
PHASE6	04C8	PHASE6<15:0>																0000
DTR6	04CA	—	—	DTR6<13:0>														0000
ALTDTR6	04CA	—	—	ALTDTR6<13:0>														0000
SDC6	04CE	SDC6<15:0>																0000
SPHASE6	04D0	SPHASE6<15:0>																0000
TRIG6	04D2	TRGCMP<12:0>													—	—	—	0000
TRGCON6	04D4	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG6	04D6	STRGCMP<12:0>													—	—	—	0000
PWMCAP6	04D8	PWMCAP<12:0>													—	—	—	0000
LEBCON6	04DA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY6	04DC	—	—	—	—	LEB<8:0>									—	—	—	0000
AUXCON6	04DE	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30:   SPI1 REGISTER MAP

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31:   SPI2 REGISTER MAP

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.2 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until V_{DD} crosses the V_{POR} threshold and the delay, T_{POR}, has elapsed. The delay, T_{POR}, ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 27.0 "Electrical Characteristics"** for details.

The Power-on Reset (POR) status bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.3 Brown-out Reset (BOR) and Power-up Timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the V_{DD} is too low (V_{DD} < V_{BOR}) for proper device operation. The BOR circuit keeps the device in Reset until V_{DD} crosses the V_{BOR} threshold and the delay, T_{BOR}, has elapsed. The delay, T_{BOR}, ensures the voltage regulator output becomes stable.

The Brown-out Reset (BOR) status bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the V_{DD} should rise to acceptable levels for full-speed operation. The PWRT provides a Power-up Time Delay (T_{PWRT}) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the SYSRST is released.

The Power-up Timer delay (T_{PWRT}) is programmed by the Power-on Reset Timer Value Select (FPWRT<2:0>) bits in the FPOR Configuration (FPOR<2:0>) register, which provides eight settings (from 0 ms to 128 ms). Refer to **Section 24.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (T_{BOR} + T_{PWRT}) is initiated each time V_{DD} rises above the V_{BOR} trip point

FIGURE 6-3: **BROWN-OUT SITUATIONS**
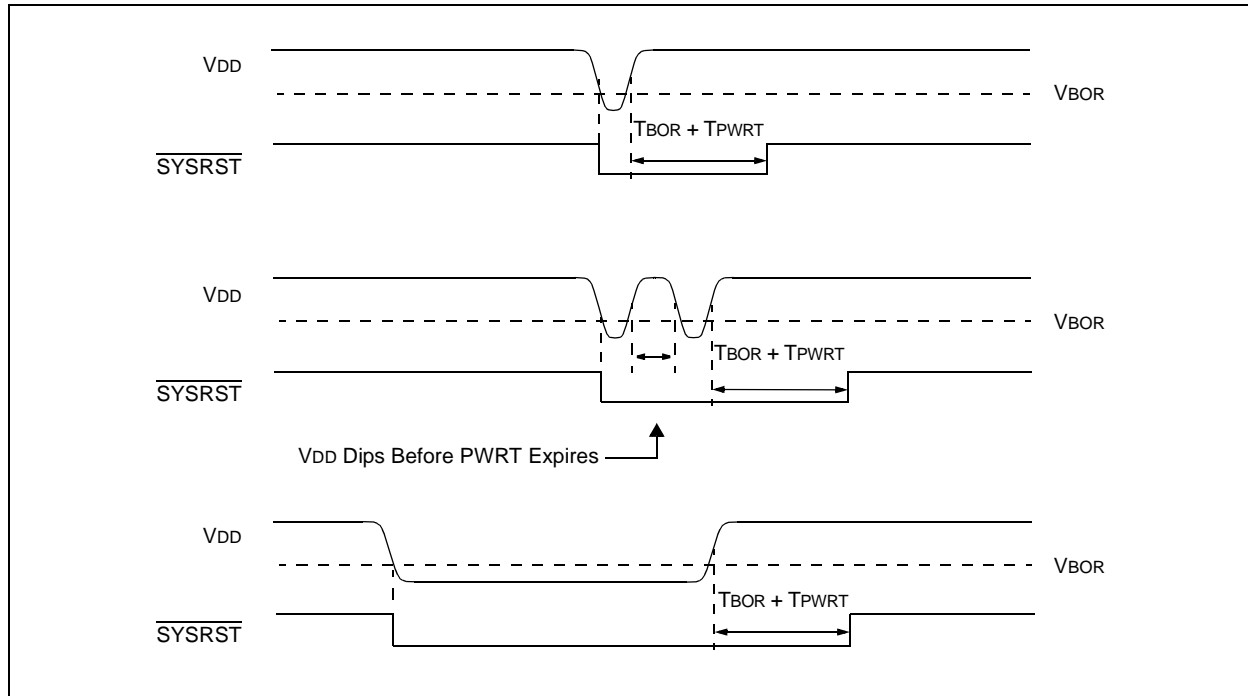
REGISTER 7-3:   INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **NSTDIS:** Interrupt Nesting Disable bit

1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14   **OVAERR:** Accumulator A Overflow Trap Flag bit

1 = Trap was caused by an overflow of Accumulator A
0 = Trap was not caused by an overflow of Accumulator A

bit 13   **OVBERR:** Accumulator B Overflow Trap Flag bit

1 = Trap was caused by an overflow of Accumulator B
0 = Trap was not caused by an overflow of Accumulator B

bit 12   **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit

1 = Trap was caused by a catastrophic overflow of Accumulator A
0 = Trap was not caused by a catastrophic overflow of Accumulator A

bit 11   **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit

1 = Trap was caused by a catastrophic overflow of Accumulator B
0 = Trap was not caused by a catastrophic overflow of Accumulator B

bit 10   **OVATE:** Accumulator A Overflow Trap Enable bit

1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9   **OVBTE:** Accumulator B Overflow Trap Enable bit

1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8   **COVTE:** Catastrophic Overflow Trap Enable bit

1 = Trap on a catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7   **SFTACERR:** Shift Accumulator Error Status bit

1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6   **DIV0ERR:** Arithmetic Error Status bit

1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5   **DMACERR:** DMA Controller Error Status bit

1 = DMA Controller error trap has occurred
0 = DMA Controller error trap has not occurred

bit 4   **MATHERR:** Arithmetic Error Status bit

1 = Math error trap has occurred
0 = Math error trap has not occurred

REGISTER 7-34:   IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	U2EIP2	U2EIP1	U2EIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11   **Unimplemented:** Read as '0'

bit 10-8   **U2EIP<2:0>:** UART2 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **U1EIP<2:0>:** UART1 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0   **Unimplemented:** Read as '0'

REGISTER 7-44:   IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP5IP2	ADCP5IP1	ADCP5IP0	—	ADCP4IP2	ADCP4IP1	ADCP4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP3IP2	ADCP3IP1	ADCP3IP0	—	ADCP2IP2	ADCP2IP1	ADCP2IP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **ADCP5IP<2:0>:** ADC Pair 5 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **ADCP4IP<2:0>:** ADC Pair 4 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **ADCP3IP<2:0>:** ADC Pair 3 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **ADCP2IP<2:0>:** ADC Pair 2 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

NOTES:

REGISTER 10-1:   PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3   **SPI1MD:** SPI1 Module Disable bit

1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2   **Unimplemented:** Read as '0'

bit 1   **C1MD:** ECAN1 Module Disable bit

1 = ECAN1 module is disabled
0 = ECAN1 module is enabled

bit 0   **ADCMD:** ADC Module Disable bit

1 = ADC module is disabled
0 = ADC module is enabled

Note 1:   Once the PWM module is re-enabled (PWMMD is set to '1' and then set to '0'), all PWM registers must be re-initialized.

REGISTER 20-2: **UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5   **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)

       1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
       0 = Address Detect mode is disabled

bit 4   **RIDLE:** Receiver Idle bit (read-only)

       1 = Receiver is Idle
       0 = Receiver is active

bit 3   **PERR:** Parity Error Status bit (read-only)

       1 = Parity error has been detected for the current character (the character at the top of the receive
           FIFO)
       0 = Parity error has not been detected

bit 2   **FERR:** Framing Error Status bit (read-only)

       1 = Framing error has been detected for the current character (the character at the top of the receive
           FIFO)
       0 = Framing error has not been detected

bit 1   **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)

       1 = Receive buffer has overflowed
       0 = Receive buffer has not overflowed; clearing a previously set OERR bit ($1 \rightarrow 0$ transition) will reset
           the receiver buffer and the UxRSR to the empty state

bit 0   **URXDA:** UARTx Receive Buffer Data Available bit (read-only)

       1 = Receive buffer has data, at least one more character can be read
       0 = Receive buffer is empty

Note 1: Refer to **"UART"** (DS70188) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for transmit operation. That section of the manual is available on the Microchip web site: www.microchip.com.

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-12   **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits

`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8   **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)

bit 7-4   **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)

bit 3-0   **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

FIGURE 22-3: ADC BLOCK DIAGRAM FOR dsPIC33FJ32GS608 AND dsPIC33FJ64GS608 DEVICES WITH TWO SARs

Note 1: AN24 (EXTREF) is an internal analog input. To measure the voltage at AN24 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN25 (INTREF) is an internal analog input and is not available on a pin.
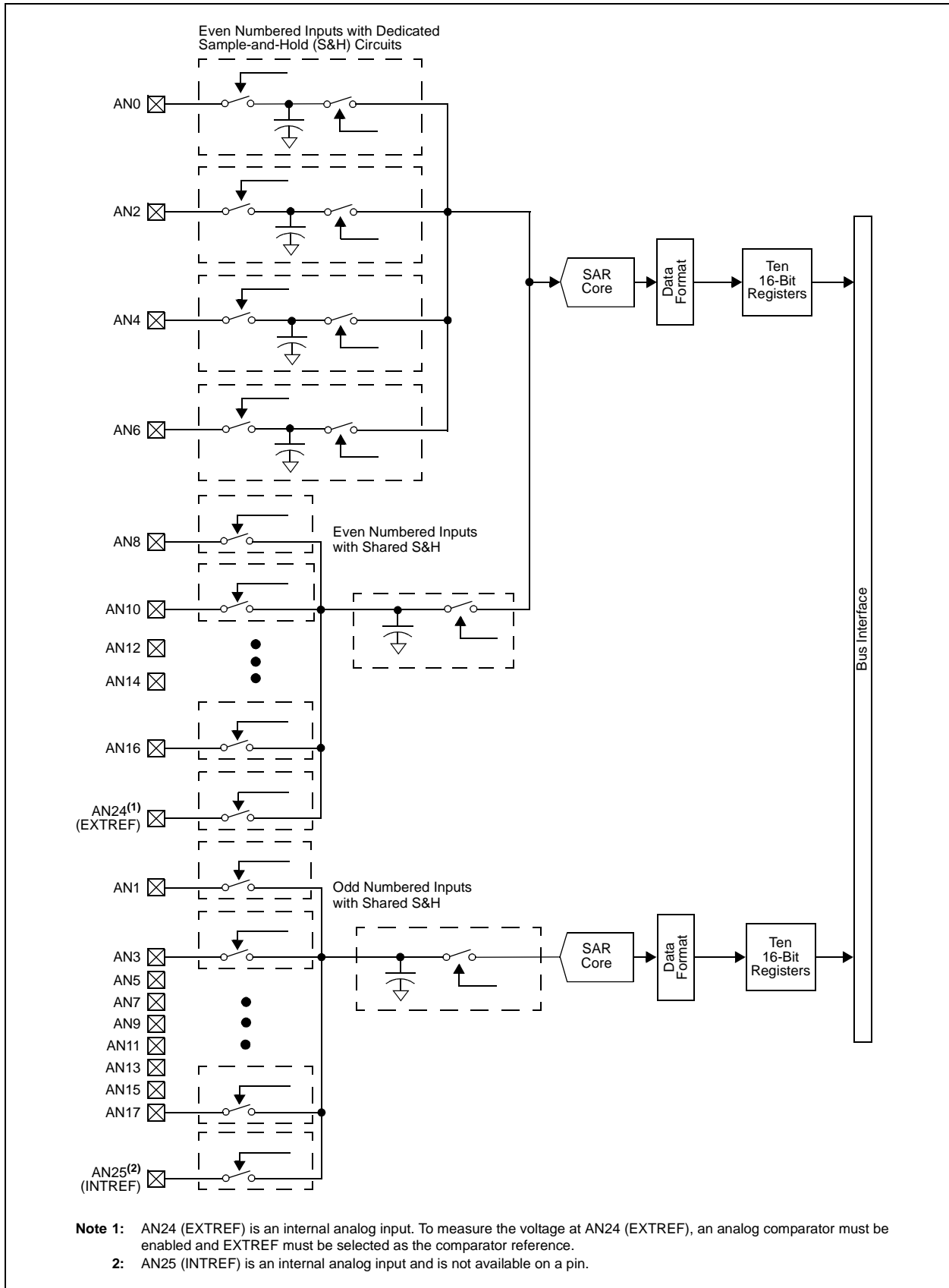
REGISTER 22-4:   ADPCFG: ADC PORT CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<15:8>**(1)**							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<7:0>**(1)**							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PCFG<15:0>:** ADC Port Configuration Control bits**(1)**

   1 = Port pin in Digital mode, port read input is enabled; Analog-to-Digital input multiplexer is connected to AVss
   0 = Port pin in Analog mode, port read input is disabled; Analog-to-Digital samples the pin voltage

Note 1: Not all PCFGx bits are available on all devices. See Figure 22-1, Figure 22-2, Figure 22-3 and Figure 22-4 for the available analog inputs (PCFGx = ANx, where x = 0-15).

REGISTER 22-5:   ADPCFG2: ADC PORT CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<23:16>**(1)**							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'
bit 7-0   **PCFG<23:16>:** ADC Port Configuration Control bits**(1)**

   1 = Port pin in Digital mode, port read input is enabled; Analog-to-Digital input multiplexer is connected to AVss
   0 = Port pin in Analog mode, port read input is disabled; Analog-to-Digital samples the pin voltage

Note 1: Not all PCFGx bits are available on all devices. See Figure 22-1, Figure 22-2, Figure 22-3 and Figure 22-4 for the available analog inputs (PCFGx = ANx, where x can be 0 through 15).

REGISTER 22-8:   ADCPC2: ADC CONVERT PAIR CONTROL REGISTER 2 (CONTINUED)

bit 12-8   **TRGSRC5<4:0>:** Trigger 5 Source Selection bits

Selects trigger source for conversion of Analog Channels AN11 and AN10.

11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

bit 7   **IRQEN4:** Interrupt Request Enable 4 bit

1 = Enables IRQ generation when requested conversion of Channels AN9 and AN8 is completed
0 = IRQ is not generated

bit 6   **PEND4:** Pending Conversion Status 4 bit

1 = Conversion of Channels AN9 and AN8 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5   **SWTRG4:** Software Trigger 4 bit

1 = Starts conversion of AN9 and AN8 (if selected by the TRGSRCx<4:0> bits)[1]
    This bit is automatically cleared by hardware when the PEND4 bit is set.
0 = Conversion has not started

Note 1:   The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.
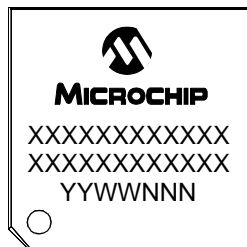
TABLE 27-31: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

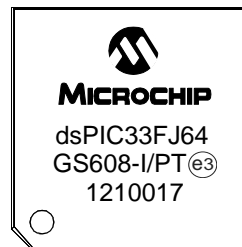| AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ[2]	Max	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	15	MHz	See **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

   2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

   3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

   4: Assumes 50 pF load on all SPIx pins.
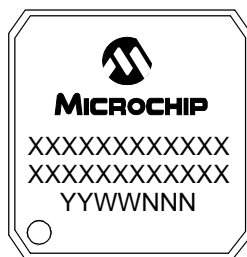
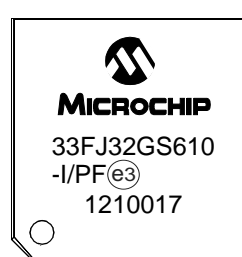## 30.1   Package Marking Information (Continued)

100-Lead TQFP (12x12x1 mm)   Example

```
  ┌─────────────────────┐              ┌─────────────────────┐
  │        (M)          │              │        (M)          │
  │     MICROCHIP       │              │     MICROCHIP       │
  │   XXXXXXXXXXX       │              │   dsPIC33FJ64       │
  │   XXXXXXXXXXX       │              │   GS608-I/PT(e3)    │
  │      YYWWNNN        │              │     1210017         │
  │  ○                  │              │  ○                  │
  └─────────────────────┘              └─────────────────────┘
```

100-Lead TQFP (14x14x1mm)   Example

```
  ┌─────────────────────┐              ┌─────────────────────┐
  │        (M)          │              │        (M)          │
  │     MICROCHIP       │              │     MICROCHIP       │
  │   XXXXXXXXXXX       │              │   33FJ32GS610       │
  │   XXXXXXXXXXX       │              │   -I/PF(e3)         │
  │      YYWWNNN        │              │     1210017         │
  │  ○                  │              │  ○                  │
  └─────────────────────┘              └─────────────────────┘
```

80-Lead Plastic Thin Quad Flatpack (PT) - 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN
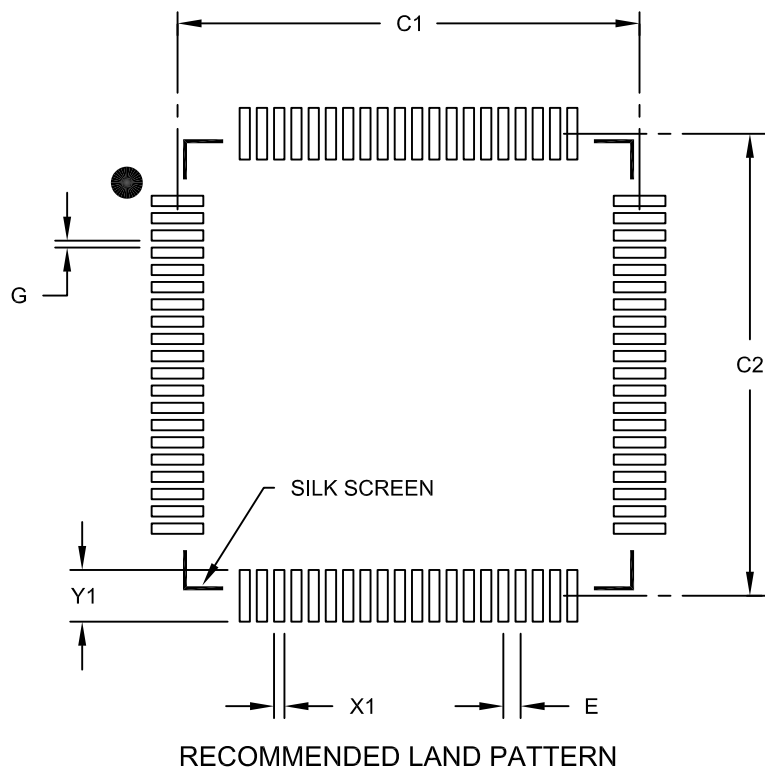
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092B