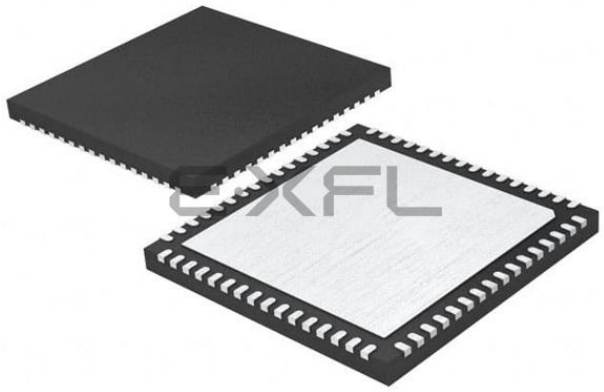
Microchip Technology - DSPIC33FJ64GS406-50I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, QEI, POR, PWM, WDT
Number of I/O	58
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs406-50i-mr

FIGURE 2-6: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

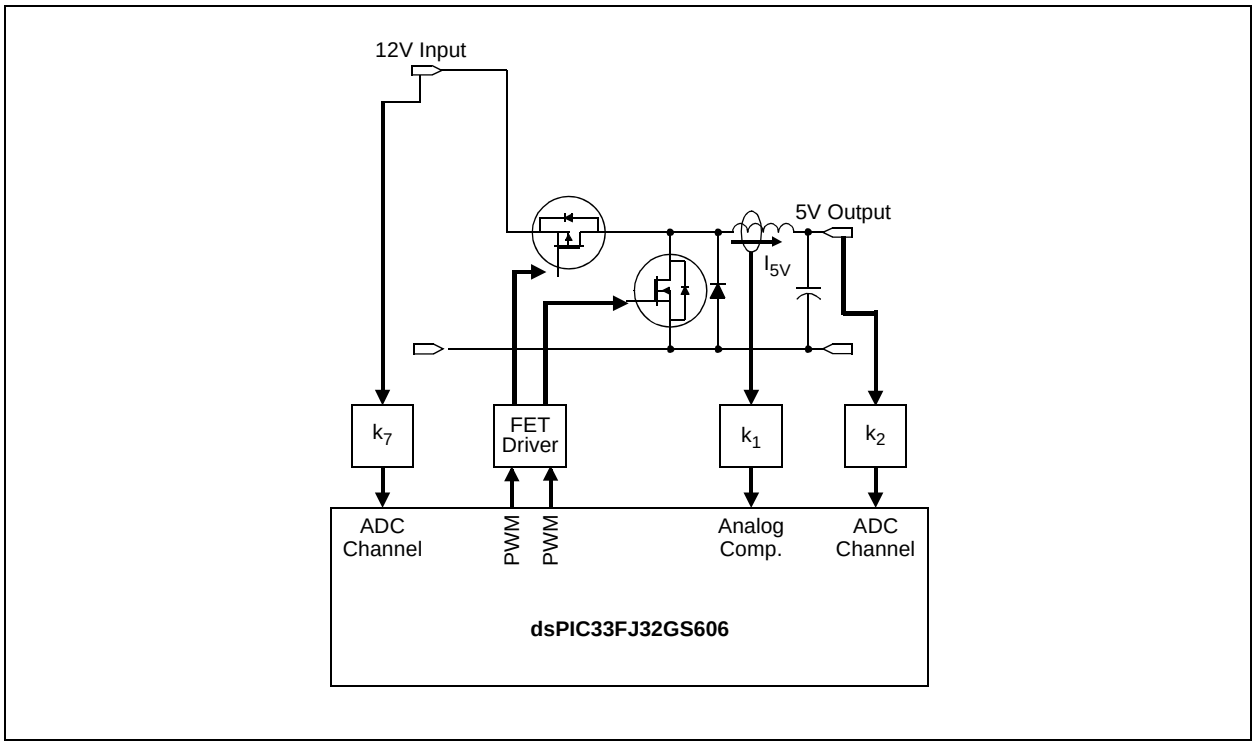


FIGURE 2-7: MULTIPHASE SYNCHRONOUS BUCK CONVERTER

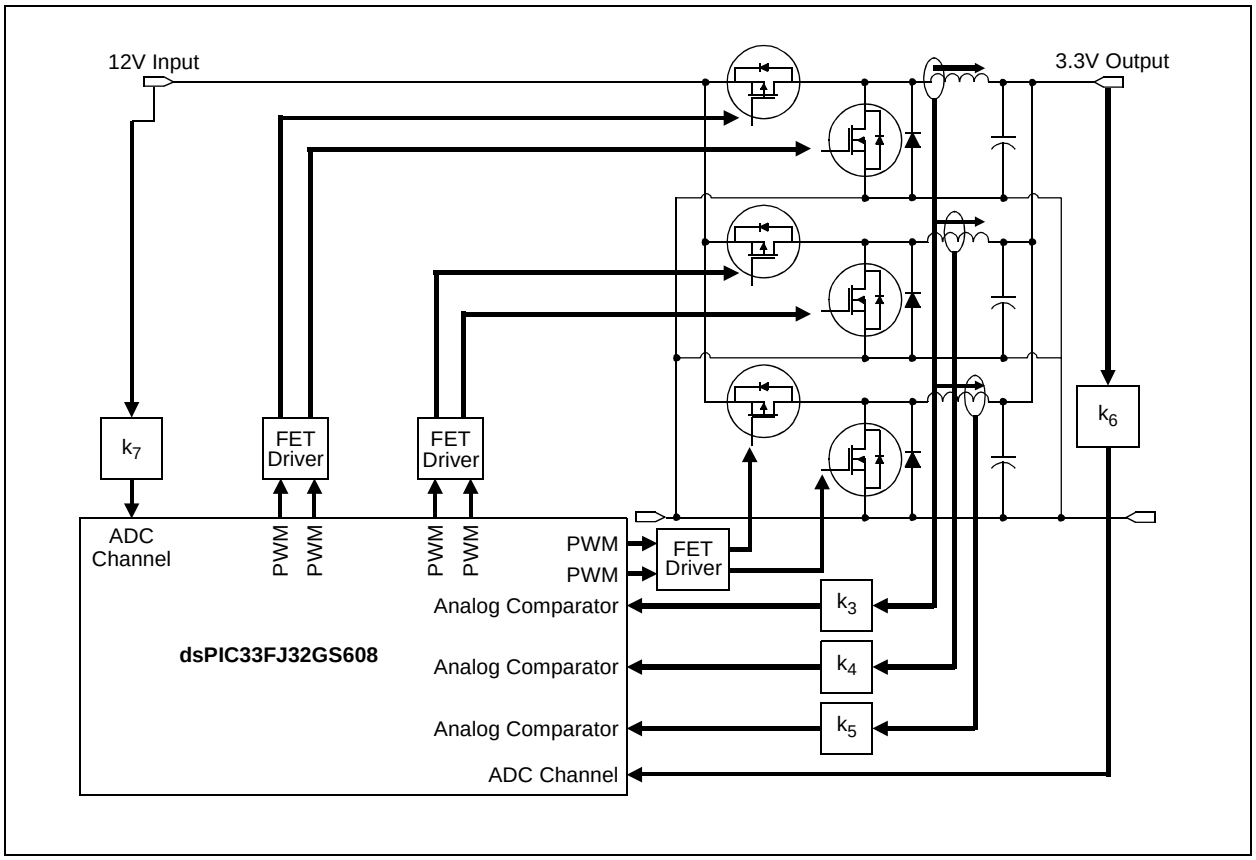


TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ64GS606 DEVICES (CONTINUED)

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC21	00CE	—	—	—	—	—	—	—	—	—	ADCP12IP2	ADCP12IP1	ADCP12IP0	—	—	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC24	00D4	—	PWM6IP2	PWM6IP1	PWM6IP0	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	4444
IPC25	00D6	—	AC2IP2	AC2IP1	AC2IP0	—	PWM9IP2	PWM9IP1	PWM9IP0	—	PWM8IP2	PWM8IP1	PWM8IP0	—	PWM7IP2	PWM7IP1	PWM7IP0	4000
IPC26	00D8	—	—	—	—	—	—	—	—	—	AC4IP2	AC4IP1	AC4IP0	—	AC3IP2	AC3IP1	AC3IP0	0044
IPC27	00DA	—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0	—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	ADCP5IP2	ADCP5IP1	ADCP5IP0	—	ADCP4IP2	ADCP4IP1	ADCP4IP0	—	ADCP3IP2	ADCP3IP1	ADCP3IP0	—	ADCP2IP2	ADCP2IP1	ADCP2IP0	4444
IPC29	00DE	—	—	—	—	—	—	—	—	—	ADCP7IP2	ADCP7IP1	ADCP7IP0	—	ADCP6IP2	ADCP6IP1	ADCP6IP0	0004
INTTREG	00E0	—	—	—	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: HIGH-SPEED PWM GENERATOR 2 REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0440	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON2	0442	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON2	0444	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC2	0446	PDC2<15:0>																0000
PHASE2	0448	PHASE2<15:0>																0000
DTR2	044A	—	—	DTR2<13:0>														0000
ALTDTR2	044C	—	—	ALTDTR2<13:0>														0000
SDC2	044E	SDC2<15:0>																0000
SPHASE2	0450	SPHASE2<15:0>																0000
TRIG2	0452	TRGCMP<12:0>													—	—	—	0000
TRGCON2	0454	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG2	0456	STRGCMP<12:0>													—	—	—	0000
PWMCAP2	0458	PWMCAP<12:0>													—	—	—	0000
LEBCON2	045A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY2	045C	—	—	—	—	LEB<8:0>									—	—	—	0000
AUXCON2	045E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 (CONTINUED)

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11EID	066E	EID<15:0>																xxxx
C1RXF12SID	0670	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF12EID	0672	EID<15:0>																xxxx
C1RXF13SID	0674	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF13EID	0676	EID<15:0>																xxxx
C1RXF14SID	0678	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF14EID	067A	EID<15:0>																xxxx
C1RXF15SID	067C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF15EID	067E	EID<15:0>																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: ANALOG COMPARATOR CONTROL REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	0540	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	0542	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON2	0544	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	0546	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON3	0548	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC3	054A	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON4	054C	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC4	054E	—	—	—	—	—	—	CMREF<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-12: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADCP7IF	ADCP6IF	ADCP5IF	ADCP4IF	ADCP3IF	ADCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **ADCP7IF:** ADC Pair 7 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **ADCP6IF:** ADC Pair 6 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **ADCP5IF:** ADC Pair 5 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **ADCP4IF:** ADC Pair 4 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **ADCP3IF:** ADC Pair 3 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **ADCP2IF:** ADC Pair 2 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

9.1 CPU Clocking System

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices provide six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS, or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator
- FRC Oscillator with Postscaler
- Secondary (LP) Oscillator

9.1.1 SYSTEM CLOCK SOURCES

The Fast RC (FRC) internal oscillator runs at a nominal frequency of 7.37 MHz. User software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

The primary oscillator can use one of the following as its clock source:

- XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins
- HS (High-Speed Crystal): Crystals in the range of 10 MHz to 50 MHz. The crystal is connected to the OSC1 and OSC2 pins
- EC (External Clock): The external clock signal is directly applied to the OSC1 pin

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The LPRC internal oscillator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 9.1.3 “PLL Configuration”**.

The FRC frequency depends on the FRC accuracy (see Table 27-20) and the value of the FRC Oscillator Tuning register (see Register 9-4).

9.1.2 SYSTEM CLOCK SELECTION

The oscillator source used at a device Power-on Reset event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 24.1 “Configuration Bits”** for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose among 12 different clock modes, shown in Table 9-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected), FOSC, is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device and speeds up to 50 MIPS are supported by the device architecture.

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$FCY = FOSC/2$$

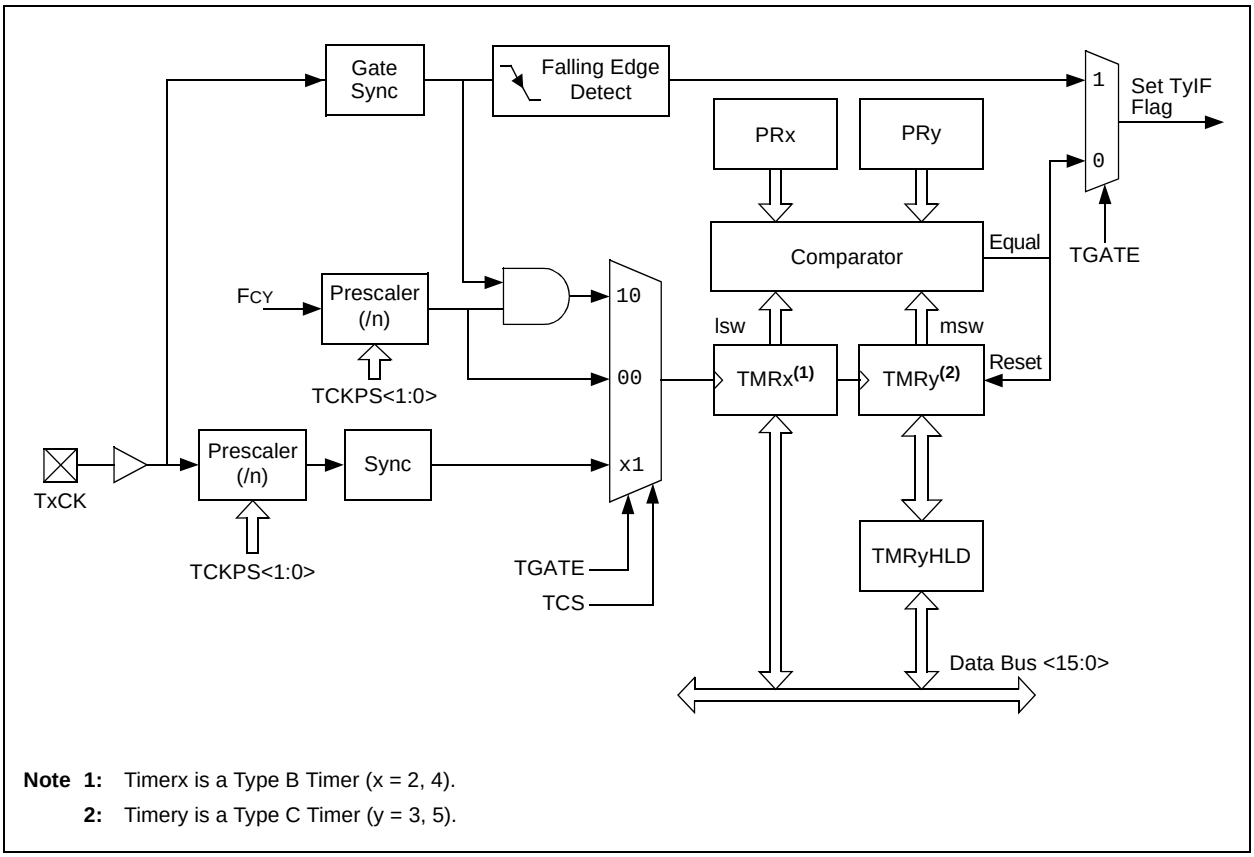
TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Secondary Oscillator (SOSC)	Secondary	xx	100	—
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	—
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	—
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	—
Primary Oscillator (XT)	Primary	01	010	—
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator with PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

FIGURE 13-3: 32-BIT TIMER BLOCK DIAGRAM



Note 1: Timerx is a Type B Timer (x = 2, 4).

2: Timery is a Type C Timer (y = 3, 5).

REGISTER 16-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
SEVTCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **SEVTCMP<12:0>:** Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

REGISTER 16-26: PWMCAPx: PRIMARY PWM TIME BASE CAPTURE x REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWMCAP<12:5>(1,2,3,4)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	U-0	U-0	U-0
PWMCAP<4:0>(1,2,3,4)					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **PWMCAP<12:0>:** Captured PWM Time Base Value bits(1,2,3,4)
The value in this register represents the captured PWM time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The capture feature is only available on the primary output (PWMxH).
2: This feature is active only after LEB processing on the current-limit input signal is complete.
3: The minimum capture resolution is 8.32 ns.
4: This feature can be used when the XPRES bit (PWMCONx<1>) is set to '0'.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware clears at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C. Hardware clears at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware clears at the end of the master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware clears at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware clears at the end of the master Start sequence.
0 = Start condition is not in progress

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bits

11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bits (same values as bits<15:14>)

REGISTER 22-8: ADCPC2: ADC CONVERT PAIR CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN5:** Interrupt Request Enable 5 bit
1 = Enables IRQ generation when requested conversion of Channels AN11 and AN10 is completed
0 = IRQ is not generated

bit 14 **PEND5:** Pending Conversion Status 5 bit
1 = Conversion of Channels AN11 and AN10 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG5:** Software Trigger 5 bit
1 = Starts conversion of AN11 and AN10 (if selected by the TRGSRCx<4:0> bits)**(1)**
This bit is automatically cleared by hardware when the PEND5 bit is set.
0 = Conversion has not started

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

REGISTER 22-9: ADCPC3: ADC CONVERT PAIR CONTROL REGISTER 3 (CONTINUED)

bit 4-0 **TRGSRC6<4:0>:** Trigger 6 Source Selection bits
Selects trigger source for conversion of Analog Channels AN13 and AN12.
11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

TABLE 24-2: dsPIC33F CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection bit 1 = Boot segment can be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits X11 = No boot program Flash segment Boot Space is 256 Instruction Words (except interrupt vectors): 110 = Standard security; boot program Flash segment ends at 0x0003FE 010 = High security; boot program Flash segment ends at 0x0003FE Boot Space is 768 Instruction Words (except interrupt vectors): 101 = Standard security; boot program Flash segment ends at 0x0007FE 001 = High security; boot program Flash segment ends at 0x0007FE Boot Space is 1792 Instruction Words (except interrupt vectors): 100 = Standard security; boot program Flash segment ends at 0x000FFE 000 = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bits 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-Speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user selected oscillator source when ready 0 = Start-up device with user selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Secondary (LP) Oscillator 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode

26.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

26.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

27.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(3) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 3.0V$(3) ..... -0.3V to (V_{DD} + 0.3V)
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin(2) ..... 250 mA
Maximum current sourced/sunk by any 4x I/O pin ..... 15 mA
Maximum current sourced/sunk by any 8x I/O pin ..... 25 mA
Maximum current sourced/sunk by any 16x I/O pin ..... 45 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(2) 200mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of the device maximum power dissipation (see Table 27-2).

3: See the **“Pin Diagrams”** section for 5V tolerant pins.

27.1 DC Characteristics

TABLE 27-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610
—	3.0-3.6V(1)	-40°C to +85°C	40
—	3.0-3.6V(1)	-40°C to +125°C	40

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN. See Parameter BO10 in Table 27-11 for the BOR values.

TABLE 27-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 27-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm)	θJA	39	—	°C/W	**1**
Package Thermal Resistance, 80-Pin TQFP (12x12x1 mm)	θJA	53.1	—	°C/W	**1**
Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm)	θJA	43	—	°C/W	**1**
Package Thermal Resistance, 100-Pin TQFP (14x14x1 mm)	θJA	43	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 27-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(2)						
DC20d	21	30	mA	-40°C	3.3V	10 MIPS (See **Note 2**)
DC20a	21	30	mA	+25°C		
DC20b	21	30	mA	+85°C		
DC20c	22	30	mA	+125°C		
DC21d	28	40	mA	-40°C	3.3V	16 MIPS (See **Notes 2** and **3**)
DC21a	28	40	mA	+25°C		
DC21b	28	40	mA	+85°C		
DC21c	29	40	mA	+125°C		
DC22d	35	45	mA	-40°C	3.3V	20 MIPS (See **Notes 2** and **3**)
DC22a	35	45	mA	+25°C		
DC22b	35	45	mA	+85°C		
DC22c	36	45	mA	+125°C		
DC23d	49	60	mA	-40°C	3.3V	30 MIPS (See **Notes 2** and **3**)
DC23a	49	60	mA	+25°C		
DC23b	49	60	mA	+85°C		
DC23c	50	60	mA	+125°C		
DC24d	66	75	mA	-40°C	3.3V	40 MIPS (See **Note 2**)
DC24a	66	75	mA	+25°C		
DC24b	66	75	mA	+85°C		
DC24c	67	75	mA	+125°C		
DC25d	153	170	mA	-40°C	3.3V	40 MIPS (See **Notes 2** and **3**), except PWM is operating at maximum speed (PTCON2 = 0x0000)
DC25a	154	170	mA	+25°C		
DC25b	155	170	mA	+85°C		
DC25c	156	170	mA	+125°C		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are all '0's)
- CPU executing `while(1)` statement
- JTAG disabled

3: These parameters are characterized but not tested in manufacturing.

TABLE 27-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off, Clock On Base Current(2)						
DC40d	8	15	mA	-40°C	3.3V	10 MIPS
DC40a	9	15	mA	+25°C		
DC40b	9	15	mA	+85°C		
DC40c	10	15	mA	+125°C		
DC41d	11	20	mA	-40°C	3.3V	16 MIPS(3)
DC41a	11	20	mA	+25°C		
DC41b	11	20	mA	+85°C		
DC41c	12	20	mA	+125°C		
DC42d	14	25	mA	-40°C	3.3V	20 MIPS(3)
DC42a	14	25	mA	+25°C		
DC42b	14	25	mA	+85°C		
DC42c	15	25	mA	+125°C		
DC43d	20	30	mA	-40°C	3.3V	30 MIPS(3)
DC43a	20	30	mA	+25°C		
DC43b	21	30	mA	+85°C		
DC43c	22	30	mA	+125°C		
DC44d	29	40	mA	-40°C	3.3V	40 MIPS
DC44a	29	40	mA	+25°C		
DC44b	30	40	mA	+85°C		
DC44c	31	40	mA	+125°C		

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are all ‘0’s)
- JTAG is disabled

3: These parameters are characterized but not tested in manufacturing.

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