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Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 50 MIPS |
| Connectivity | I ² C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, QEI, POR, PWM, WDT |
| Number of I/O | 58 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs406t-50i-mr |

■ = Pins are up to 5V tolerant

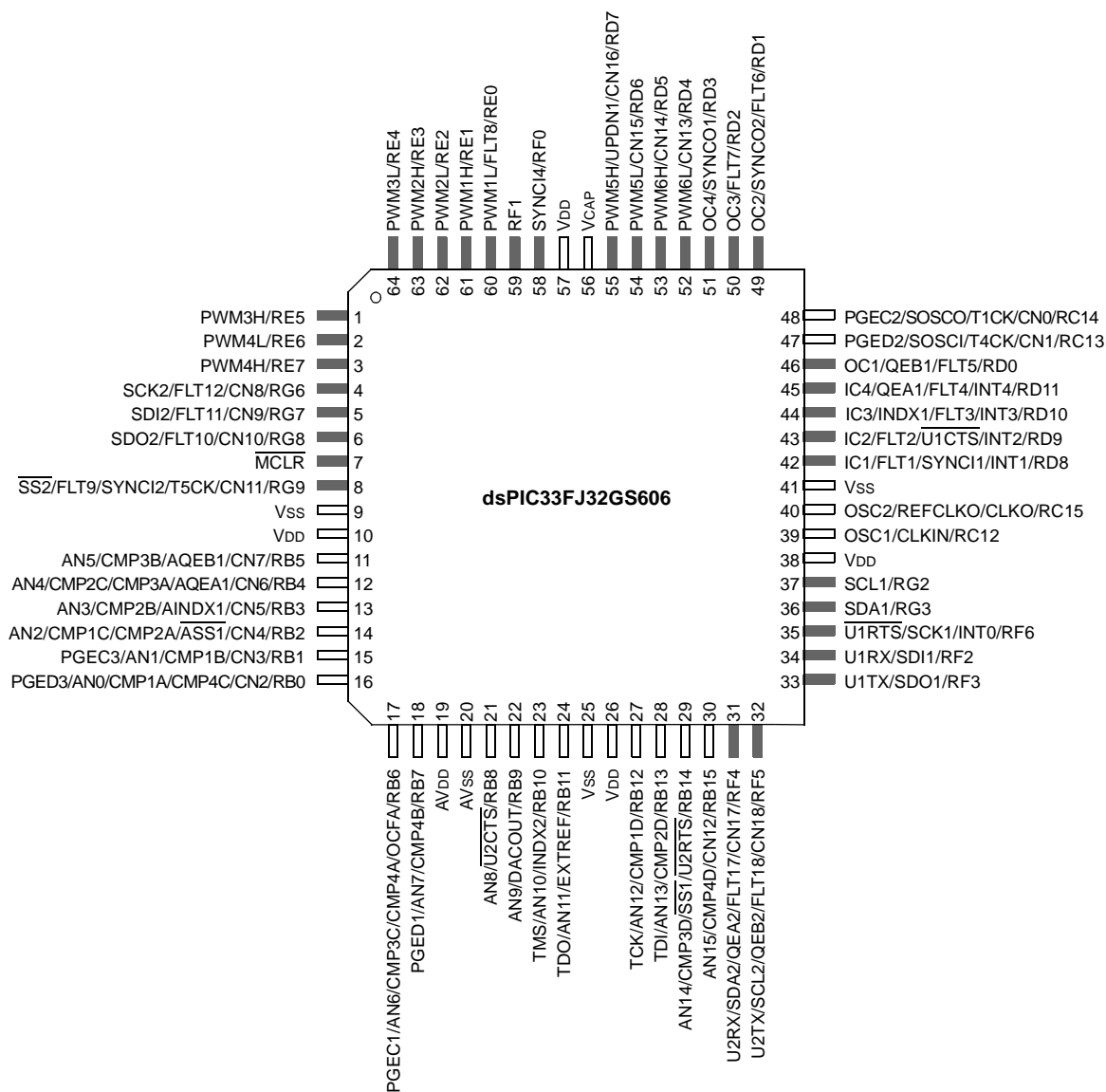
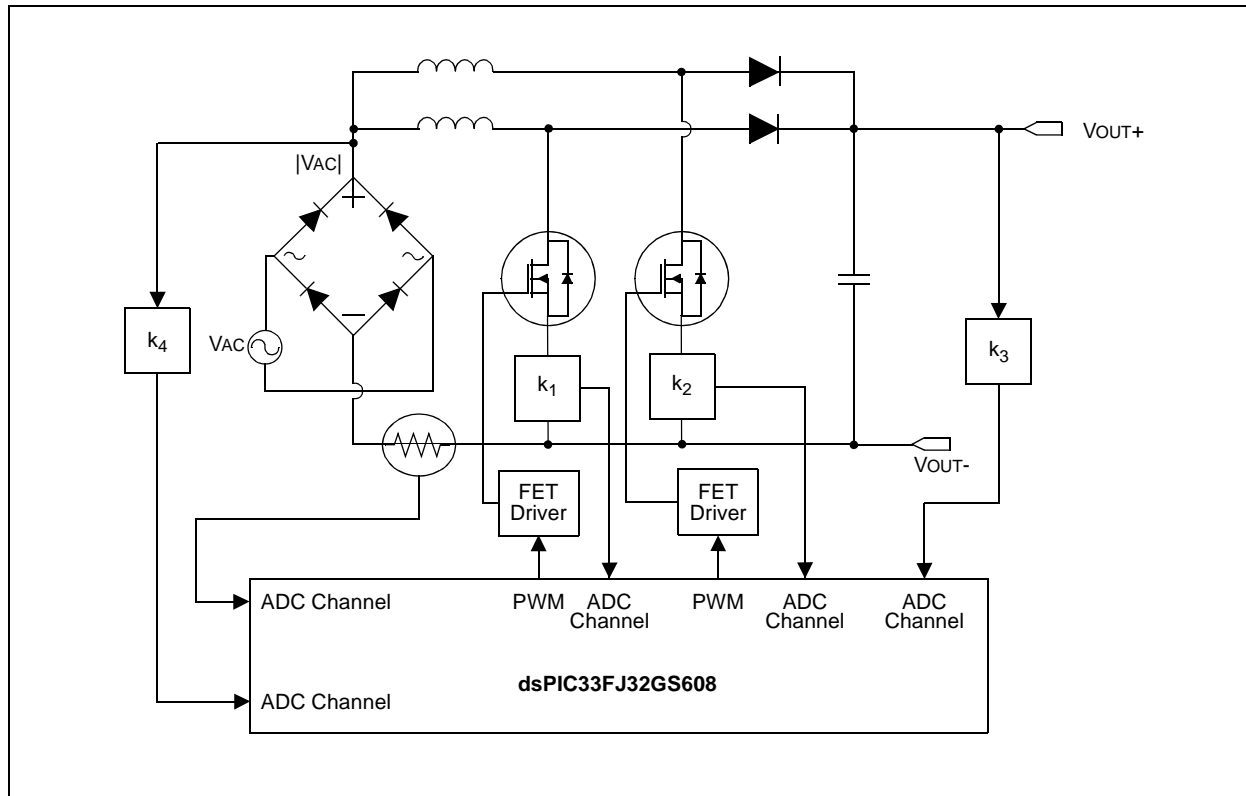


FIGURE 2-9: INTERLEAVED PFC



4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *dsPIC33/PIC24 Family Reference Manual, Program Memory* (DS70203), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access to program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory maps are shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY MAPS FOR dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 DEVICES

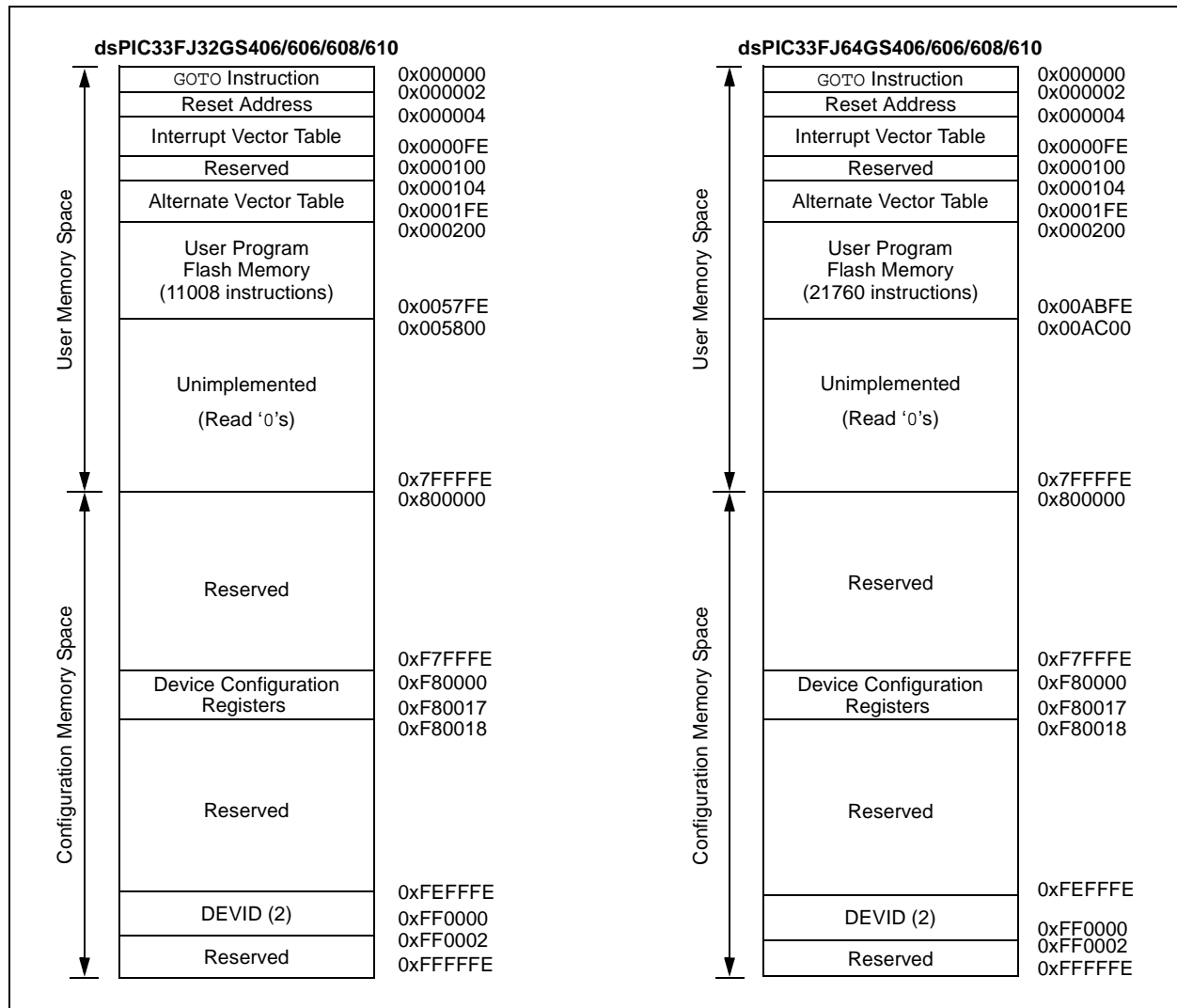


TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ64GS610 DEVICES (CONTINUED)

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|----------|--------|-----------|-----------|-----------|--------|----------|----------|----------|-------|-----------|-----------|-----------|---------|-----------|-----------|-----------|------------|
| IPC14 | 00C0 | — | — | — | — | — | QE11IP2 | QE11IP1 | QE11IP0 | — | PSEMIP2 | PSEMIP1 | PSEMIP0 | — | — | — | — | 0440 |
| IPC16 | 00C4 | — | — | — | — | — | U2EIP2 | U2EIP1 | U2EIP0 | — | U1EIP2 | U1EIP1 | U1EIP0 | — | — | — | — | 0440 |
| IPC17 | 00C6 | — | — | — | — | — | C1TXIP2 | C1TXIP1 | C1TXIP0 | — | — | — | — | — | — | — | — | 0400 |
| IPC18 | 00C8 | — | QE12IP2 | QE12IP1 | QE12IP0 | — | — | — | — | — | PSESMIP2 | PSESMIP1 | PSESMIP0 | — | — | — | — | 4040 |
| IPC20 | 00CC | — | ADCP10IP2 | ADCP10IP1 | ADCP10IP0 | — | ADCP9IP2 | ADCP9IP1 | ADCP9IP0 | — | ADCP8IP2 | ADCP8IP1 | ADCP8IP0 | — | — | — | — | 4440 |
| IPC21 | 00CE | — | — | — | — | — | — | — | — | — | ADCP12IP2 | ADCP12IP1 | ADCP12IP0 | — | ADCP11IP2 | ADCP11IP1 | ADCP11IP0 | 0044 |
| IPC23 | 00D2 | — | PWM2IP2 | PWM2IP1 | PWM2IP0 | — | PWM1IP2 | PWM1IP1 | PWM1IP0 | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 00D4 | — | PWM6IP2 | PWM6IP1 | PWM6IP0 | — | PWM5IP2 | PWM5IP1 | PWM5IP0 | — | PWM4IP2 | PWM4IP1 | PWM4IP0 | — | PWM3IP2 | PWM3IP1 | PWM3IP0 | 4444 |
| IPC25 | 00D6 | — | AC2IP2 | AC2IP1 | AC2IP0 | — | PWM9IP2 | PWM9IP1 | PWM9IP0 | — | PWM8IP2 | PWM8IP1 | PWM8IP0 | — | PWM7IP2 | PWM7IP1 | PWM7IP0 | 4444 |
| IPC26 | 00D8 | — | — | — | — | — | — | — | — | — | AC4IP2 | AC4IP1 | AC4IP0 | — | AC3IP2 | AC3IP1 | AC3IP0 | 0044 |
| IPC27 | 00DA | — | ADCP11IP2 | ADCP11IP1 | ADCP11IP0 | — | ADCP0IP2 | ADCP0IP1 | ADCP0IP0 | — | — | — | — | — | — | — | — | 4400 |
| IPC28 | 00DC | — | ADCP5IP2 | ADCP5IP1 | ADCP5IP0 | — | ADCP4IP2 | ADCP4IP1 | ADCP4IP0 | — | ADCP3IP2 | ADCP3IP1 | ADCP3IP0 | — | ADCP2IP2 | ADCP2IP1 | ADCP2IP0 | 4444 |
| IPC29 | 00DE | — | — | — | — | — | — | — | — | — | ADCP7IP2 | ADCP7IP1 | ADCP7IP0 | — | ADCP6IP2 | ADCP6IP1 | ADCP6IP0 | 0044 |
| INTTREG | 00E0 | — | — | — | — | ILR3 | ILR2 | ILR1 | ILR0 | — | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 | 0000 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-57: SYSTEM CONTROL REGISTER MAP

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|----------|--------|--------|---------|--------|--------|-----------|-----------|-------------|----------|----------|----------|---------|---------|---------|---------|---------|---------------------|
| RCON | 0740 | TRAPR | IOPUWR | — | — | — | — | — | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | xxxx ⁽¹⁾ |
| OSCCON | 0742 | — | COSC2 | COSC1 | COSC0 | — | NOSC2 | NOSC1 | NOSC0 | CLKLOCK | — | LOCK | — | CF | — | — | OSWEN | 0300 ⁽²⁾ |
| CLKDIV | 0744 | ROI | DOZE2 | DOZE1 | DOZE0 | DOZEN | FRCDIV2 | FRCDIV1 | FRCDIV0 | PLLPOST1 | PLLPOST0 | — | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 | 0040 |
| PLLFBD | 0746 | — | — | — | — | — | — | — | PLLDIV<8:0> | | | | | | | | | 0030 |
| OSCTUN | 0748 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |
| REFOCON | 074E | ROON | — | ROSSLP | ROSEL | RODIV3 | RODIV2 | RODIV1 | RODIV0 | — | — | — | — | — | — | — | — | 0000 |
| ACLKCON | 0750 | ENAPLL | APLLCK | SELACLK | — | — | APSTSCLR2 | APSTSCLR1 | APSTSCLR0 | ASRCSEL | FRCSEL | — | — | — | — | — | — | 2300 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The RCON register Reset values are dependent on the type of Reset.

2: The OSCCON register Reset values are dependent on the FOSC_x Configuration bits and on the type of Reset.

TABLE 4-58: NVM REGISTER MAP

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|----------|--------|--------|--------|--------|--------|--------|-------|-------|-------------|-------|-------|-------|--------|--------|--------|--------|---------------------|
| NVMCON | 0760 | WR | WREN | WRERR | — | — | — | — | — | — | ERASE | — | — | NVMOP3 | NVMOP2 | NVMOP1 | NVMOP0 | 0000 ⁽¹⁾ |
| NVMKEY | 0766 | — | — | — | — | — | — | — | — | NVMKEY<7:0> | | | | | | | | 0000 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The Reset value shown is for POR only. The value on other Reset states is dependent on the state of the memory write or erase operations at the time of Reset.

TABLE 4-59: PMD REGISTER MAP FOR dsPIC33FJ64GS610 DEVICES

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|--------|--------|--------|-------|--------|--------|------------|
| PMD1 | 0770 | T5MD | T4MD | T3MD | T2MD | T1MD | QE11MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD | ADCMD | 0000 |
| PMD2 | 0772 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0774 | — | — | — | — | — | CMPMD | — | — | — | — | QE12MD | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0776 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | — | — | — | 0000 |
| PMD6 | 077A | PWM8MD | PWM7MD | PWM6MD | PWM5MD | PWM4MD | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 077C | — | — | — | — | CMP4MD | CMP3MD | CMP2MD | CMP1MD | — | — | — | — | — | — | — | PWM9MD | 0000 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.2.7 SOFTWARE STACK

In addition to its use as a Working register, the W15 register in the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices is also used as a Software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note: A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

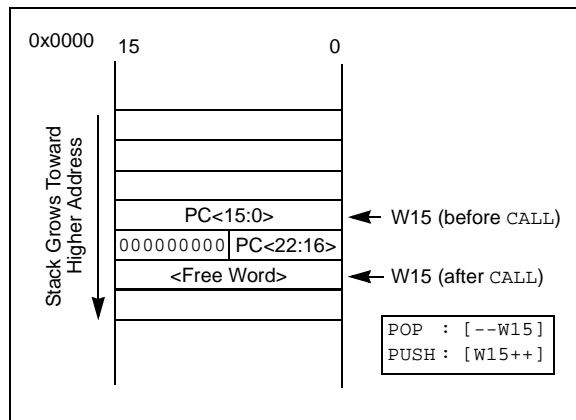
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1800 in RAM, initialize the SPLIM with the value, 0x17FE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: CALL STACK FRAME



4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-66 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a Working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Flash Programming**” (DS70191) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming

pin pairs: PGEC1/PGED1, PGEC2/PGED2 or PGEC3/PGED3), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the Digital Signal Controller (DSC) just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data, either in blocks or ‘rows’ of 64 instructions (192 bytes) at a time, or a single program memory word, and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

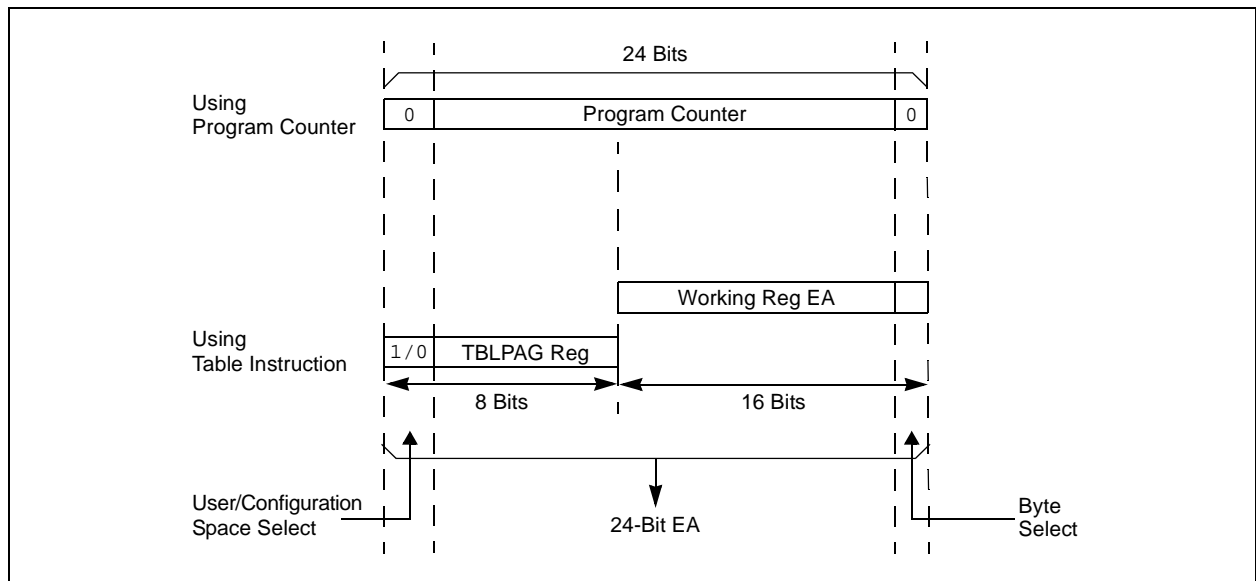
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

| | | | | | | | |
|--------|-----|-------|-------|-----|-------|-----|-------|
| R-0 | R-0 | R/C-0 | R/C-0 | R-0 | R/C-0 | R-0 | R/W-0 |
| OA | OB | SA | SB | OAB | SAB | DA | DC |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------------------|----------------------|----------------------|-----|-------|-------|-------|-------|
| R/W-0 ⁽³⁾ | R/W-0 ⁽³⁾ | R/W-0 ⁽³⁾ | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IPL2 ⁽²⁾ | IPL1 ⁽²⁾ | IPL0 ⁽²⁾ | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| | |
|-------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | '0' = Bit is cleared |
| | x = Bit is unknown |
| | U = Unimplemented bit, read as '0' |

bit 7-5 **IPL<2:0>: CPU Interrupt Priority Level Status bits^(2,3)**

111 = CPU Interrupt Priority Level is 7 (15), user interrupts are disabled
 110 = CPU Interrupt Priority Level is 6 (14)
 101 = CPU Interrupt Priority Level is 5 (13)
 100 = CPU Interrupt Priority Level is 4 (12)
 011 = CPU Interrupt Priority Level is 3 (11)
 010 = CPU Interrupt Priority Level is 2 (10)
 001 = CPU Interrupt Priority Level is 1 (9)
 000 = CPU Interrupt Priority Level is 0 (8)

- Note 1:** For complete register details, see Register 3-1.
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

| | | | | | | | |
|--------|-----|-----|-------|-------|-----|-----|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| — | — | — | US | EDT | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|--------|---------------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R/W-0 | R/W-0 | R/W-0 |
| SATA | SATB | SATDW | ACCSAT | IPL3 ⁽²⁾ | PSV | RND | IF |
| bit 7 | | | | | | | bit 0 |

| | |
|----------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| '0' = Bit is cleared | 'x' = Bit is unknown |
| | -n = Value at POR |
| | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |

bit 3 **IPL3: CPU Interrupt Priority Level Status bit⁽²⁾**

1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

- Note 1:** For complete register details, see Register 3-2.
- 2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-26: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|---------|---------|---------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
| — | — | — | — | — | INT1IP2 | INT1IP1 | INT1IP0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3

Unimplemented: Read as '0'

bit 2-0

INT1IP<2:0>: External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

-
-
-

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

REGISTER 7-35: IPC17: INTERRUPT PRIORITY CONTROL REGISTER 17

| | | | | | | | |
|--------|-----|-----|-----|-----|------------------------|------------------------|------------------------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
| — | — | — | — | — | C1TXIP2 ⁽¹⁾ | C1TXIP1 ⁽¹⁾ | C1TXIP0 ⁽¹⁾ |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **C1TXIP<2:0>:** ECAN1 Transmit Data Request Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

-
-
-

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Interrupts are disabled on devices without ECAN™ modules.

15.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OCxCON<2:0>) register. Table 15-1 lists the different bit settings for the Output Compare modes. Figure 15-2 illustrates the output compare operation for various modes. The user

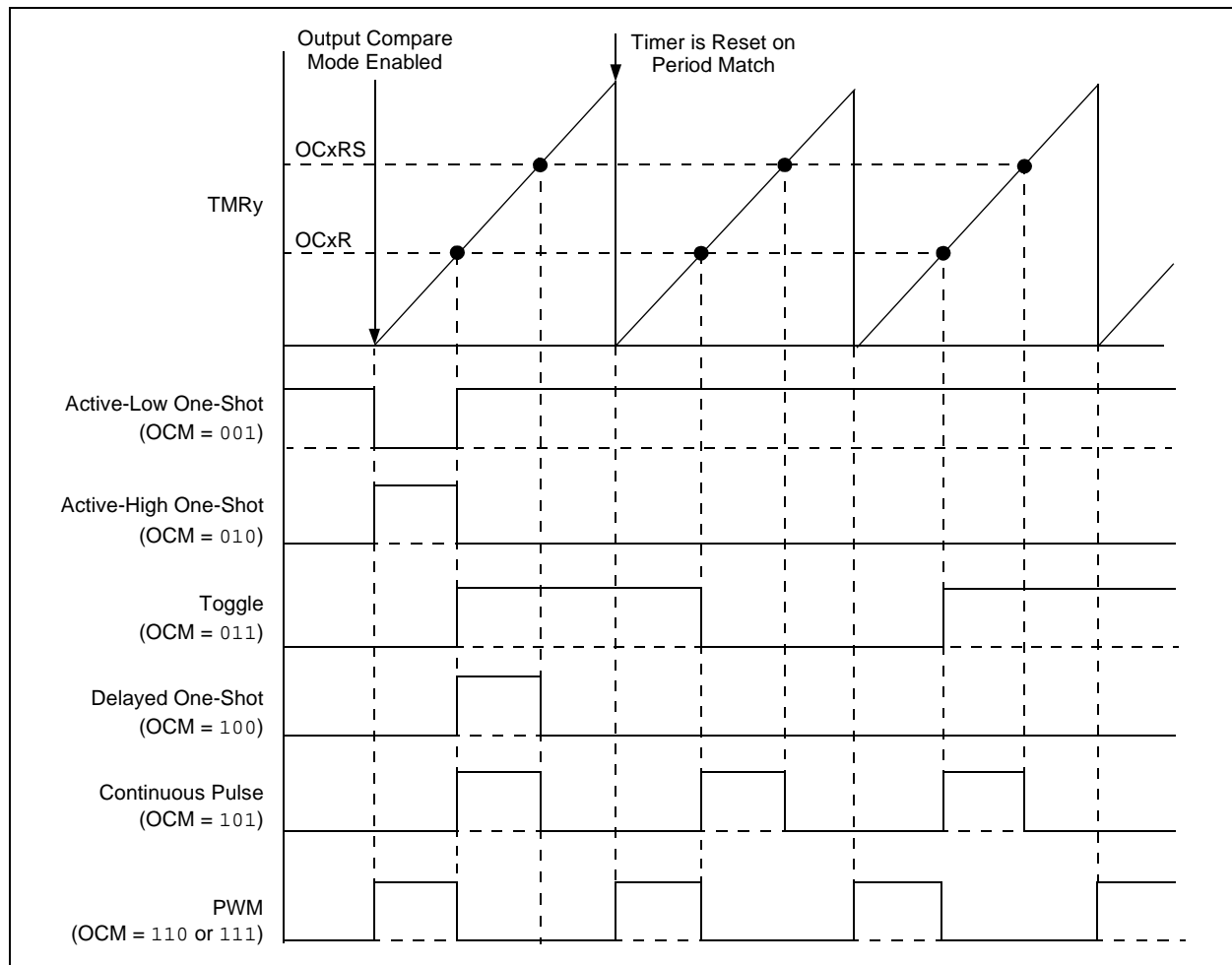
application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

Note: See “Output Compare” (DS70005157) in the “dsPIC33/PIC24 Family Reference Manual” for OCxR and OCxRS register restrictions.

TABLE 15-1: OUTPUT COMPARE MODES

| OCM<2:0> | Mode | OCx Pin Initial State | OCx Interrupt Generation |
|----------|------------------------------|---|----------------------------------|
| 000 | Module Disabled | Controlled by GPIO register | — |
| 001 | Active-Low One-Shot | 0 | OCx rising edge |
| 010 | Active-High One-Shot | 1 | OCx falling edge |
| 011 | Toggle | Current output is maintained | OCx rising and falling edge |
| 100 | Delayed One-Shot | 0 | OCx falling edge |
| 101 | Continuous Pulse | 0 | OCx falling edge |
| 110 | PWM without Fault Protection | ‘0’ if OCxR is zero, ‘1’ if OCxR is non-zero | No interrupt |
| 111 | PWM with Fault Protection | ‘0’ if OCxR is zero, ‘1’ if OCxR is non-zero | OCFA falling edge for OC1 to OC4 |

FIGURE 15-2: OUTPUT COMPARE x OPERATION



REGISTER 16-11: PWMCONx: PWM CONTROL x REGISTER (CONTINUED)

- bit 7-6 **DTC<1:0>**: Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all output modes
- bit 5 **DTCP**: Dead-Time Compensation Polarity bit⁽⁴⁾
1 = If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened;
 If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened
0 = If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened;
 If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **MTBS**: Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and the clock source for the PWM generation logic
- bit 2 **CAM**: Center-Aligned Mode Enable bit^(2,3,5)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled
- bit 1 **XPRES**: External PWM Reset Control bit⁽⁶⁾
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base
- bit 0 **IUE**: Immediate Update Enable bit
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active PDCx registers are synchronized to the PWM time base

- Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
- 2:** The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 3:** These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.
- 4:** For DTCP to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.
- 5:** Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
- 6:** Configure CLMOD (FCLCONX<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **EID<15:0>**: Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| F7MSK1 | F7MSK0 | F6MSK1 | F6MSK0 | F5MSK1 | F5MSK0 | F4MSK1 | F4MSK0 |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| F3MSK1 | F3MSK0 | F2MSK1 | F2MSK0 | F1MSK1 | F1MSK0 | F0MSK1 | F0MSK0 |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **F7MSK<1:0>**: Mask Source for Filter 7 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>**: Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10 **F5MSK<1:0>**: Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8 **F4MSK<1:0>**: Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6 **F3MSK<1:0>**: Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4 **F2MSK<1:0>**: Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2 **F1MSK<1:0>**: Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0 **F0MSK<1:0>**: Mask Source for Filter 0 bits (same values as bits<15:14>)

REGISTER 22-1: ADCON: ADC CONTROL REGISTER (CONTINUED)

- bit 4 **ASYNCSAMP:** Asynchronous Dedicated S&H Sampling Enable bit⁽¹⁾
1 = The dedicated S&H is constantly sampling and then terminates sampling as soon as the trigger pulse is detected
0 = The dedicated S&H starts sampling when the trigger event is detected and completes the sampling process in two ADC clock cycles
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **ADCS<2:0>:** Analog-to-Digital Conversion Clock Divider Select bits⁽¹⁾
111 = FADC/8
110 = FADC/7
101 = FADC/6
100 = FADC/5
011 = FADC/4 (default)
010 = FADC/3
001 = FADC/2
000 = FADC/1

- Note 1:** This control bit can only be changed while the ADC is disabled (ADON = 0).
2: This control bit is only active on devices that have one SAR.

REGISTER 22-7: ADCPC1: ADC CONVERT PAIR CONTROL REGISTER 1

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|-------|--------|----------|----------|----------|----------|----------|
| IRQEN3 | PEND3 | SWTRG3 | TRGSRC34 | TRGSRC33 | TRGSRC32 | TRGSRC31 | TRGSRC30 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|-------|--------|----------|----------|----------|----------|----------|
| IRQEN2 | PEND2 | SWTRG2 | TRGSRC24 | TRGSRC23 | TRGSRC22 | TRGSRC21 | TRGSRC20 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **IRQEN3:** Interrupt Request Enable 3 bit
 1 = Enables IRQ generation when requested conversion of Channels AN7 and AN6 is completed
 0 = IRQ is not generated
- bit 14 **PEND3:** Pending Conversion Status 3 bit
 1 = Conversion of Channels AN7 and AN6 is pending; set when selected trigger is asserted
 0 = Conversion is complete
- bit 13 **SWTRG3:** Software Trigger 3 bit
 1 = Starts conversion of AN7 and AN6 (if selected by the TRGSRCx<4:0> bits)⁽¹⁾
 This bit is automatically cleared by hardware when the PEND3 bit is set.
 0 = Conversion has not started

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

REGISTER 22-12: ADCPC6: ADC CONVERT PAIR CONTROL REGISTER 6⁽²⁾ (CONTINUED)

bit 4-0

TRGSRC12<4:0>: Trigger 12 Source Selection bits

Selects trigger source for conversion of analog channels AN25 and AN24.

11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

- Note 1:** The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.
- 2:** This register is not available on dsPIC33FJ32GS406 and dsPIC33FJ64GS406 devices.

23.3 Module Applications

This module provides a means for the SMPS dsPIC® DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 10-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample-and-Convert Process
- Truncate the PWM Signal (current limit)
- Truncate the PWM Period (current minimum)
- Disable the PWM Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) generate an interrupt, 2) have the ADC take a sample and convert it, and 3) truncate the PWM output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

23.4 DAC

The range of the DAC is controlled via an analog multiplexer that selects either $AV_{DD}/2$, an internal reference source, INTREF, or an external reference source, EXTREF. The full range of the DAC ($AV_{DD}/2$) will typically be used when the chosen input source pin is shared with the ADC. The reduced range option (INTREF) will likely be used when monitoring current levels using a current sense resistor. Usually, the measured voltages in such applications are small ($<1.25V$); therefore the option of using a reduced reference range for the comparator extends the available DAC resolution in these applications. The use of an external reference enables the user to connect to a reference that better suits their application.

DACOUT, shown in Figure 23-1, can only be associated with a single comparator at a given time.

Note: It should be ensured in software that multiple DACOE bits are not set. The output on the DACOUT pin will be indeterminate if multiple comparators enable the DAC output.

23.5 Interaction with I/O Buffers

If the comparator module is enabled and a pin has been selected as the source for the comparator, then the chosen I/O pad must disable the digital input buffer associated with the pad to prevent excessive currents in the digital buffer due to analog input voltages.

23.6 Digital Logic

The CMPCONx register (see Register 23-1) provides the control logic that configures the comparator module. The digital logic provides a glitch filter for the comparator output to mask transient signals in less than two instruction cycles. In Sleep or Idle mode, the glitch filter is bypassed to enable an asynchronous path from the comparator to the interrupt controller. This asynchronous path can be used to wake-up the processor from Sleep or Idle mode.

The comparator can be disabled while in Idle mode if the CMPSIDL bit is set. If a device has multiple comparators, if any CMPSIDL bit is set, then the entire group of comparators will be disabled while in Idle mode. This behavior reduces complexity in the design of the clock control logic for this module.

The digital logic also provides a one T_{CY} width pulse generator for triggering the ADC and generating interrupt requests.

The CMPDACx (see Register 23-2) register provides the digital input value to the reference DAC.

If the module is disabled, the DAC and comparator are disabled to reduce power consumption.

23.7 Comparator Input Range

The comparator has a limitation for the input Common-Mode Range (CMR) of $(AV_{DD} - 1.5V)$, typical. This means that both inputs should not exceed this range. As long as one of the inputs is within the Common-Mode Range, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated.

If both inputs exceed the CMR, the comparator output will be indeterminate.

23.8 DAC Output Range

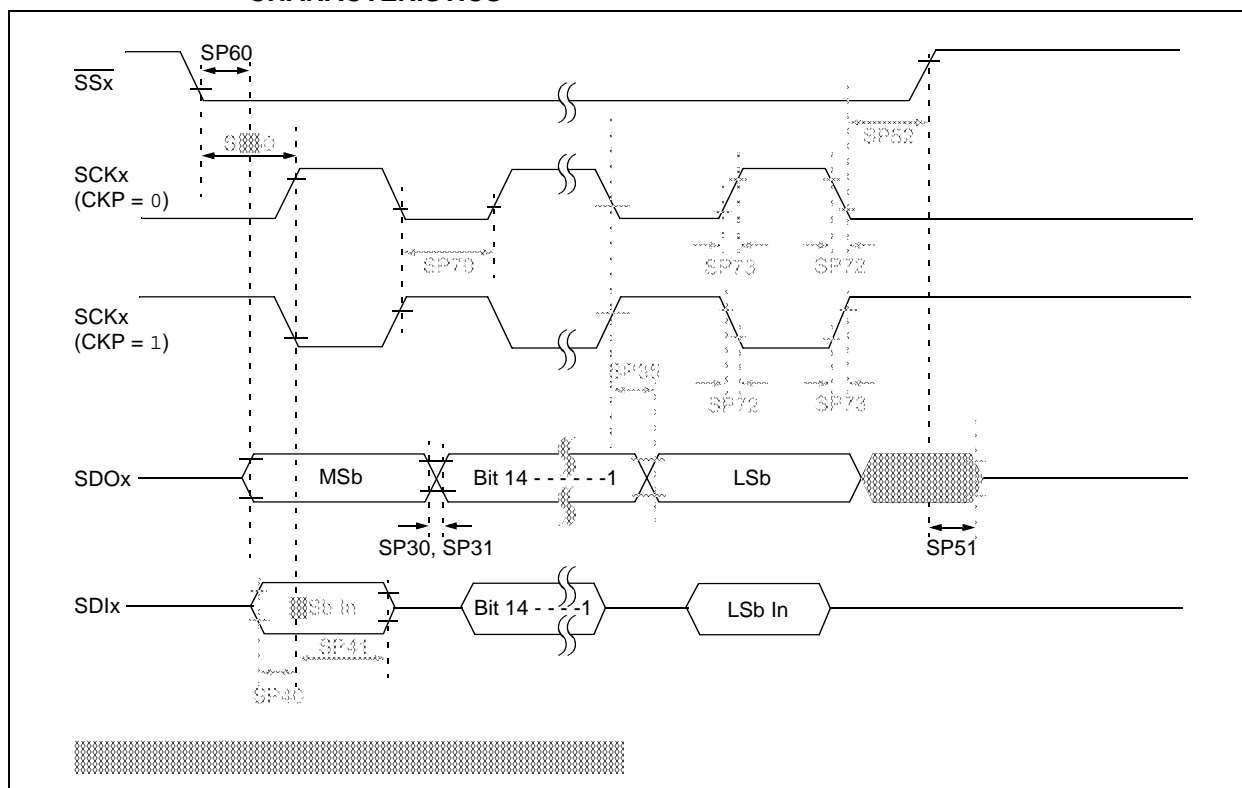
The DAC has a limitation for the maximum reference voltage input of $(AV_{DD} - 1.6)$ volts. An external reference voltage input should not exceed this value or the reference DAC output will become indeterminate.

23.9 Comparator Registers

The comparator module is controlled by the following registers:

- CMPCONx: Comparator Control x Register
- CMPDACx: Comparator DAC Control x Register

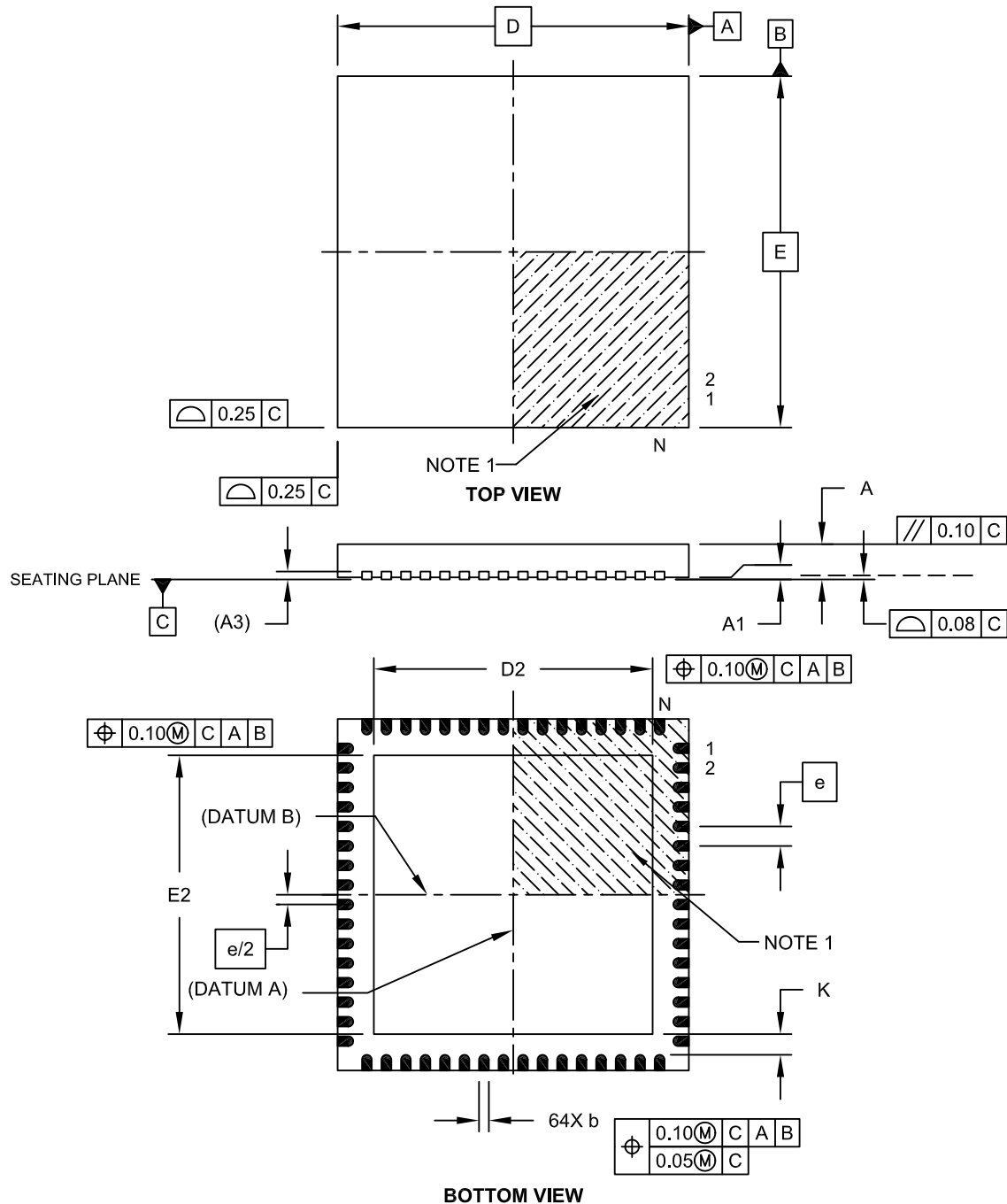
FIGURE 27-15: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



30.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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