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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

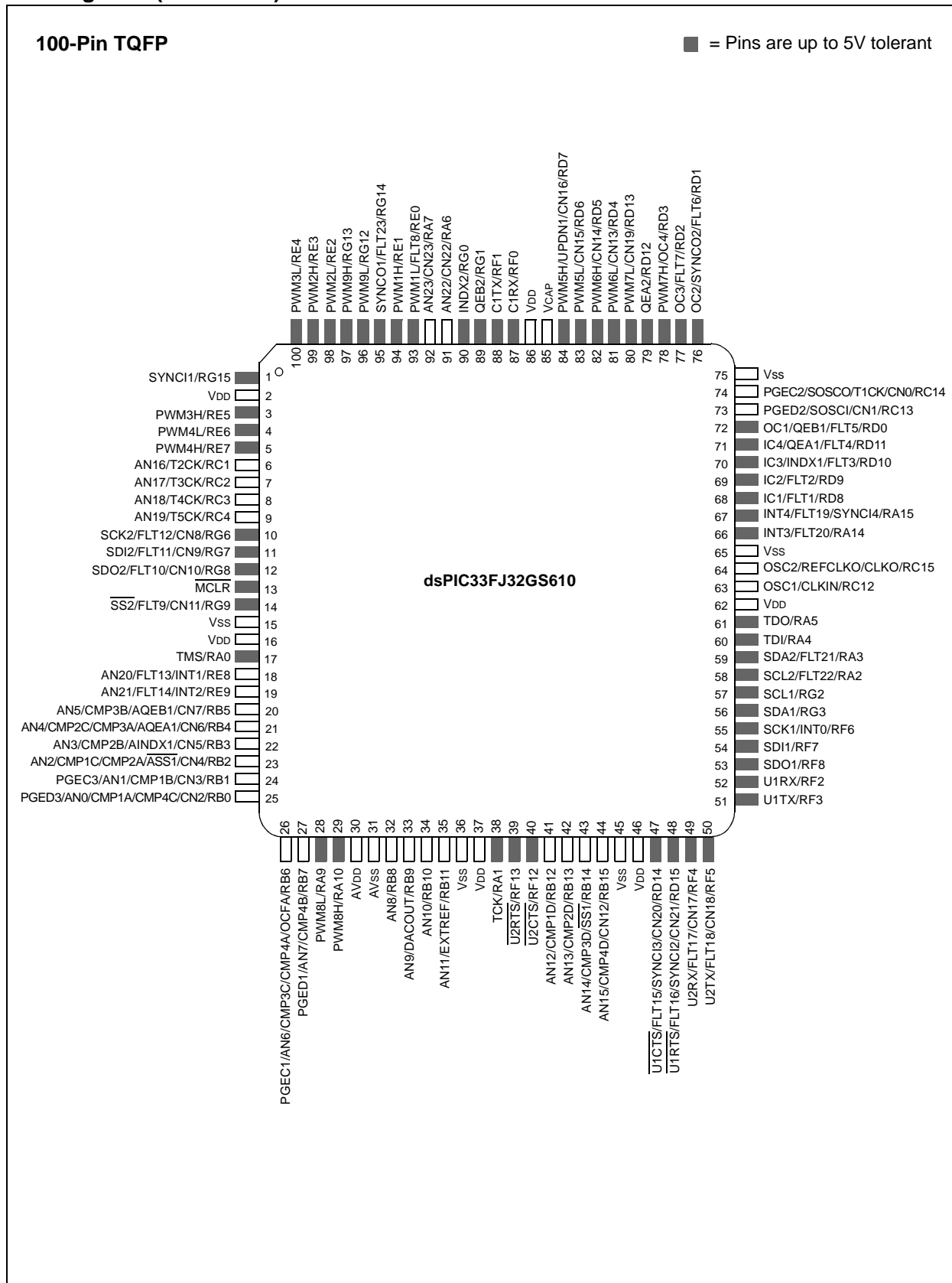| Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, QEI, POR, PWM, WDT
Number of I/O	58
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs406t-50i-pt

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant

dsPIC33FJ32GS610

Top pins (100–76):
- 100 PWM3L/RE4
- 99 PWM2H/RE3
- 98 PWM2L/RE2
- 97 PWM9H/RG13
- 96 PWM9L/RG12
- 95 SYNCO1/FLT23/RG14
- 94 PWM1H/RE1
- 93 PWM1L/FLT8/RE0
- 92 AN23/CN23/RA7
- 91 AN22/CN22/RA6
- 90 INDX2/RG0
- 89 QEB2/RG1
- 88 C1TX/RF1
- 87 C1RX/RF0
- 86 VDD
- 85 VCAP
- 84 PWM5H/UPDN1/CN16/RD7
- 83 PWM5L/CN15/RD6
- 82 PWM6H/CN14/RD5
- 81 PWM6L/CN13/RD4
- 80 PWM7L/CN19/RD13
- 79 QEA2/RD12
- 78 PWM7H/OC4/RD3
- 77 OC3/FLT7/RD2
- 76 OC2/SYNCO2/FLT6/RD1

Left pins (1–25):
- 1 SYNCI1/RG15
- 2 VDD
- 3 PWM3H/RE5
- 4 PWM4L/RE6
- 5 PWM4H/RE7
- 6 AN16/T2CK/RC1
- 7 AN17/T3CK/RC2
- 8 AN18/T4CK/RC3
- 9 AN19/T5CK/RC4
- 10 SCK2/FLT12/CN8/RG6
- 11 SDI2/FLT11/CN9/RG7
- 12 SDO2/FLT10/CN10/RG8
- 13 MCLR
- 14 SS2/FLT9/CN11/RG9
- 15 VSS
- 16 VDD
- 17 TMS/RA0
- 18 AN20/FLT13/INT1/RE8
- 19 AN21/FLT14/INT2/RE9
- 20 AN5/CMP3B/AQEB1/CN7/RB5
- 21 AN4/CMP2C/CMP3A/AQEA1/CN6/RB4
- 22 AN3/CMP2B/AINDX1/CN5/RB3
- 23 AN2/CMP1C/CMP2A/ASS1/CN4/RB2
- 24 PGEC3/AN1/CMP1B/CN3/RB1
- 25 PGED3/AN0/CMP1A/CMP4C/CN2/RB0

Bottom pins (26–50):
- 26 PGEC1/AN6/CMP3C/CMP4A/OCFA/RB6
- 27 PGED1/AN7/CMP4B/RB7
- 28 PWM8L/RA9
- 29 PWM8H/RA10
- 30 AVDD
- 31 AVSS
- 32 AN8/RB8
- 33 AN9/DACOUT/RB9
- 34 AN10/RB10
- 35 AN11/EXTREF/RB11
- 36 VSS
- 37 VDD
- 38 TCK/RA1
- 39 U2RTS/RF13
- 40 U2CTS/RF12
- 41 AN12/CMP1D/RB12
- 42 AN13/CMP2D/RB13
- 43 AN14/CMP3D/SS1/RB14
- 44 AN15/CMP4D/CN12/RB15
- 45 VSS
- 46 VDD
- 47 U1CTS/FLT15/SYNCI3/CN20/RD14
- 48 U1RTS/FLT16/SYNCI2/CN21/RD15
- 49 U2RX/FLT17/CN17/RF4
- 50 U2TX/FLT18/CN18/RF5

Right pins (75–51):
- 75 VSS
- 74 PGEC2/SOSCO/T1CK/CN0/RC14
- 73 PGED2/SOSCI/CN1/RC13
- 72 OC1/QEB1/FLT5/RD0
- 71 IC4/QEA1/FLT4/RD11
- 70 IC3/INDX1/FLT3/RD10
- 69 IC2/FLT2/RD9
- 68 IC1/FLT1/RD8
- 67 INT4/FLT19/SYNCI4/RA15
- 66 INT3/FLT20/RA14
- 65 VSS
- 64 OSC2/REFCLKO/CLKO/RC15
- 63 OSC1/CLKIN/RC12
- 62 VDD
- 61 TDO/RA5
- 60 TDI/RA4
- 59 SDA2/FLT21/RA3
- 58 SCL2/FLT22/RA2
- 57 SCL1/RG2
- 56 SDA1/RG3
- 55 SCK1/INT0/RF6
- 54 SDI1/RF7
- 53 SDO1/RF8
- 52 U1RX/RF2
- 51 U1TX/RF3

TABLE 1-1:   PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
FLT1-FLT23	I	ST	Fault inputs to PWM module.
SYNCI1-SYNCI4	I	ST	External synchronization signal to PWM master time base.
SYNCO1-SYNCO2	O	—	PWM master time base for external device synchronization.
PWM1L	O	—	PWM1 low output.
PWM1H	O	—	PWM1 high output.
PWM2L	O	—	PWM2 low output.
PWM2H	O	—	PWM2 high output.
PWM3L	O	—	PWM3 low output.
PWM3H	O	—	PWM3 high output.
PWM4L	O	—	PWM4 low output.
PWM4H	O	—	PWM4 high output.
PWM5L	O	—	PWM5 low output.
PWM5H	O	—	PWM5 high output.
PWM6L	O	—	PWM6 low output.
PWM6H	O	—	PWM6 high output.
PWM7L	O	—	PWM7 low output.
PWM7H	O	—	PWM7 high output.
PWM8L	O	—	PWM8 low output.
PWM8H	O	—	PWM8 high output.
PWM9L	O	—	PWM9 low output.
PWM9H	O	—	PWM9 high output.
PGED1	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	Positive supply for analog modules.
AVSS	P	P	Ground reference for analog modules.
VDD	P	—	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	CPU logic filter capacitor connection.
VSS	P	—	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   I = Input
ST = Schmitt Trigger input with CMOS levels   P = Power   O = Output
TTL = Transistor-Transistor Logic

The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user application. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). Programmers can check one bit in the STATUS Register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This is useful for complex number arithmetic, which typically uses both accumulators.

The device supports three Saturation and Overflow modes:

- Bit 39 Overflow and Saturation:
  When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFFFF) or maximally negative 9.31 value (0x8000000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. This condition is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (such as gain calculations).
- Bit 31 Overflow and Saturation:
  When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFFF) or maximally negative 1.31 value (0x0080000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. When this Saturation mode is in effect, the guard bits are not used, so the OA, OB or OAB bits are never set.
- Bit 39 Catastrophic Overflow:
  The bit 39 Overflow Status bit from the adder is used to set the SA or SB bit, which remains set until cleared by the user application. No saturation operation is performed, and the accumulator is allowed to overflow, destroying its sign. If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

3.6.3 ACCUMULATOR 'WRITE-BACK'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

- W13, Register Direct:
  The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13] + = 2, Register Indirect with Post-Increment:
  The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

3.6.3.1 Round Logic

The round logic is a combinational block that performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value that is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator).

- If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented.
- If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged.

A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined:

- If it is '1', ACCxH is incremented.
- If it is '0', ACCxH is not modified.

Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC), or rounded (SAC.R) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.3.2 "Data Space Write Saturation"**). For the MAC class of instructions, the accumulator write-back operation functions in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ32GS406 AND dsPIC33FJ64GS406 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS2	0088	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	—	—	—	SPI2IF	SPI2EIF	0000
IFS3	008A	—	—	—	—	—	QEI1IF	PSEMIF	—	—	INT4IF	INT3IF	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	008C	—	—	—	—	—	—	PSESMIF	—	—	—	—	—	—	U2EIF	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	ADCP12IF	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	ADCP7IF	ADCP6IF	ADCP5IF	ADCP4IF	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	—	—	—	SPI2IE	SPI2EIE	0000
IEC3	009A	—	—	—	—	—	QEI1IE	PSEMIE	—	—	INT4IE	INT3IE	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	009C	—	—	—	—	—	—	PSESMIE	—	—	—	—	—	—	U2EIE	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	ADCP12IE	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	—	ADCP0IE	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	ADCP7IE	ADCP6IE	ADCP5IE	ADCP4IE	ADCP3IE	ADCP2IE	0000
IPC0	00A4		T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	00A6		T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	00A8		U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	00AA		—	—	—	—	—	—	—	—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	—	—	—	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	00B0	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	00B2	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	00B4	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	0044
IPC9	00B6	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—	0440
IPC12	00BC	—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—	0440
IPC13	00BE	—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0	—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—	0440
IPC14	00C0	—	—	—	—	—	QEI1IP2	QEI1IP1	QEI1IP0	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0440
IPC16	00C4	—	—	—	—	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0440
IPC18	00C8	—	—	—	—	—	—	—	—	—	PSESMIP2	PSESMIP1	PSESMIP0	—	—	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ32GS608 AND dsPIC33FJ64GS608 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003
ADPCFG	0302	PCFG<15:0>																0000
ADPCFG2	0304	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCFG<17:16>		0000
ADSTAT	0306	—	—	—	P12RDY	—	—	—	P8RDY	P7RDY	P6RDY	P5RDY	P4RDY	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000
ADCPC2	030E	IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50	IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40	0000
ADCPC3	0310	IRQEN7	PEND7	SWTRG7	TRGSRC74	TRGSRC73	TRGSRC72	TRGSRC71	TRGSRC70	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC640	0000
ADCPC4	0312	—	—	—	—	—	—	—	—	IRQEN8	PEND8	SWTRG8	TRGSRC84	TRGSRC83	TRGSRC82	TRGSRC81	TRGSRC80	0000
ADCPC6	0316	—	—	—	—	—	—	—	—	IRQEN12	PEND12	SWTRG12	TRGSRC124	TRGSRC123	TRGSRC122	TRGSRC121	TRGSRC120	0000
ADCBUF0	0340	ADC Data Buffer 0																xxxx
ADCBUF1	0342	ADC Data Buffer 1																xxxx
ADCBUF2	0344	ADC Data Buffer 2																xxxx
ADCBUF3	0346	ADC Data Buffer 3																xxxx
ADCBUF4	0348	ADC Data Buffer 4																xxxx
ADCBUF5	034A	ADC Data Buffer 5																xxxx
ADCBUF6	034C	ADC Data Buffer 6																xxxx
ADCBUF7	034E	ADC Data Buffer 7																xxxx
ADCBUF8	0350	ADC Data Buffer 8																xxxx
ADCBUF9	0352	ADC Data Buffer 9																xxxx
ADCBUF10	0354	ADC Data Buffer 10																xxxx
ADCBUF11	0356	ADC Data Buffer 11																xxxx
ADCBUF12	0358	ADC Data Buffer 12																xxxx
ADCBUF13	035A	ADC Data Buffer 13																xxxx
ADCBUF14	035C	ADC Data Buffer 14																xxxx
ADCBUF15	035E	ADC Data Buffer 15																xxxx
ADCBUF16	0360	ADC Data Buffer 16																xxxx
ADCBUF17	0362	ADC Data Buffer 17																xxxx
ADCBUF24	0370	ADC Data Buffer 24																xxxx
ADCBUF25	0372	ADC Data Buffer 25																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-45:   PORTC REGISTER MAP FOR dsPIC33FJ32GS608 AND dsPIC33FJ64GS608 DEVICES**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0		TRISC<15:12>			—	—	—	—	—	—	—	—	—	TRISC<2:1>		—	F006
PORTC	02D2		RC<15:12>			—	—	—	—	—	—	—	—	—	RC<2:1>		—	xxxx
LATC	02D4		LATC<15:12>			—	—	—	—	—	—	—	—	—	LATC<2:1>		—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46:   PORTC REGISTER MAP FOR dsPIC33FJ32GS406/606 AND dsPIC33FJ64GS406/606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0		TRISC<15:12>			—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTC	02D2		RC<15:12>			—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATC	02D4		LATC<15:12>			—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47:   PORTD REGISTER MAP FOR dsPIC33FJ32GS608/610 AND dsPIC33FJ64GS608/610 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D8								TRISD<15:0>									FFFF
PORTD	02DA								RD<15:0>									xxxx
LATD	02DC								LATD<15:0>									0000
ODCD	02DE								ODCD<15:0>									0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48:   PORTD REGISTER MAP FOR dsPIC33FJ32GS406/606 AND dsPIC33FJ64GS406/606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D8	—	—	—	—					TRISD<11:0>								0FFF
PORTD	02DA	—	—	—	—					RD<11:0>								xxxx
LATD	02DC	—	—	—	—					LATD<11:0>								0000
ODCD	02DE	—	—	—	—					ODCD<11:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 4-8: **BIT-REVERSED ADDRESS EXAMPLE**
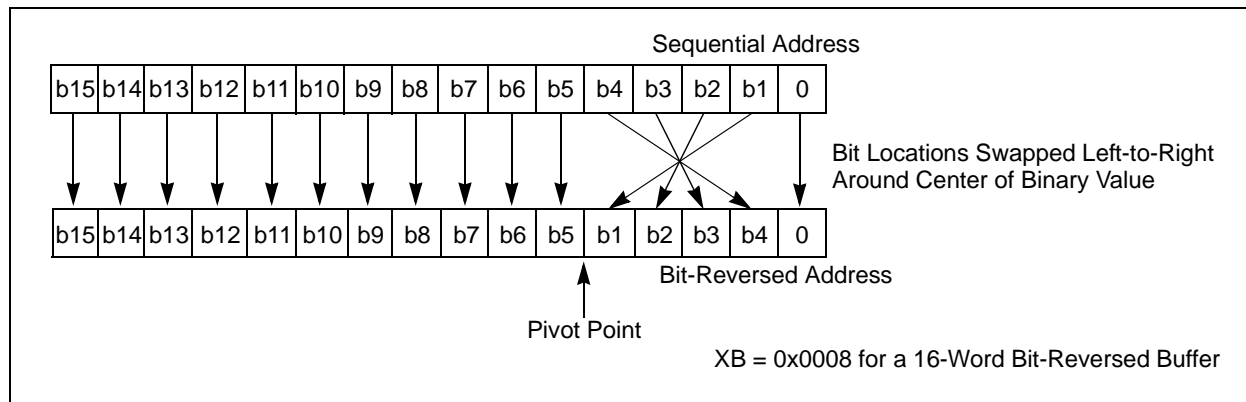
TABLE 4-67: **BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)**

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

EXAMPLE 5-2:   LOADING THE WRITE BUFFERS

```
; Set up NVMCON for row programming operations
        MOV     #0x4001, W0             ;
        MOV     W0, NVMCON             ; Initialize NVMCON
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
        MOV     #0x0000, W0             ;
        MOV     W0, TBLPAG             ; Initialize PM Page Boundary SFR
        MOV     #0x6000, W0             ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
        MOV     #LOW_WORD_0, W2         ;
        MOV     #HIGH_BYTE_0, W3        ;
        TBLWTL  W2, [W0]               ; Write PM low word into program latch
        TBLWTH  W3, [W0++]             ; Write PM high byte into program latch
; 1st_program_word
        MOV     #LOW_WORD_1, W2         ;
        MOV     #HIGH_BYTE_1, W3        ;
        TBLWTL  W2, [W0]               ; Write PM low word into program latch
        TBLWTH  W3, [W0++]             ; Write PM high byte into program latch
;  2nd_program_word
        MOV     #LOW_WORD_2, W2         ;
        MOV     #HIGH_BYTE_2, W3        ;
        TBLWTL  W2, [W0]               ; Write PM low word into program latch
        TBLWTH  W3, [W0++]             ; Write PM high byte into program latch
        •
        •
        •
; 63rd_program_word
        MOV     #LOW_WORD_31, W2        ;
        MOV     #HIGH_BYTE_31, W3       ;
        TBLWTL  W2, [W0]               ; Write PM low word into program latch
        TBLWTH  W3, [W0++]             ; Write PM high byte into program latch
```

EXAMPLE 5-3:   INITIATING A PROGRAMMING SEQUENCE

```
        DISI    #5                     ; Block all interrupts with priority <7
                                       ; for next 5 instructions
        MOV     #0x55, W0
        MOV     W0, NVMKEY             ; Write the 55 key
        MOV     #0xAA, W1              ;
        MOV     W1, NVMKEY             ; Write the AA key
        BSET    NVMCON, #WR           ; Start the erase sequence
        NOP                           ; Insert two NOPs after the
        NOP                           ; erase command is asserted
```

REGISTER 7-7:   IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4IF	IC3IF	DMA3IF	C1IF[1]	C1RXIF[1]	SPI2IF	SPI2EIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7   **Unimplemented:** Read as '0'

bit 6   **IC4IF:** Input Capture Channel 4 Interrupt Flag Status bit
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 5   **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 4   **DMA3IF:** DMA Channel 3 Data Transfer Complete Interrupt Flag Status bit
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 3   **C1IF:** ECAN1 Event Interrupt Flag Status bit[1]
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 2   **C1RXIF:** ECAN1 External Event Interrupt Flag Status bit[1]
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 1   **SPI2IF:** SPI2 Event Interrupt Flag Status bit
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

bit 0   **SPI2EIF:** SPI2 Error Interrupt Flag Status bit
        1 = Interrupt request has occurred
        0 = Interrupt request has not occurred

Note 1:   Interrupts are disabled on devices without ECAN™ modules.

REGISTER 7-13:   IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DMA1IE	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DMA1IE:** DMA Channel 1 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **ADIE:** ADC1 Conversion Complete Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI1IE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **SPI1EIE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **T3IE:** Timer3 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **DMA0IE:** DMA Channel 0 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 16-12: PDCx: PWM GENERATOR DUTY CYCLE x REGISTER[(1,2,3)]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDCx<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDCx<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PDCx<15:0>:** PWM Generator # Duty Cycle Value bits

Note 1: In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In the Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL.

2: The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0009.

3: As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 16-13: SDCx: PWM SECONDARY DUTY CYCLE x REGISTER[(1,2,3)]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SDCx<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SDCx<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **SDCx<15:0>:** Secondary Duty Cycle bits for PWMxL Output Pin

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.

2: The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0009.

3: As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 17-2: **DFLTxCON: DIGITAL FILTER x CONTROL REGISTER**

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IMV1	IMV0	CEID
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
QEOUT	QECK2	QECK1	QECK0	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11   **Unimplemented:** Read as '0'

bit 10-9   **IMV<1:0>:** Index Match Value bits

These bits allow the user application to specify the state of the QEAx and QEBx input pins during an index pulse when the POSxCNT register is to be reset.

In x4 Quadrature Count Mode:
IMV1 = Required state of Phase B input signal for match on index pulse
IMV0 = Required state of Phase A input signal for match on index pulse

In x2 Quadrature Count Mode:
IMV1 = Selects phase input signal for index state match (0 = Phase A, 1 = Phase B)
IMV0 = Required state of the selected phase input signal for match on index pulse

bit 8   **CEID:** Count Error Interrupt Disable bit

1 = Interrupts due to count errors are disabled
0 = Interrupts due to count errors are enabled

bit 7   **QEOUT:** QEAx/QEBx/INDXx Pin Digital Filter Output Enable bit

1 = Digital filter outputs are enabled
0 = Digital filter outputs are disabled (normal pin operation)

bit 6-4   **QECK<2:0>:** QEAx/QEBx/INDXx Digital Filter Clock Divide Select Bits

111 = 1:256 clock divide
110 = 1:128 clock divide
101 = 1:64 clock divide
100 = 1:32 clock divide
011 = 1:16 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 3-0   **Unimplemented:** Read as '0'

REGISTER 19-2:   I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3   **S:** Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 2   **R_W:** Read/Write Information bit (when operating as I^{2}C slave)

1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware is set or clear after reception of an I^{2}C device address byte.

bit 1   **RBF:** Receive Buffer Full Status bit

1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0   **TBF:** Transmit Buffer Full Status bit

1 = Transmit in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of the data transmission.

FIGURE 21-1: **ECANx MODULE BLOCK DIAGRAM**
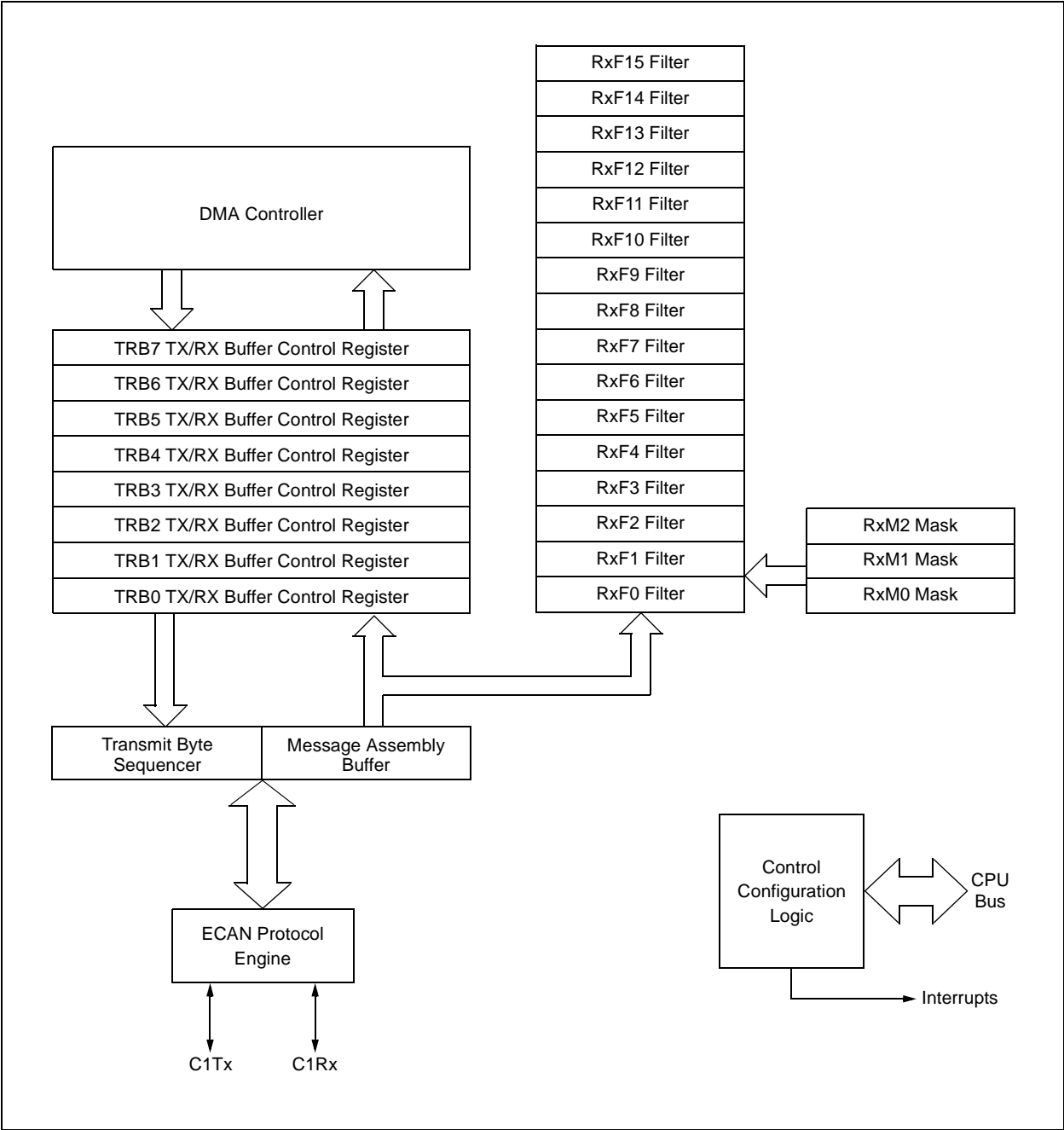
REGISTER 23-1:   CMPCONx: COMPARATOR CONTROL x REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
CMPON	—	CMPSIDL	—	—	—	—	DACOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **CMPON:** Comparator Operating Mode bit

1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)

bit 14   **Unimplemented:** Read as '0'

bit 13   **CMPSIDL:** Comparator Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode.
0 = Continues module operation in Idle mode
If a device has multiple comparators, any CMPSIDL bit set to '1' disables **ALL** comparators while in Idle mode.

bit 12-9   **Unimplemented:** Read as '0'

bit 8   **DACOE:** DAC Output Enable

1 = DAC analog voltage is output to the DACOUT pin[1]
0 = DAC analog voltage is not connected to the DACOUT pin

bit 7-6   **INSEL<1:0>:** Input Source Select for Comparator bits

11 = Selects CMPxD input pin
10 = Selects CMPxC input pin
01 = Selects CMPxB input pin
00 = Selects CMPxA input pin

bit 5   **EXTREF:** Enable External Reference bit

1 = External source provides reference to DAC (maximum DAC voltage determined by external voltage source)
0 = Internal reference sources provide reference to DAC (maximum DAC voltage determined by RANGE bit setting)

bit 4   **Unimplemented:** Read as '0'

bit 3   **CMPSTAT:** Current State of Comparator Output Including CMPPOL Selection bit

bit 2   **Unimplemented:** Read as '0'

bit 1   **CMPPOL:** Comparator Output Polarity Control bit

1 = Output is inverted
0 = Output is non-inverted

bit 0   **RANGE:** Selects DAC Output Voltage Range bit

1 = High Range: Max DAC Value = AVDD/2, 1.65V at 3.3V AVDD
0 = Low Range: Max DAC Value = INTREF

Note 1:   DACOUT can be associated only with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DAC output by setting their respective DACOE bit.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

> **Note:** For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

TABLE 25-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means "literal defined by text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register $\in$ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) $\in$ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address $\in$ {0x0000...0x1FFF}
lit1	1-bit unsigned literal $\in$ {0,1}
lit4	4-bit unsigned literal $\in$ {0...15}
lit5	5-bit unsigned literal $\in$ {0...31}
lit8	8-bit unsigned literal $\in$ {0...255}
lit10	10-bit unsigned literal $\in$ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal $\in$ {0...16384}
lit16	16-bit unsigned literal $\in$ {0...65535}
lit23	23-bit unsigned literal $\in$ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in$ {-512...511}
Slit16	16-bit signed literal $\in$ {-32768...32767}
Slit6	6-bit signed literal $\in$ {-16...16}
Wb	Base W register $\in$ {W0..W15}
Wd	Destination W register $\in$ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register $\in$ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

TABLE 27-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ[1]	Max	Units	Conditions
Operating Voltage							
DC10	VDD	**Supply Voltage[4]**	3.0	—	3.6	V	Industrial and extended
DC12	VDR	**RAM Data Retention Voltage[2]**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate[3]** to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0-3.0V in 0.1s

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: These parameters are characterized but not tested in manufacturing.

4: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below VDDMIN. See Parameter BO10 in Table 27-11 for the BOR values.

TABLE 27-39: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	Symbol	Characteristic		Min	Max	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode[1]	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode[1]	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode[1]	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode[1]	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode[1]	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode[1]	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode[1]	250		ns	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode[1]	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode[1]	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

APPENDIX A: MIGRATING FROM dsPIC33FJ06GS101/X02 AND dsPIC33FJ16GSX02/X04 TO dsPIC33FJ32GS406/606/608/610 AND dsPIC33FJ64GS406/606/608/610 DEVICES

This appendix provides an overview of considerations for migrating from the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family of devices to the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family of devices. The code developed for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices can be ported to the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices after making the appropriate changes outlined below.

A.1 Device Pins and Peripheral Pin Select (PPS)

On dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices, some peripherals such as the Timer, Input Capture, Output Compare, UART, SPI, External Interrupts, Analog Comparator Output, as well as the PWM4 pin pair, were mapped to physical pins via Peripheral Pin Select (PPS) functionality. On dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices, these peripherals are hard-coded to dedicated pins. Because of this, as well as pinout differences between the two devices families, software must be updated to utilize peripherals on the desired pin locations.

A.2 High-Speed PWM

A.2.1 FAULT AND CURRENT-LIMIT CONTROL SIGNAL SOURCE SELECTION

Fault and Current-Limit Control Signal Source selection has changed between the two families of devices. On dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices, Fault1 through Fault8 were assigned to Fault and Current-Limit Controls with the following values:

- `00000` = Fault 1
- `00001` = Fault 2
- `00010` = Fault 3
- `00011` = Fault 4
- `00100` = Fault 5
- `00101` = Fault 6
- `00110` = Fault 7
- `00111` = Fault 8

On dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices, Fault1 through Fault8 were assigned to Fault and Current-Limit Controls with the following values:

- `01000` = Fault 1
- `01001` = Fault 2
- `01010` = Fault 3
- `01011` = Fault 4
- `01100` = Fault 5
- `01101` = Fault 6
- `01110` = Fault 7
- `01111` = Fault 8

A.2.2 ANALOG COMPARATORS CONNECTION

Connection of analog comparators to the PWM Fault and Current-Limit Control Signal Sources on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is performed by assigning a comparator to one of the Fault sources via the virtual PPS pins, and then selecting the desired Fault as the source for Fault and Current-Limit Control. On dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices, analog comparators have a direct connection to Fault and Current-Limit Control, and can be selected with the following values for the CLSRC or FLTSRC bits:

- `00000` = Analog Comparator 1
- `00001` = Analog Comparator 2
- `00010` = Analog Comparator 3
- `00011` = Analog Comparator 4

A.2.3 LEADING-EDGE BLANKING (LEB)

The Leading-Edge Blanking Delay (LEB) bits have been moved from the LEBCOx register on dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices to the LEBDLYx register on dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices.

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