Microchip Technology - DSPIC33FJ64GS608-I/PT Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, QEI, POR, PWM, WDT
Number of I/O	74
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	9K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs608-i-pt

TABLE 4-33: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ32GS608 AND dsPIC33FJ64GS608 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003
ADPCFG	0302	PCFG<15:0>																0000
ADPCFG2	0304	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCFG<17:16>		0000
ADSTAT	0306	—	—	—	P12RDY	—	—	—	P8RDY	P7RDY	P6RDY	P5RDY	P4RDY	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000
ADCPC2	030E	IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50	IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40	0000
ADCPC3	0310	IRQEN7	PEND7	SWTRG7	TRGSRC74	TRGSRC73	TRGSRC72	TRGSRC71	TRGSRC70	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC640	0000
ADCPC4	0312	—	—	—	—	—	—	—	—	IRQEN8	PEND8	SWTRG8	TRGSRC84	TRGSRC83	TRGSRC82	TRGSRC81	TRGSRC80	0000
ADCPC6	0316	—	—	—	—	—	—	—	—	IRQEN12	PEND12	SWTRG12	TRGSRC124	TRGSRC123	TRGSRC122	TRGSRC121	TRGSRC120	0000
ADCBUF0	0340	ADC Data Buffer 0																xxxx
ADCBUF1	0342	ADC Data Buffer 1																xxxx
ADCBUF2	0344	ADC Data Buffer 2																xxxx
ADCBUF3	0346	ADC Data Buffer 3																xxxx
ADCBUF4	0348	ADC Data Buffer 4																xxxx
ADCBUF5	034A	ADC Data Buffer 5																xxxx
ADCBUF6	034C	ADC Data Buffer 6																xxxx
ADCBUF7	034E	ADC Data Buffer 7																xxxx
ADCBUF8	0350	ADC Data Buffer 8																xxxx
ADCBUF9	0352	ADC Data Buffer 9																xxxx
ADCBUF10	0354	ADC Data Buffer 10																xxxx
ADCBUF11	0356	ADC Data Buffer 11																xxxx
ADCBUF12	0358	ADC Data Buffer 12																xxxx
ADCBUF13	035A	ADC Data Buffer 13																xxxx
ADCBUF14	035C	ADC Data Buffer 14																xxxx
ADCBUF15	035E	ADC Data Buffer 15																xxxx
ADCBUF16	0360	ADC Data Buffer 16																xxxx
ADCBUF17	0362	ADC Data Buffer 17																xxxx
ADCBUF24	0370	ADC Data Buffer 24																xxxx
ADCBUF25	0372	ADC Data Buffer 25																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator A
0 = Trap was not caused by an overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator B
0 = Trap was not caused by an overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator A
0 = Trap was not caused by a catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator B
0 = Trap was not caused by a catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on a catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Arithmetic Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMA Controller Error Status bit
1 = DMA Controller error trap has occurred
0 = DMA Controller error trap has not occurred

bit 4 **MATHERR:** Arithmetic Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4IF	IC3IF	DMA3IF	C1IF(1)	C1RXIF(1)	SPI2IF	SPI2EIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **IC4IF:** Input Capture Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **DMA3IF:** DMA Channel 3 Data Transfer Complete Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **C1IF:** ECAN1 Event Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **C1RXIF:** ECAN1 External Event Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **SPI2IF:** SPI2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SPI2EIF:** SPI2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: Interrupts are disabled on devices without ECAN™ modules.

REGISTER 7-12: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADCP7IF	ADCP6IF	ADCP5IF	ADCP4IF	ADCP3IF	ADCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **ADCP7IF:** ADC Pair 7 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **ADCP6IF:** ADC Pair 6 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **ADCP5IF:** ADC Pair 5 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **ADCP4IF:** ADC Pair 4 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **ADCP3IF:** ADC Pair 3 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **ADCP2IF:** ADC Pair 2 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-15: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4IE	IC3IE	DMA3IE	C1IE(1)	C1RXIE(1)	SPI2IE	SPI2EIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **IC4IE:** Input Capture Channel 4 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **IC3IE:** Input Capture Channel 3 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **DMA3IE:** DMA Channel 3 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **C1IE:** ECAN1 Event Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **C1RXIE:** ECAN1 Receive Data Ready Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **SPI2IE:** SPI2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SPI2EIE:** SPI2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: Interrupts are disabled on devices without ECAN™ modules.

REGISTER 7-40: IPC24: INTERRUPT PRIORITY CONTROL REGISTER 24

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PWM6IP2	PWM6IP1	PWM6IP0	—	PWM5IP2	PWM5IP1	PWM5IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **PWM6IP<2:0>:** PWM6 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **PWM5IP<2:0>:** PWM5 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **PWM4IP<2:0>:** PWM4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PWM3IP<2:0>:** PWM3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 16-16: DTRx: PWM DEAD-TIME x REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Value for PWMx Dead-Time Unit bits

REGISTER 16-17: ALTDTRx: PWM ALTERNATE DEAD-TIME x REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Value for PWMx Dead-Time Unit bits

REGISTER 16-19: IOCONx: PWM I/O CONTROL x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1(1)	PMOD0(1)	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1(2)	FLTDAT0(2)	CLDAT1(2)	CLDAT0(2)	SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWM # I/O Pin Mode bits(1)
11 = PWM I/O pin pair is in the True Independent Output mode
10 = PWM I/O pin pair is in the Push-Pull Output mode
01 = PWM I/O pin pair is in the Redundant Output mode
00 = PWM I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> provides data for output on PWMxH pin
0 = PWM generator provides data for output on PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> provides data for output on PWMxL pin
0 = PWM generator provides data for output on PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, OVRDAT<1> provides data for PWMxH
If OVERENL = 1, OVRDAT<0> provides data for PWMxL

bit 5-4 **FLTDAT<1:0>:** State for PWMxH and PWMxL Pins if FLTMOD is Enabled bits(2)
IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If Fault is active, then FLTDAT<1> provides the state for PWMxH.
If Fault is active, then FLTDAT<0> provides the state for PWMxL.
IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
If current-limit is active, then FLTDAT<1> provides the state for PWMxH.
If Fault is active, then FLTDAT<0> provides the state for PWMxL.

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).
2: State represents the active/inactive state of the PWM depending on the POLH and POLL bit settings.

REGISTER 22-1: ADCON: ADC CONTROL REGISTER (CONTINUED)

bit 4 **ASYNCSAMP:** Asynchronous Dedicated S&H Sampling Enable bit(1)

1 = The dedicated S&H is constantly sampling and then terminates sampling as soon as the trigger pulse is detected

0 = The dedicated S&H starts sampling when the trigger event is detected and completes the sampling process in two ADC clock cycles

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ADCS<2:0>:** Analog-to-Digital Conversion Clock Divider Select bits(1)

111 = FADC/8
110 = FADC/7
101 = FADC/6
100 = FADC/5
011 = FADC/4 (default)
010 = FADC/3
001 = FADC/2
000 = FADC/1

Note 1: This control bit can only be changed while the ADC is disabled (ADON = 0).

2: This control bit is only active on devices that have one SAR.

REGISTER 22-10: ADCPC4: ADC CONVERT PAIR CONTROL REGISTER 4 (CONTINUED)

bit 4-0 **TRGSRC8<4:0>:** Trigger 8 Source Selection bits

Selects trigger source for conversion of Analog Channels AN17 and AN16.
11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to ‘1’. If other conversions are in progress, the conversion is performed when the conversion resources are available.

REGISTER 22-11: ADCPC5: ADC CONVERT PAIR CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN11	PEND11	SWTRG11	TRGSRC114	TRGSRC113	TRGSRC112	TRGSRC111	TRGSRC110
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN10	PEND10	SWTRG10	TRGSRC104	TRGSRC103	TRGSRC102	TRGSRC101	TRGSRC100
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN11:** Interrupt Request Enable 11 bit
1 = Enables IRQ generation when requested conversion of Channels AN23 and AN22 is completed
0 = IRQ is not generated

bit 14 **PEND11:** Pending Conversion Status 11 bit
1 = Conversion of Channels AN23 and AN22 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG11:** Software Trigger 11 bit
1 = Starts conversion of AN23 and AN22 (if selected by the TRGSRCx<4:0> bits)**(1)**
This bit is automatically cleared by hardware when the PEND11 bit is set.
0 = Conversion is not started

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

26.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

26.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

26.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

26.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

26.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 27-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO20A	VOH1	**Output High Voltage** I/O Pins: 4x Sink Driver Pins – RA0-RA7, RA14, RA15, RB0-RB15, RC1-RC4, RC12-RC14, RD0-RD2, RD8-RD12, RD14, RD15, RE8, RE9, RF0-RF8, RF12, RF13, RG0-RG3, RG6-RG9, RG14, RG15	1.5	—	—	V	IOH ≥ -12 mA, VDD = 3.3V (See **Note 1**)
			2.0	—	—	V	IOH ≥ -11 mA, VDD = 3.3V (See **Note 1**)
			3.0	—	—	V	IOH ≥ -3 mA, VDD = 3.3V (See **Note 1**)
		Output High Voltage I/O Pins: 8x Sink Driver Pin – RC15	1.5	—	—	V	IOH ≥ -16 mA, VDD = 3.3V (See **Note 1**)
			2.0	—	—	V	IOH ≥ -12 mA, VDD = 3.3V (See **Note 1**)
			3.0	—	—	V	IOH ≥ -4 mA, VDD = 3.3V (See **Note 1**)
		Output High Voltage I/O Pins: 16x Sink Driver Pins – RA9, RA10, RD3-RD7, RD13, RE0-RE7, RG12, RG13	1.5	—	—	V	IOH ≥ -30 mA, VDD = 3.3V (See **Note 1**)
			2.0	—	—	V	IOH ≥ -25 mA, VDD = 3.3V (See **Note 1**)
			3.0	—	—	V	IOH ≥ -8 mA, VDD = 3.3V (See **Note 1**)

Note 1: Parameters are characterized, but not tested.

TABLE 27-11: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(3) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min(1)**	**Typ**	**Max**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.6	—	2.95	V	See **Note 2**

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The device will operate as normal until the VDDMIN threshold is reached.

3: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN.

TABLE 27-19: AC CHARACTERISTICS: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)							
F20a	FRC	-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	—	+2	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN<5:0> bits can be used to compensate for temperature drift.

TABLE 27-20: AC CHARACTERISTICS: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
LPRC @ 32.768 kHz(1)						
F21a	LPRC	-40	—	+40	%	-40°C ≤ TA ≤ +85°C
F21b	LPRC	-50	—	+50	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 27-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS

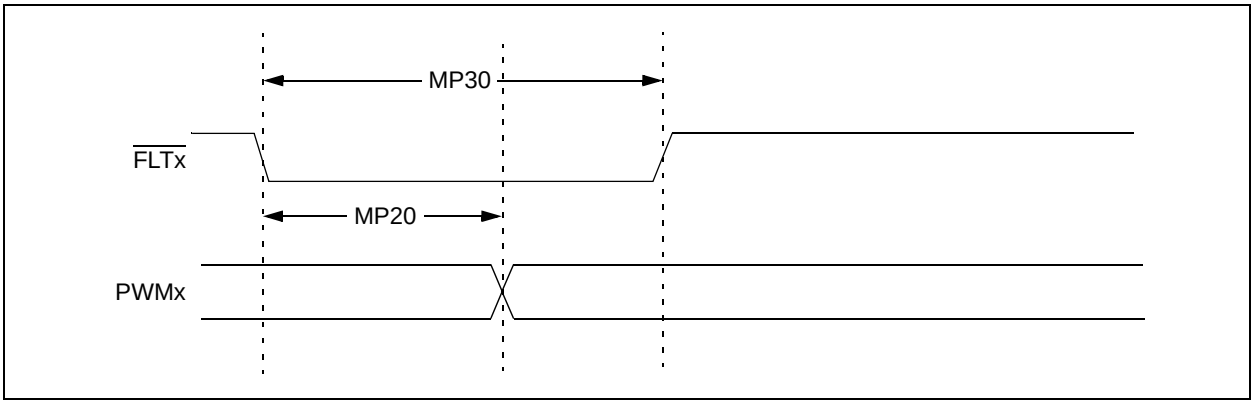
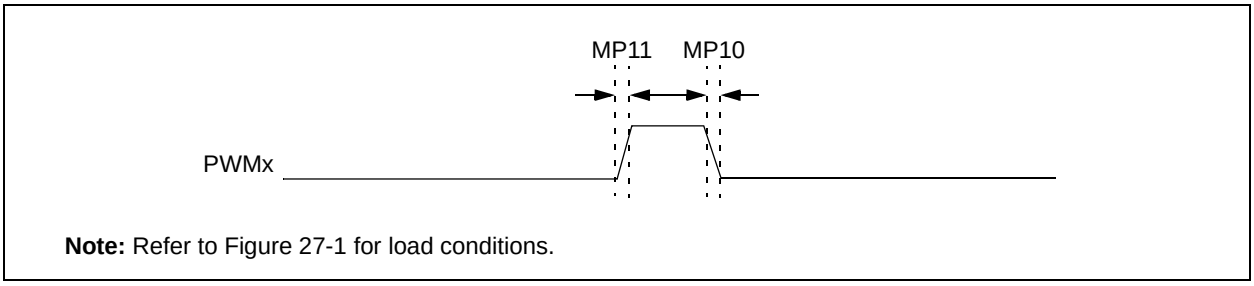


FIGURE 27-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 27-1 for load conditions.

TABLE 27-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS

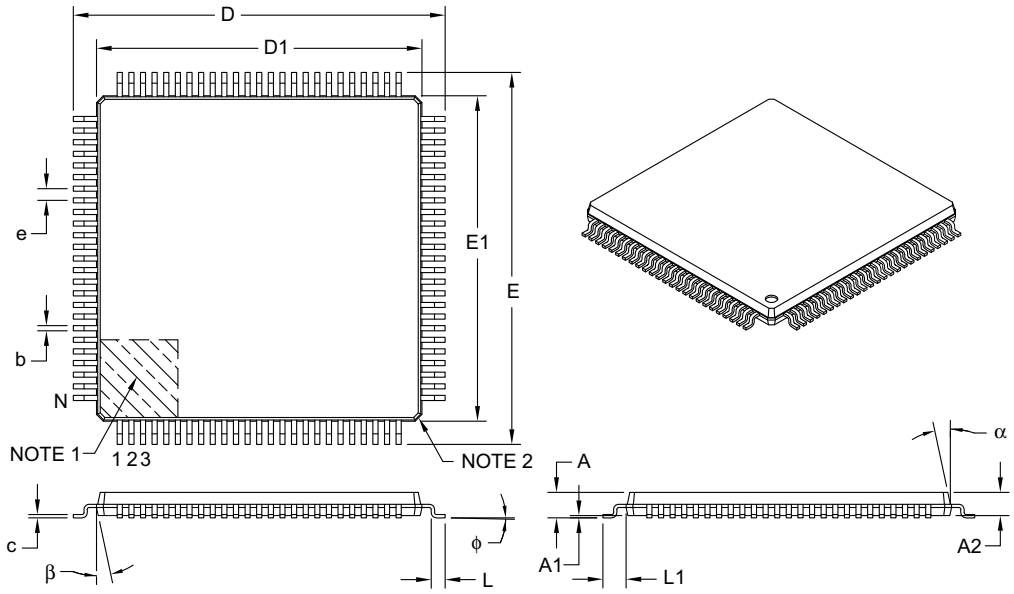
AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
MP10	TFPWM	PWMx Output Fall Time	—	2.5	—	ns	
MP11	TRPWM	PWMx Output Rise Time	—	2.5	—	ns	
MP20	TFD	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	DTC<1:0> = 10
MP30	TFH	Minimum PWMx Fault Pulse Width	8	—	—	ns	
MP31	TPDLY	Tap Delay	1.04	—	—	ns	ACLK = 120 MHz
MP32	ACLK	PWMx Input Clock	—	—	120	MHz	See **Note 2**

Note 1: These parameters are characterized but not tested in manufacturing.

2: This parameter is a maximum allowed input clock for the PWM module.

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 27.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4. Updated all Operating Current (I_{DD}) Typical and Max values in Table 27-5. Updated all Idle Current (I_{IDLE}) Typical and Max values in Table 27-6. Updated all Power-Down Current (I_{PD}) Typical and Max values in Table 27-7. Updated all Doze Current (I_{DOZE}) Typical and Max values in Table 27-8. Updated the Typ and Max values for parameter D150 and removed parameters DI26, DI28, and DI29 from the I/O Pin Input Specifications (see Table 27-9). Updated the Typ and Max values for parameter DO10 and DO27 and the Min and Typ values for parameter DO20 in the I/O Pin Output Specifications (see Table 27-10). Added parameter numbers to the Auxiliary PLL Clock Timing Specifications (see Table 27-18). Added parameters numbers and updated the Internal RC Accuracy Min, Typ, and Max values (see Table 27-19 and Table 27-20). Added parameter numbers, Note 2, updated the Min and Typ parameter values for MP31 and MP32, and removed the conditions for MP10 and MP11 in the High-Speed PWM Module Timing Requirements (see Table 27-29). Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Figure 27-14). Added parameter IM51 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 27-34). Updated the Max value for parameter AD33 in the 10-bit High-Speed ADC Module Specifications (see Table 27-36). Updated the titles and added parameter numbers to the Comparator and DAC Module Specifications (see Table 27-38 and Table 27-39) and the DAC Output Buffer Specifications (see Table 27-40).

Revision D (January 2012)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All occurrences of PGCn and PGDn (where n = 1, 2, or 3) were updated to: PGECn and PGEDn throughout the document.

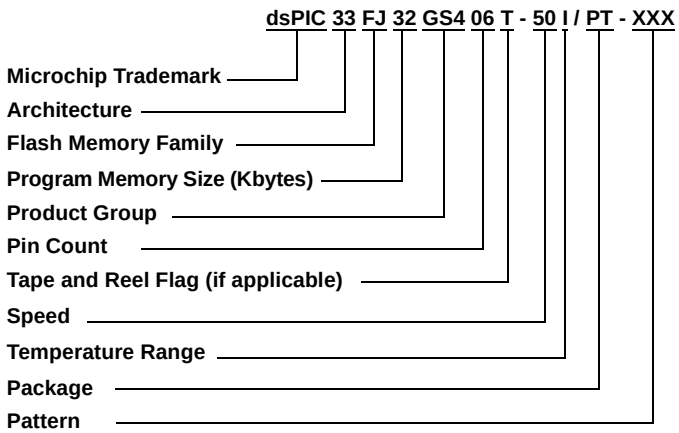
All other changes are referenced by their respective section in Table B-3.

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-Bit Digital Signal Controllers with High-Speed PWM, ADC and Comparators"	Added 50 MIPS to Operating Range. Changed the Oscillator frequency range in System Management. Added the **"Referenced Sources"** section.
Section 1.0 "Device Overview"	Updated the block diagram of the core and peripheral modules (see Figure 1-1).
Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1). Updated the VCAP pin capacitor specification in **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**.
Section 4.0 "Memory Organization"	Removed IPC20 and updated IFS5, IFS7, IEC5, IEC7, and IPC29 in the Interrupt Controller Register Map for dsPIC33FJ64GS606 devices (see Table 4-6). Removed IPC20 and IPC21 and updated IFS5, IFS7, IEC5, IEC7, and IPC29 in the Interrupt Controller Register Map for dsPIC33FJ32GS406 and dsPIC33FJ64GS406 devices (see Table 4-7). Removed IPC20 and updated IFS5, IFS7, IEC5, IEC7, and IPC29 in the Interrupt Controller Register Map for dsPIC33FJ32GS606 devices (see Table 4-10). Added High-Speed 10-bit ADC Register Map for dsPIC33FJ32GS406 and dsPIC33FJ64GS406 devices (see Table 4-35). Updated ODCG in PORTG Register Map for dsPIC33FJ32GS610 and dsPIC33FJ64GS610 devices (see Table 4-54). Updated ODCG in PORTG Register Map for dsPIC33FJ32GS608 and dsPIC33FJ64GS608 devices (see Table 4-55). Updated ODCG in PORTG Register Map for dsPIC33FJ32GS406/606 and dsPIC33FJ64GS406/606 devices (see Table 4-56).
Section 9.0 "Oscillator Configuration"	Changed the High-Speed Crystal (HS) frequency range in **Section 9.1.1 "System Clock sources"**. Updated the device operating speed to up to 50 MHz in **Section 9.1.2 "System Clock Selection"**. Updated **Section 9.1.3 "PLL Configuration"** to reflect the new operating range/speed of 50 MIPS/50 MHz. Updated **Section 9.2 "Auxiliary Clock Generation"**.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	33	=	16-Bit Digital Signal Controller
Flash Memory Family:	FJ	=	Flash program memory, 3.3V
Product Group:	GS4	=	Switch Mode Power Supply (SMPS) family
	GS6	=	Switch Mode Power Supply (SMPS) family
Pin Count:	06	=	64-pin
	08	=	80-pin
	10	=	100-pin
Speed:	50	=	50 MIPS
		=	40 MIPS (marking intentionally absent)
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	PT	=	Plastic Thin Quad Flatpack – 10x10x1 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack – 12x12x1 mm body (TQFP)
	PF	=	Plastic Thin Quad Flatpack – 14x14x1 mm body (TQFP)
	MR	=	Plastic Quad Flat, No Lead Package – 9x9x0.9 mm body (QFN)

Examples:

a) dsPIC33FJ32GS406-50-I/PT: SMPS dsPIC33, 32-Kbyte program memory, 64-pin, 50 MIPS, Industrial temp., TQFP package.

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