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Microchip Technology - DSPIC33FJ64GS608T-50I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, QEI, POR, PWM, WDT
Number of I/O	74
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	9K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs608t-50i-pt

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant

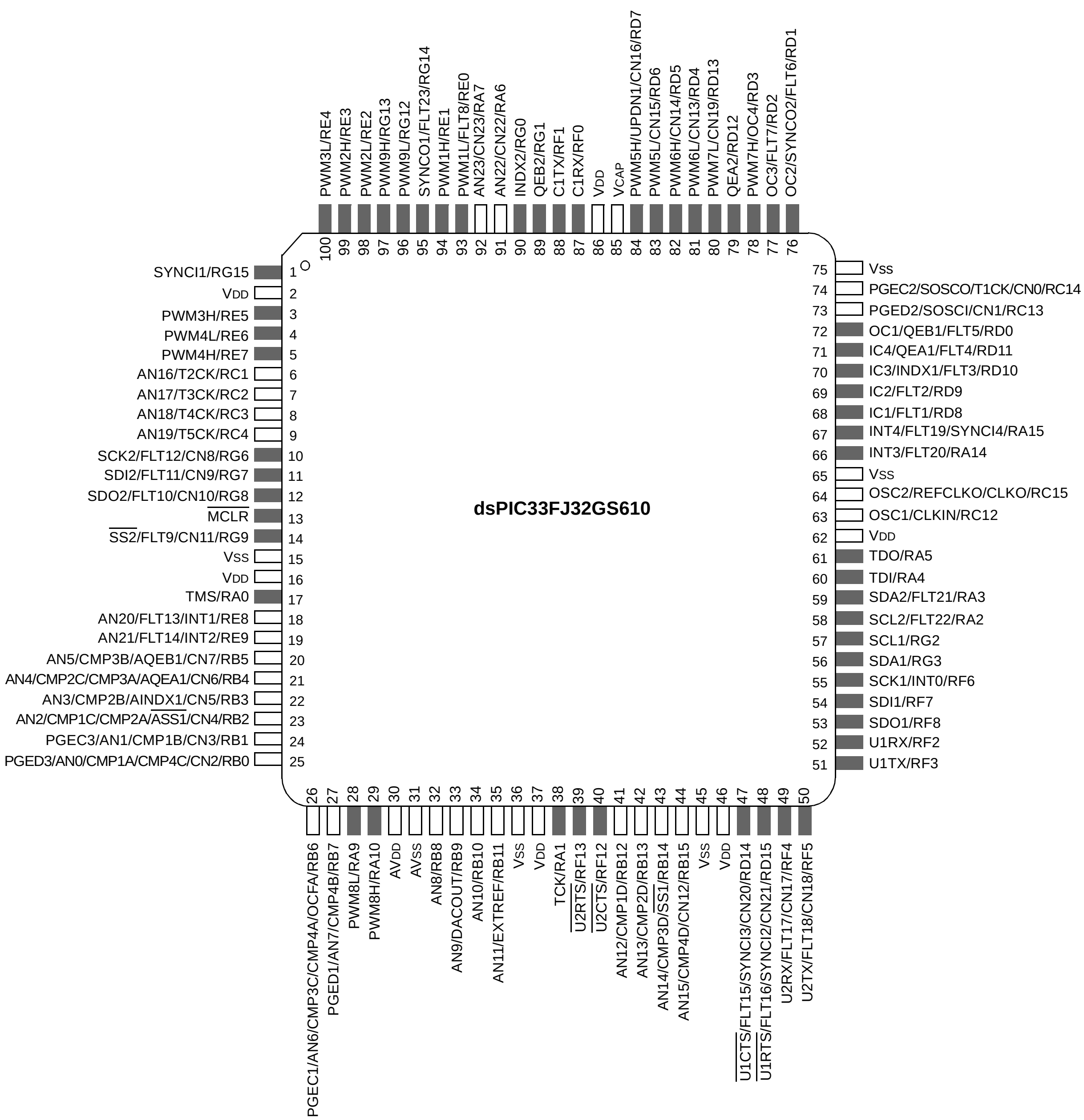

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TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN23	I	Analog	Analog input channels.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1 OSC2	I I/O	ST/CMOS —	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI SOSCO	I O	ST/CMOS —	32.768 kHz low-power oscillator crystal input; CMOS otherwise. 32.768 kHz low-power oscillator crystal output.
CN0-CN23	I	ST	Change Notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX C1TX	I O	ST —	ECAN1 bus receive pin. ECAN1 bus transmit pin.
IC1-IC4	I	ST	Capture Inputs 1 through 4.
INDX1, INDX2, AINDX1 QEA1, QEA2, AQEA1 QEB1, QEB2, AQEB1 UPDN1	I I I O	ST ST ST CMOS	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Position Up/Down Counter Direction State.
OCFA OC1-OC4	I O	ST —	Compare Fault A input. Compare Outputs 1 through 4.
INT0 INT1 INT2 INT3 INT4	I I I I I	ST ST ST ST ST	External Interrupt 0. External Interrupt 1. External Interrupt 2. External Interrupt 3. External Interrupt 4.
RA0-RA15	I/O	ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC0-RC15	I/O	ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF13	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG15	I/O	ST	PORTG is a bidirectional I/O port.
T1CK T2CK T3CK T4CK T5CK	I I I I I	ST ST ST ST ST	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic

TABLE 4-2: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ32GS608/610 AND dsPIC33FJ64GS608/610 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-3: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ32GS406/606 AND dsPIC33FJ64GS406/606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	CN23IE	CN22IE	—	—	—	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	CN23PUE	CN22PUE	—	—	—	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-9: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ32GS608

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS2	0088	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	—	—	—	SPI2IF	SPI2EIF	0000
IFS3	008A	—	—	—	—	—	QEI1IF	PSEMIF	—	—	INT4IF	INT3IF	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	008C	—	—	—	—	QEI2IF	—	PSESMIF	—	—	—	—	—	—	U2EIF	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	ADCP12IF	—	—	—	—	—	—	—	—	—	—	—	ADCP8IF	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	PWM8IF	PWM7IF	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	ADCP7IF	ADCP6IF	ADCP5IF	ADCP4IF	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	—	—	—	SPI2IE	SPI2EIE	0000
IEC3	009A	—	—	—	—	—	QEI1IE	PSEMIE	—	—	INT4IE	INT3IE	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	009C	—	—	—	—	QEI2IE	—	PSESMIE	—	—	—	—	—	—	U2EIE	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	ADCP12IE	—	—	—	—	—	—	—	—	—	—	—	ADCP8IE	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	PWM8IE	PWM7IE	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	ADCP7IE	ADCP6IE	ADCP5IE	ADCP4IE	ADCP3IE	ADCP2IE	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	00A8	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	AC1IP2	AC1IP1	AC1IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	00B0	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	00B2	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	00B4	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	0044
IPC9	00B6	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—	0440
IPC12	00BC	—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—	0440
IPC13	00BE	—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0	—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—	0440
IPC14	00C0	—	—	—	—	—	QEI1IP2	QEI1IP1	QEI1IP0	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0440
IPC16	00C4	—	—	—	—	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0440
IPC18	00C8	—	QEI2IP2	QEI2IP1	QEI2IP0	—	—	—	—	—	PSESMIP2	PSESMIP1	PSESMIP0	—	—	—	—	4040
IPC20	00CC	—	—	—	—	—	—	—	—	—	ADCP8IP2	ADCP8IP1	ADCP8IP0	—	—	—	—	0040

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-63: PMD REGISTER MAP FOR dsPIC33FJ64GS606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	ADCMD	0000
PMD2	0772	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	QEI2MD	—	—	—	I2C2MD	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	077C	—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-64: PMD REGISTER MAP FOR dsPIC33FJ32GS606 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	QEI2MD	—	—	—	I2C2MD	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	077C	—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-65: PMD REGISTER MAP FOR dsPIC33FJ32GS406 AND dsPIC33FJ64GS406 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	—	—	—	—	—	QEI2MD	—	—	—	I2C2MD	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4 Modulo Addressing

Modulo Addressing mode is a method used to provide an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.4.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

> **Note:** Y Space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.4.2 W ADDRESS REGISTER SELECTION

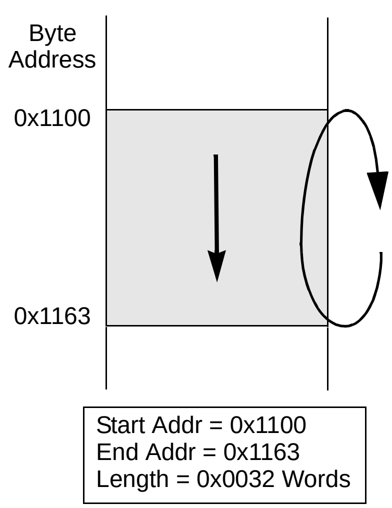
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that will operate with Modulo Addressing:

- If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-7: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT    ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND     ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON     ;enable W1, X AGU for modulo

MOV     #0x0000, W0    ;W0 holds buffer fill value

MOV     #0x1110, W1    ;point W1 to buffer

DO      AGAIN, #0x31   ;fill the 50 buffer locations
MOV     W0, [W1++]     ;fill the next location
AGAIN:  INC W0, W0     ;increment the fill value
```

REGISTER 7-32: IPC13: INTERRUPT PRIORITY CONTROL REGISTER 13

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **INT4IP<2:0>:** External Interrupt 4 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT3IP<2:0>:** External Interrupt 3 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 16-12: PDCx: PWM GENERATOR DUTY CYCLE x REGISTER(1,2,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx<15:0>:** PWM Generator # Duty Cycle Value bits

Note 1: In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In the Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL.

2: The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0009.

3: As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 16-13: SDCx: PWM SECONDARY DUTY CYCLE x REGISTER(1,2,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle bits for PWMxL Output Pin

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.

2: The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0009.

3: As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 16-23: LEBCONx: LEADING-EDGE BLANKING CONTROL x REGISTER (CONTINUED)

bit 1	**BPLH:** Blanking in PWMxL High Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high 0 = No blanking when PWMxL output is high
bit 0	**BPLL:** Blanking in PWMxL Low Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low 0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

19.0 INTER-INTEGRATED CIRCUIT (I^2C™)

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Inter-Integrated Circuit (I^2C) module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard with a 16-bit interface.

The I^2C module has a 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I^2C module offers the following key features:

- I^2C Interface Supporting Both Master and Slave modes of Operation
- I^2C Slave mode Supports 7-Bit and 10-Bit Addressing
- I^2C Master mode Supports 7-Bit and 10-Bit Addressing
- I^2C Port allows Bidirectional Transfers Between Master and Slaves
- Serial Clock Synchronization for I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I^2C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly

19.1 Operating Modes

The hardware fully implements all the master and slave functions of the I^2C Standard and Fast mode specifications, as well as 7-bit and 10-bit addressing.

The I^2C module can operate either as a slave or a master on an I^2C bus.

The following types of I^2C operation are supported:

- I^2C slave operation with 7-bit addressing
- I^2C slave operation with 10-bit addressing
- I^2C master operation with 7-bit or 10-bit addressing

For details about the communication sequence in each of these modes, refer to the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33/PIC24 Family Reference Manual"* sections.

19.2 I^2C Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write:

- I2CxRSR is the shift register used for shifting data internal to the module and the user application has no access to it.
- I2CxRCV is the receive buffer and the register to which data bytes are written or from which data bytes are read.
- I2CxTRN is the transmit register to which bytes are written during a transmit operation.
- The I2CxADD register holds the slave address.
- A status bit, ADD10, indicates 10-Bit Addressing mode.
- The I2CxBRG acts as the Baud Rate Generator (BRG) reload value.

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV and an interrupt pulse is generated.

REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 4	**URXINV:** Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	**BRGH:** High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	**PDSEL<1:0>:** Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	**STSEL:** Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

Note 1: Refer to **"UART"** (DS70188) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation. That section of the manual is available on the Microchip web site: www.microchip.com.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = SIDx bit is don’t care in filter comparison

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in filter
0 = Matches either standard or extended address message if filters match
(i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 2 **Unimplemented:** Read as ‘0’

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is don’t care in filter comparison

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is don’t care in filter comparison

REGISTER 22-2: ADSTAT: ADC STATUS REGISTER

U-0	U-0	U-0	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS
—	—	—	P12RDY(1)	P11RDY(1)	P10RDY(1)	P9RDY(1)	P8RDY(1)
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS
P7RDY(1)	P6RDY(1)	P5RDY(1)	P4RDY(1)	P3RDY(1)	P2RDY(1)	P1RDY(1)	P0RDY(1)
bit 7							bit 0

Legend:	C = Clearable bit	HS - Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 6 **P12RDY:** Conversion Data for Pair 12 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 5 **P11RDY:** Conversion Data for Pair 11 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 4 **P10RDY:** Conversion Data for Pair 10 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 3 **P9RDY:** Conversion Data for Pair 9 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 2 **P8RDY:** Conversion Data for Pair 8 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 1 **P7RDY:** Conversion Data for Pair 7 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 6 **P6RDY:** Conversion Data for Pair 6 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 5 **P5RDY:** Conversion Data for Pair 5 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 4 **P4RDY:** Conversion Data for Pair 4 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 3 **P3RDY:** Conversion Data for Pair 3 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 2 **P2RDY:** Conversion Data for Pair 2 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 1 **P1RDY:** Conversion Data for Pair 1 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

bit 0 **P0RDY:** Conversion Data for Pair 0 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a ‘0’ is written to this bit.

Note 1: Not all PxRDY bits are available on all devices. See Figure 22-1, Figure 22-2, Figure 22-3 and Figure 22-4 for the available analog inputs.

TABLE 24-2: dsPIC33F CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection bit 1 = Boot segment can be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits X11 = No boot program Flash segment Boot Space is 256 Instruction Words (except interrupt vectors): 110 = Standard security; boot program Flash segment ends at 0x0003FE 010 = High security; boot program Flash segment ends at 0x0003FE Boot Space is 768 Instruction Words (except interrupt vectors): 101 = Standard security; boot program Flash segment ends at 0x0007FE 001 = High security; boot program Flash segment ends at 0x0007FE Boot Space is 1792 Instruction Words (except interrupt vectors): 100 = Standard security; boot program Flash segment ends at 0x000FFE 000 = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bits 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-Speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user selected oscillator source when ready 0 = Start-up device with user selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Secondary (LP) Oscillator 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode

24.8 Code Protection and CodeGuard™ Security

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices offer the intermediate implementation of CodeGuard™ Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard Security can be used to securely update Flash even when multiple IPs reside on a single chip.

The code protection features are controlled by the Configuration registers: FBS and FGS.

Secure segment and RAM protection is not implemented in dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices.

Note:	Refer to **"CodeGuard™ Security"** (DS70199) *in the "dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

TABLE 24-3: CODE FLASH SECURITY SEGMENT SIZES FOR 64-KBYTE DEVICES

BSS<2:0> = `x11`, 0K	**BSS<2:0> = `x10`, 1K**	**BSS<2:0> = `x01`, 4K**	**BSS<2:0> = `x00`, 8K**
VS = 256 IW: 000000h–0001FEh 000200h GS = 21760 IW 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 768 IW: 000200h–0007FEh 000800h GS = 20992 IW 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 3840 IW: 000200h–001FFEh 002000h GS = 17920 IW 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 7936 IW: 000200h–003FFEh 004000h GS = 13824 IW 00ABFEh

TABLE 24-4: CODE FLASH SECURITY SEGMENT SIZES FOR 32-KBYTE DEVICES

BSS<2:0> = `x11`, 0K	**BSS<2:0> = `x10`, 1K**	**BSS<2:0> = `x01`, 4K**	**BSS<2:0> = `x00`, 8K**
VS = 256 IW: 000000h–0001FEh 000200h GS = 11008 IW 0057FEh 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 768 IW: 000200h–0007FEh 000800h GS = 10240 IW 0057FEh 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 3840 IW: 000200h–001FFEh 002000h GS = 7168 IW 0057FEh 00ABFEh	VS = 256 IW: 000000h–0001FEh BS = 7936 IW: 000200h–003FFEh 004000h GS = 3072 IW 0057FEh 00ABFEh

FIGURE 27-15: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

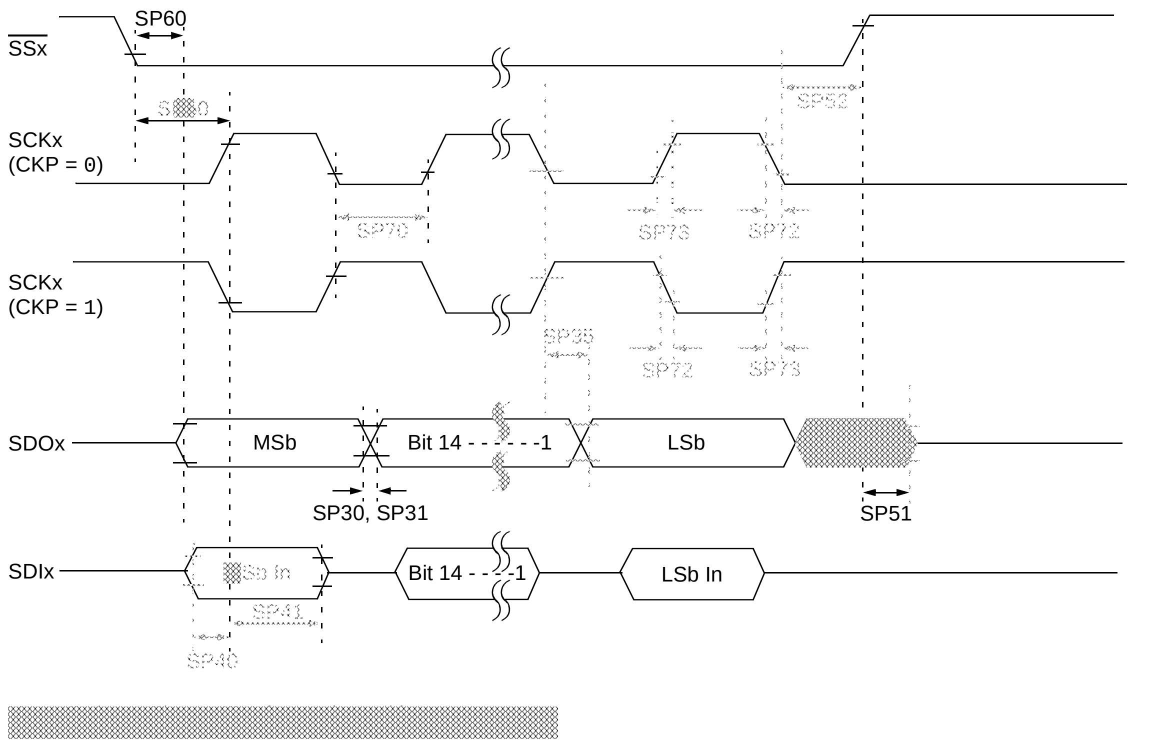


FIGURE 27-17: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

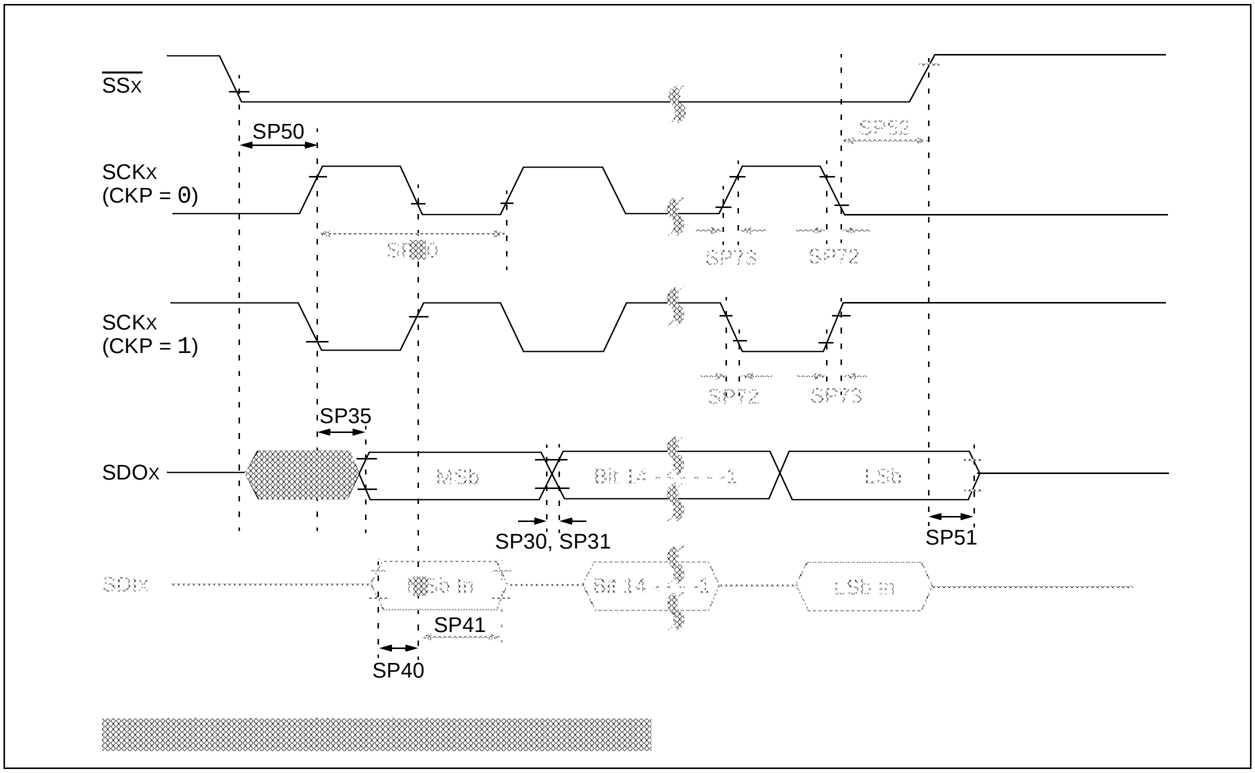
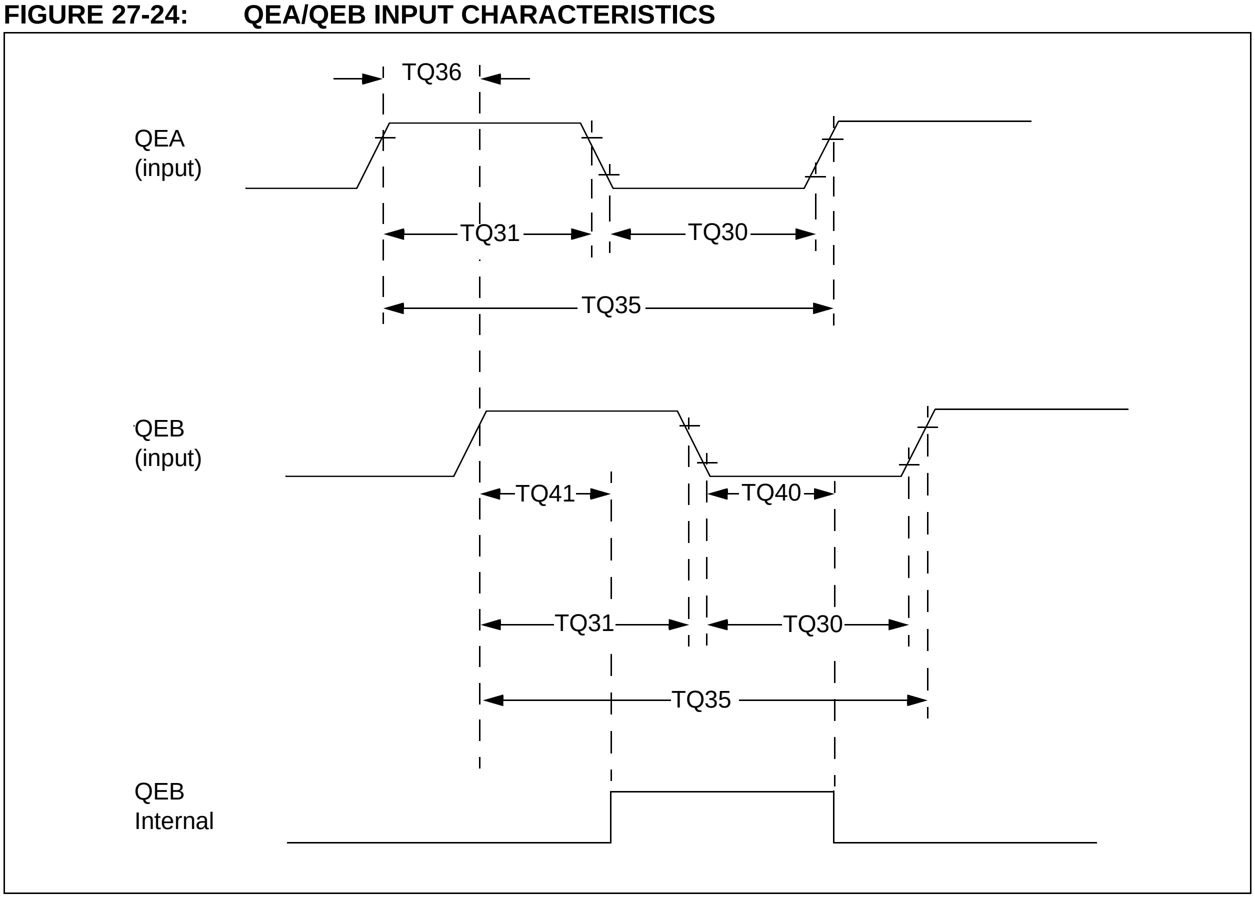


TABLE 27-44: DAC OUTPUT BUFFER SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
DA10	RLOAD	Resistive Output Load Impedance	3K	—	—	Ω	
DA11	CLOAD	Output Load Capacitance	—	20	35	pF	
DA12	IOUT	Output Current Drive Strength	200	300	400	μA	Sink and source
DA13	VRANGE	Full Output Drive Strength Voltage Range	AVSS + 250 mV	—	AVDD – 900 mV	V	
DA14	VLRANGE	Output Drive Voltage Range at Reduced Current Drive of 50 μA	AVSS + 50 mV	—	AVDD – 500 mV	V	
DA15	IDD	Current Consumed when Module is Enabled, High-Power Mode	—	—	1.3 x IOUT	μA	Module will always consume this current even if no load is connected to the output
DA16	ROUTON	Output Impedance when Module is Enabled	—	500	—	Ω	

FIGURE 27-24: QEA/QEB INPUT CHARACTERISTICS



NOTES: