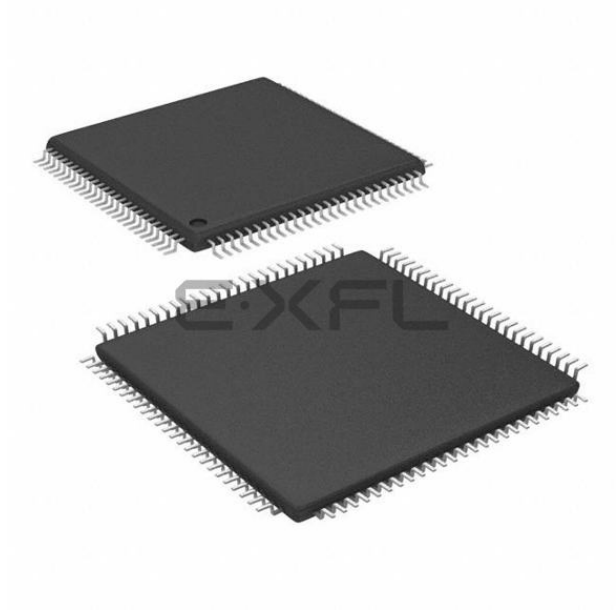
Microchip Technology - DSPIC33FJ64GS610-E/PF Datasheet



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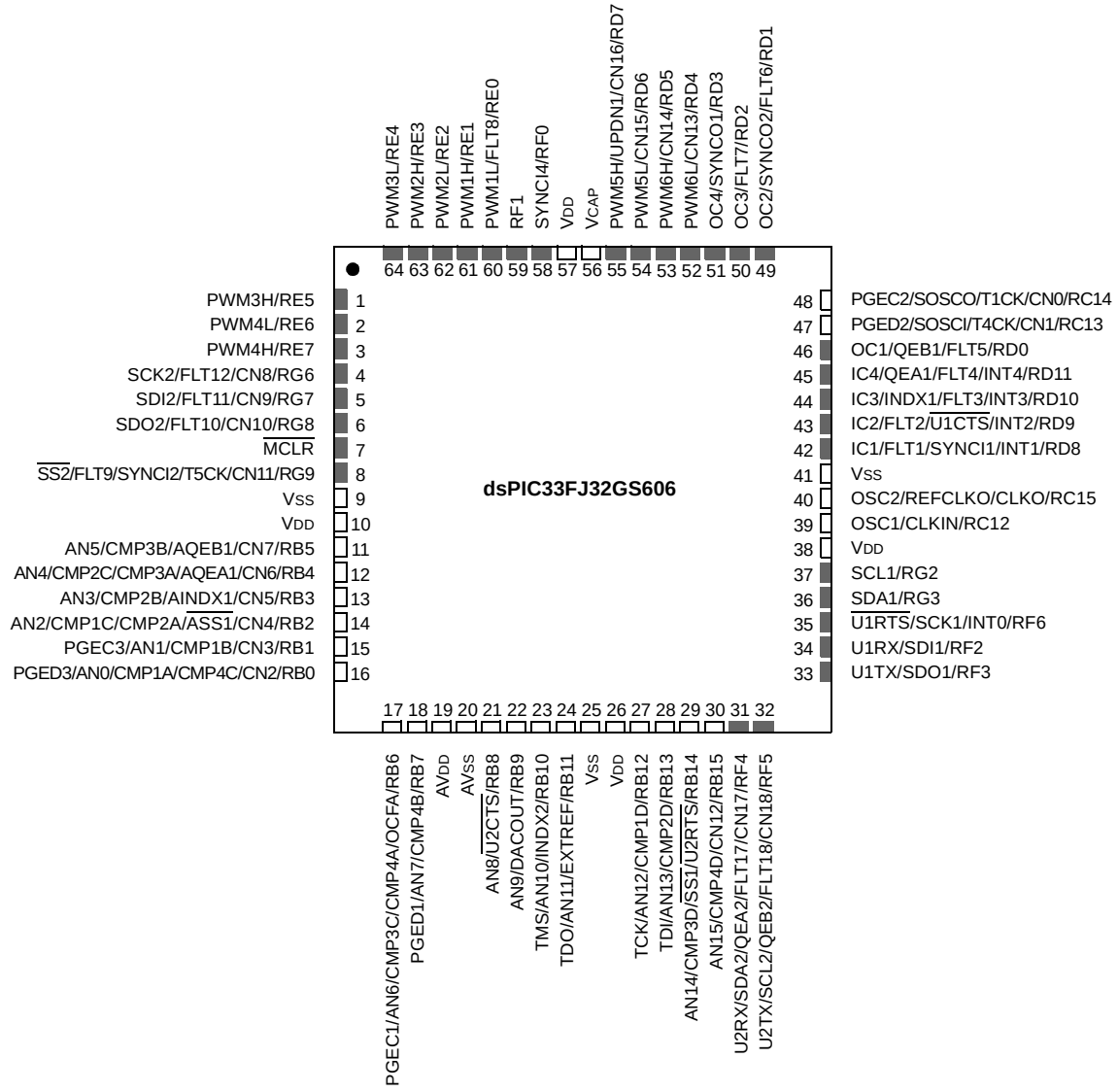
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, QEI, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	9K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gs610-e-pf

Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop is in progress
0 = REPEAT loop is not in progress

bit 3 **N:** MCU ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of a magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit
1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: This bit can be read or cleared (not set).
2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
3: The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).
4: Clearing this bit will clear SA and SB.

TABLE 4-1: CPU CORE REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0000	Working Register 0																0000
WREG1	0002	Working Register 1																0000
WREG2	0004	Working Register 2																0000
WREG3	0006	Working Register 3																0000
WREG4	0008	Working Register 4																0000
WREG5	000A	Working Register 5																0000
WREG6	000C	Working Register 6																0000
WREG7	000E	Working Register 7																0000
WREG8	0010	Working Register 8																0000
WREG9	0012	Working Register 9																0000
WREG10	0014	Working Register 10																0000
WREG11	0016	Working Register 11																0000
WREG12	0018	Working Register 12																0000
WREG13	001A	Working Register 13																0000
WREG14	001C	Working Register 14																0000
WREG15	001E	Working Register 15																0800
SPLIM	0020	Stack Pointer Limit Register																xxxx
ACCAL	0022	ACCAL																xxxx
ACCAH	0024	ACCAH																xxxx
ACCAU	0026	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCAU								xxxx
ACCBL	0028	ACCBL																xxxx
ACCBH	002A	ACCBH																xxxx
ACCBU	002C	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCBU								xxxx
PCL	002E	Program Counter Low Byte Register																0000
PCH	0030	—	—	—	—	—	—	—	—	Program Counter High Byte Register								0000
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Page Address Pointer Register								0000
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Memory Visibility Page Address Pointer Register								0000
RCOUNT	0036	REPEAT Loop Counter Register																xxxx
DCOUNT	0038	DCOUNT<15:0>																xxxx
DOSTARTL	003A	DOSTARTL<15:1>															0	xxxx
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						00xx
DOENDL	003E	DOENDL<15:1>															0	xxxx
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH						00xx
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.2 RTSP Operation

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. Table 27-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the Table Write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 27-20) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time and Word Write Cycle Time parameters (see Table 27-12).

EQUATION 5-1: PROGRAMMING TIME

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±2%. If the TUN<5:0> bits (see Register 9-4) are set to 'b000000, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 + 0.02) \times (1 - 0.000938)} = 1.473\ ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 - 0.02) \times (1 - 0.000938)} = 1.533\ ms$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0(1)	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	ERASE	—	—	NVMOP3(2)	NVMOP2(2)	NVMOP1(2)	NVMOP0(2)
bit 7							bit 0

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **ERASE:** Erase/Program Enable bit(1)
- 1 = Performs the erase operation specified by the NVMOP<3:0> bits on the next WR command
- 0 = Performs the program operation specified by the NVMOP<3:0> bits on the next WR command

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(1,2)

If ERASE = 1:
- 1111 = Memory bulk erase operation
- 1101 = Erases General Segment (GS)
- 0011 = No operation
- 0010 = Memory page erase operation
- 0001 = No operation
- 0000 = Erases a single Configuration register byte

If ERASE = 0:
- 1111 = No operation
- 1101 = No operation
- 0011 = Memory word program operation
- 0010 = No operation
- 0001 = Memory row program operation
- 0000 = Programs a single Configuration register byte

Note 1: These bits can only be reset on a Power-on Reset.

2: All other combinations of NVMOP<3:0> are unimplemented.

NOTES:

REGISTER 16-11: PWMCONx: PWM CONTROL x REGISTER

HS/HC-0	HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(3)	MDCS(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP(4)	—	MTBS	CAM(2,3,5)	XPRES(6)	IUE
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(3)
1 = PHASEx/SPHASEx registers provide time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(3)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx and SDCx registers provide duty cycle information for this PWM generator

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.

2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

3: These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.

4: For DTCP to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.

6: Configure CLMOD (FCLCONX<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

REGISTER 16-11: PWMCONx: PWM CONTROL x REGISTER (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(4)
1 = If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened;
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened
0 = If DTCMPx = 0, PWMxH is shortened and PWMLx is lengthened;
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened

bit 4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and the clock source for the PWM generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3,5)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWM Reset Control bit(6)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active PDCx registers are synchronized to the PWM time base

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
3: These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.
4: For DTCP to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.
5: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
6: Configure CLMOD (FCLCONX<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

REGISTER 16-26: PWMCAPx: PRIMARY PWM TIME BASE CAPTURE x REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWMCAP<12:5>(1,2,3,4)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	U-0	U-0	U-0
PWMCAP<4:0>(1,2,3,4)					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **PWMCAP<12:0>:** Captured PWM Time Base Value bits(1,2,3,4)
The value in this register represents the captured PWM time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The capture feature is only available on the primary output (PWMxH).
2: This feature is active only after LEB processing on the current-limit input signal is complete.
3: The minimum capture resolution is 8.32 ns.
4: This feature can be used when the XPRES bit (PWMCONx<1>) is set to '0'.

REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	r	REQOP2	REQOP1	REQOP0
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** ECANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **Reserved:** Do not use

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Sets Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Sets Configuration mode
011 = Sets Listen Only Mode
010 = Sets Loopback mode
001 = Sets Disable mode
000 = Sets Normal Operation mode

bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** ECAN Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on ECAN message receive
0 = Disables ECAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

BUFFER 21-3: ECANx MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **EID<5:0>:** Extended Identifier bits

bit 9 **RTR:** Remote Transmission Request bit
1 = Message will request remote transmission
0 = Normal message

bit 8 **RB1:** Reserved Bit 1
User must set this bit to ‘0’ per ECAN™ protocol.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **RB0:** Reserved Bit 0
User must set this bit to ‘0’ per ECAN protocol.

bit 3-0 **DLC<3:0>:** Data Length Code bits

BUFFER 21-4: ECANx MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

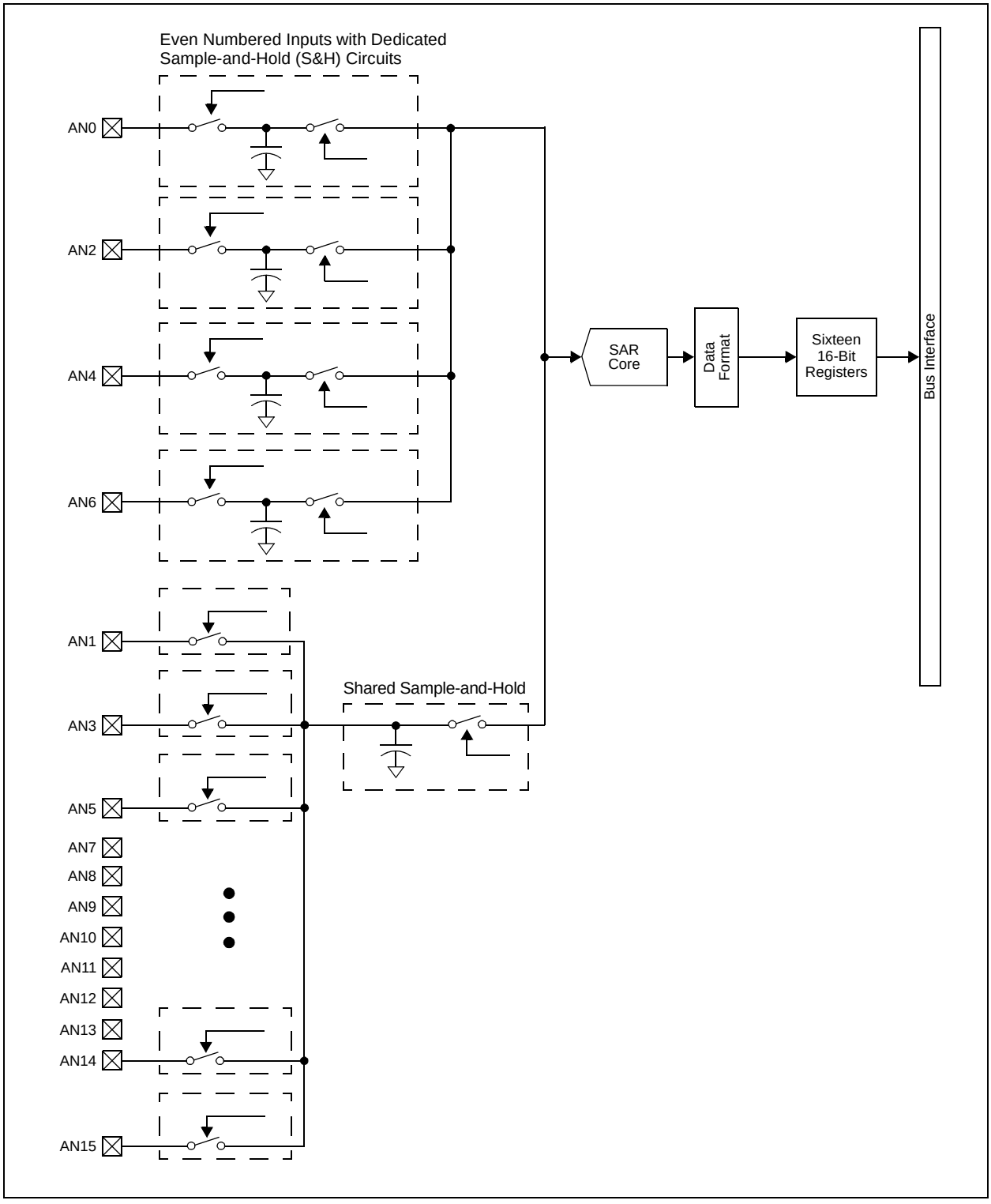
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 1<15:8>:** ECANx Message Byte 1

bit 7-0 **Byte 0<7:0>:** ECANx Message Byte 0

FIGURE 22-1: ADC BLOCK DIAGRAM FOR dsPIC33FJ32GS406 AND dsPIC33FJ64GS406 DEVICES WITH ONE SAR



REGISTER 22-9: ADCPC3: ADC CONVERT PAIR CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN7	PEND7	SWTRG7	TRGSRC74	TRGSRC73	TRGSRC72	TRGSRC71	TRGSRC70
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC60
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN7:** Interrupt Request Enable 7 bit
1 = Enables IRQ generation when requested conversion of Channels AN15 and AN14 is completed
0 = IRQ is not generated

bit 14 **PEND7:** Pending Conversion Status 7 bit
1 = Conversion of Channels AN15 and AN14 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG7:** Software Trigger 7 bit
1 = Starts conversion of AN15 and AN14 (if selected by the TRGSRCx<4:0> bits)**(1)**
This bit is automatically cleared by hardware when the PEND7 bit is set.
0 = Conversion has not started

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

REGISTER 22-9: ADCPC3: ADC CONVERT PAIR CONTROL REGISTER 3 (CONTINUED)

bit 4-0 **TRGSRC6<4:0>:** Trigger 6 Source Selection bits
Selects trigger source for conversion of Analog Channels AN13 and AN12.
11111 = Timer2 period match
11110 = PWM Generator 8 current-limit ADC trigger
11101 = PWM Generator 7 current-limit ADC trigger
11100 = PWM Generator 6 current-limit ADC trigger
11011 = PWM Generator 5 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = PWM Generator 9 secondary trigger selected
10101 = PWM Generator 8 secondary trigger selected
10100 = PWM Generator 7 secondary trigger selected
10011 = PWM Generator 6 secondary trigger selected
10010 = PWM Generator 5 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
01110 = PWM Generator 1 secondary trigger selected
01101 = PWM secondary Special Event Trigger selected
01100 = Timer1 period match
01011 = PWM Generator 8 primary trigger selected
01010 = PWM Generator 7 primary trigger selected
01001 = PWM Generator 6 primary trigger selected
01000 = PWM Generator 5 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00100 = PWM Generator 1 primary trigger selected
00011 = PWM Special Event Trigger selected
00010 = Global software trigger selected
00001 = Individual software trigger selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as an individual software trigger prior to setting this bit to '1'. If other conversions are in progress, the conversion is performed when the conversion resources are available.

TABLE 25-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-Bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE,Expr	Branch if Greater Than or Equal	1	1 (2)	None
		BRA	GEU,Expr	Branch if Unsigned Greater Than or Equal	1	1 (2)	None
		BRA	GT,Expr	Branch if Greater Than	1	1 (2)	None
		BRA	GTU,Expr	Branch if Unsigned Greater Than	1	1 (2)	None
		BRA	LE,Expr	Branch if Less Than or Equal	1	1 (2)	None
		BRA	LEU,Expr	Branch if Unsigned Less Than or Equal	1	1 (2)	None
		BRA	LT,Expr	Branch if Less Than	1	1 (2)	None
		BRA	LTU,Expr	Branch if Unsigned Less Than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (2)	None
		BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2)	None
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
		BRA	SA,Expr	Branch if Accumulator A Saturated	1	1 (2)	None
		BRA	SB,Expr	Branch if Accumulator B Saturated	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws<Wb>	1	1	None

TABLE 27-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off, Clock On Base Current(2)						
DC40d	8	15	mA	-40°C	3.3V	10 MIPS
DC40a	9	15	mA	+25°C		
DC40b	9	15	mA	+85°C		
DC40c	10	15	mA	+125°C		
DC41d	11	20	mA	-40°C	3.3V	16 MIPS(3)
DC41a	11	20	mA	+25°C		
DC41b	11	20	mA	+85°C		
DC41c	12	20	mA	+125°C		
DC42d	14	25	mA	-40°C	3.3V	20 MIPS(3)
DC42a	14	25	mA	+25°C		
DC42b	14	25	mA	+85°C		
DC42c	15	25	mA	+125°C		
DC43d	20	30	mA	-40°C	3.3V	30 MIPS(3)
DC43a	20	30	mA	+25°C		
DC43b	21	30	mA	+85°C		
DC43c	22	30	mA	+125°C		
DC44d	29	40	mA	-40°C	3.3V	40 MIPS
DC44a	29	40	mA	+25°C		
DC44b	30	40	mA	+85°C		
DC44c	31	40	mA	+125°C		

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are all ‘0’s)
- JTAG is disabled

3: These parameters are characterized but not tested in manufacturing.

TABLE 27-8: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typical(1)**	**Max**	**Doze Ratio**	**Units**	**Conditions**		
Doze Current (IDOZE)(2)							
DC73a	45	60	1:2	mA	-40°C	3.3V	40 MIPS
DC73f	40	60	1:64	mA			
DC73g	40	60	1:128	mA			
DC70a	43	60	1:2	mA	+25°C	3.3V	40 MIPS
DC70f	38	60	1:64	mA			
DC70g	38	60	1:128	mA			
DC71a	42	60	1:2	mA	+85°C	3.3V	40 MIPS
DC71f	37	60	1:64	mA			
DC71g	37	60	1:128	mA			
DC72a	41	60	1:2	mA	+125°C	3.3V	40 MIPS
DC72f	36	60	1:64	mA			
DC72g	36	60	1:128	mA			

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

2: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are all '0's)
- CPU executing `while(1)` statement
- JTAG disabled

FIGURE 27-21: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

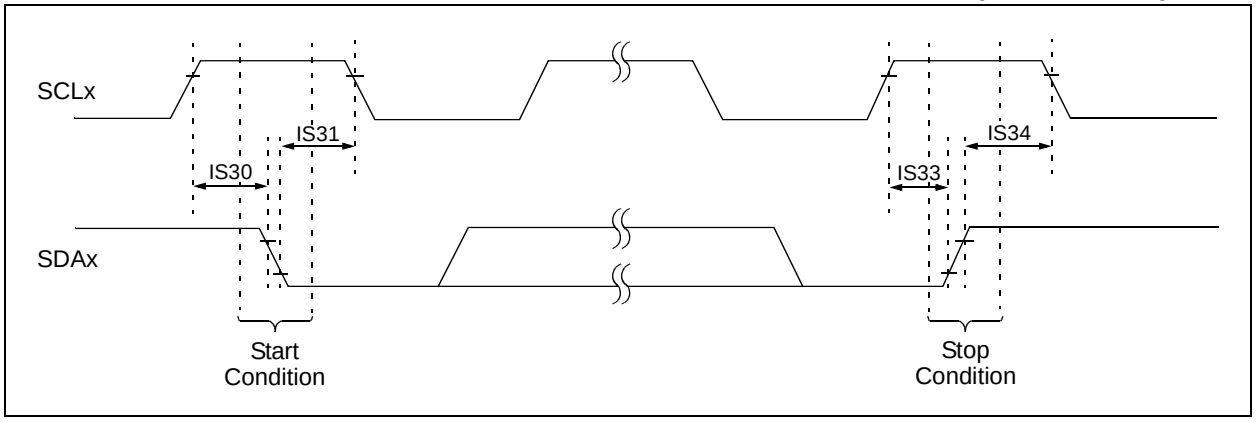


FIGURE 27-22: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

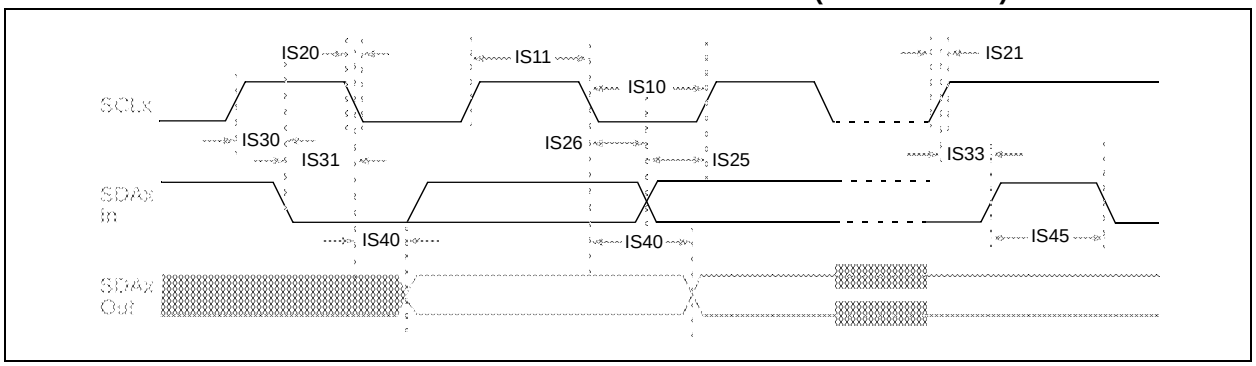


TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 27.0 "Electrical Characteristics" (Continued)	Updated the Timer1, Timer2, and Timer3 External Clock Timing Requirements (see Table 27-23, Table 27-24, and Table 27-25). Updated the Simple OC/PWM Mode Timing Requirements (see Table 27-28). Updated all SPI Timing specifications (see Figure 27-11-Figure 27-18 and Table 27-30-Table 27-37). Added Note 2 to the 10-bit High-Speed ADC Module Specifications (see Table 27-40). Added Note 2 to the 10-bit High-Speed ADC Module Timing Requirements (see Table 27-41). Added parameter DA08 to the DAC Module Specifications (see Table 27-43). Updated parameter DA16 in the DAC Output Buffer Specifications (see Table 27-44). Added DMA Read/Write Timing Requirements (see Table 27-49).
Section 28.0 "50 MIPS Electrical Characteristics"	Added new chapter with electrical specifications for 50 MIPS devices.
Section 29.0 "DC and AC Device Characteristics Graphs"	Added new chapter.

Revision E (October 2012)

This revision removes the Preliminary watermark and includes minor typographical and formatting changes throughout the data sheet.

Revision F (July 2014)

Changes CHOP bit to CHOPCLK in the High Speed PWM Register Map and CHOPCLK PWMCHOP Clock Generator Register (see Register 4-16 and Register 16-9).

Changes values in the Minimum Row Write Time and Maximum Row Write time equation examples (see Equation 5-2 and Equation 5-3).

Adds the Oscillator Delay table (see Table 6-2).

Updates TUN bit ranges in the OSCTUN: Oscillator Tuning Register (see Register 9-4).

Updates the Type C Timer Block Diagram (see Figure 13-2).

Adds Note 1 to the CxFCTRL: ECANx FIFO Control Register (see Register 21-4).

Adds Note 10 to the DC Characteristics: I/O Pin Input Specifications (see Table 27-9).

Updates values in the DC Characteristics: Program Memory Table (see Table 27-12).

Adds Register 29-7 through Register 29-12 to **Section 29.0 "DC and AC Device Characteristics Graphs"**

Also includes minor typographical and formatting changes throughout the data sheet.