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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
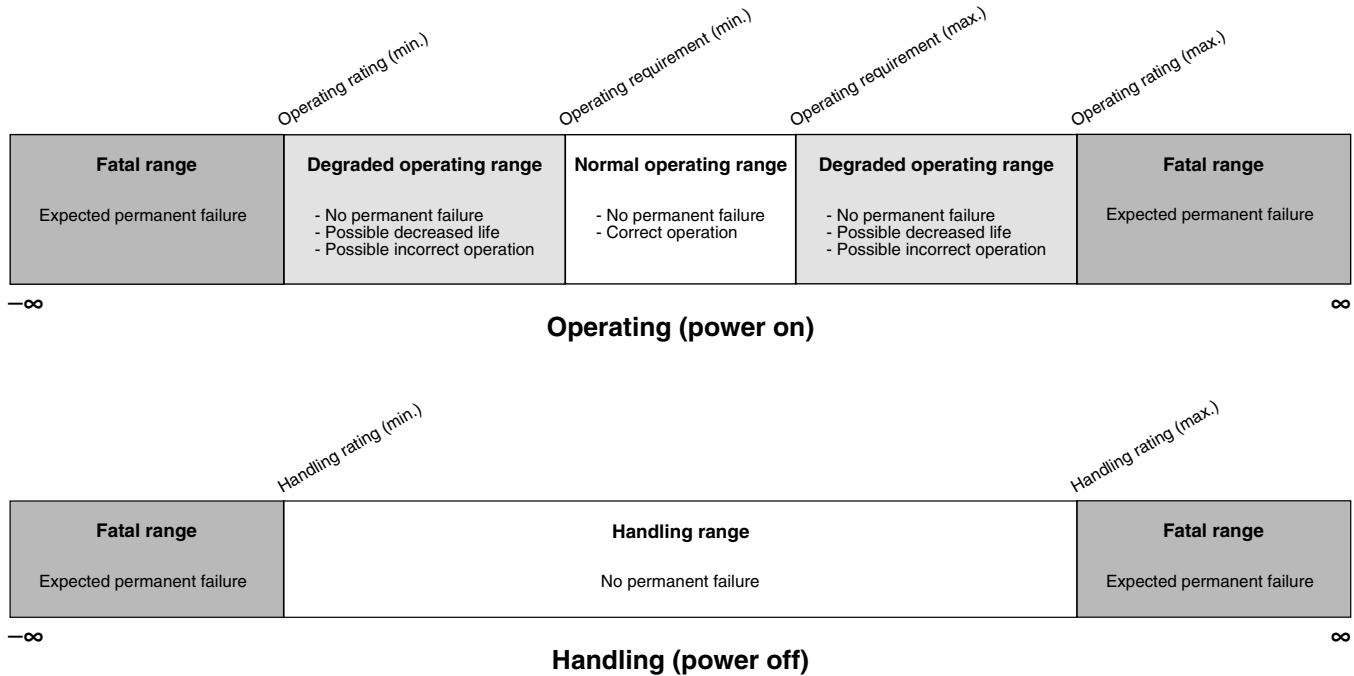
## Applications of "Embedded - Microcontrollers"

### Details

| | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit |
| Speed | 100MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, IrDA, SDHC, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LCD, LVD, POR, PWM, Touch-Sense, WDT |
| Number of I/O | 94 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk53dx256zclq10 |

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - I2S module

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Freescale Semiconductor, Inc.

## 3.6 Relationship between ratings and operating requirements



**Operating (power on)**



**Handling (power off)**

## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:
- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

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**Table 6.  Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| I$_{DD\_VBAT}$ | Average current when CPU is not accessing RTC registers |  |  |  |  | 10 |
|  | • @ 1.8V |  |  |  |  |  |
|  |    • @ −40 to 25°C | — | 0.71 | 0.81 | µA |  |
|  |    • @ 70°C | — | 1.01 | 1.3 | µA |  |
|  |    • @ 105°C | — | 2.82 | 4.3 | µA |  |
|  | • @ 3.0V |  |  |  |  |  |
|  |    • @ −40 to 25°C | — | 0.84 | 0.94 | µA |  |
|  |    • @ 70°C | — | 1.17 | 1.5 | µA |  |
|  |    • @ 105°C | — | 3.16 | 4.6 | µA |  |

1.  The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2.  100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3.  100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
4.  Max values are measured with CPU executing DSP instructions.
5.  25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6.  2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7.  2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8.  2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9.  Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 µA.
10.  Includes 32kHz oscillator current and RTC operation.

## 5.2.5.1   Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

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2. $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 12 MHz (crystal), $f_{SYS}$ = 96 MHz, $f_{BUS}$ = 48MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7   Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1.  Go to www.freescale.com.
2.  Perform a keyword search for "EMC design."

## 5.2.8   Capacitance attributes

**Table 8.   Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

# 5.3   Switching specifications

## 5.3.1   Device clock specifications

**Table 9.   Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Normal run mode | | | | |
| $f_{SYS}$ | System and core clock | — | 100 | MHz | |
| $f_{SYS\_USB}$ | System and core clock when Full Speed USB in operation | 20 | — | MHz | |
| $f_{ENET}$ | System and core clock when ethernet in operation | | | MHz | |
| | • 10 Mbps | 5 | — | | |
| | • 100 Mbps | 50 | — | | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| FB_CLK | FlexBus clock | — | 50 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |

2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 Debug trace timing specifications

**Table 12. Debug trace operating behaviors**

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $T_{cyc}$ | Clock period | Frequency dependent | | MHz |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |
| $T_s$ | Data setup | 3 | — | ns |
| $T_h$ | Data hold | 2 | — | ns |
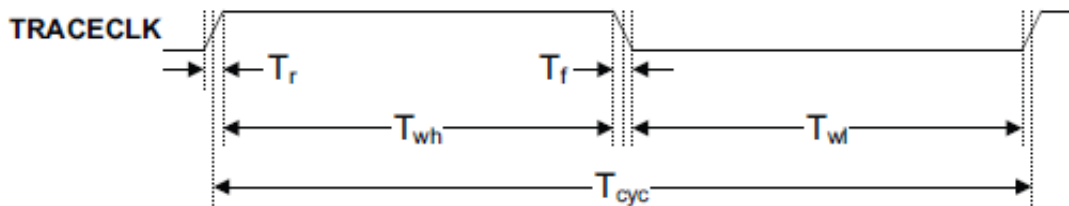


**Figure 3. TRACE_CLKOUT specifications**
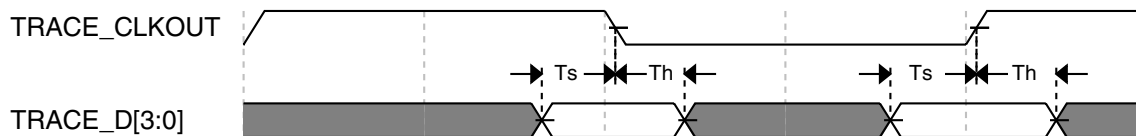


**Figure 4. Trace data specifications**

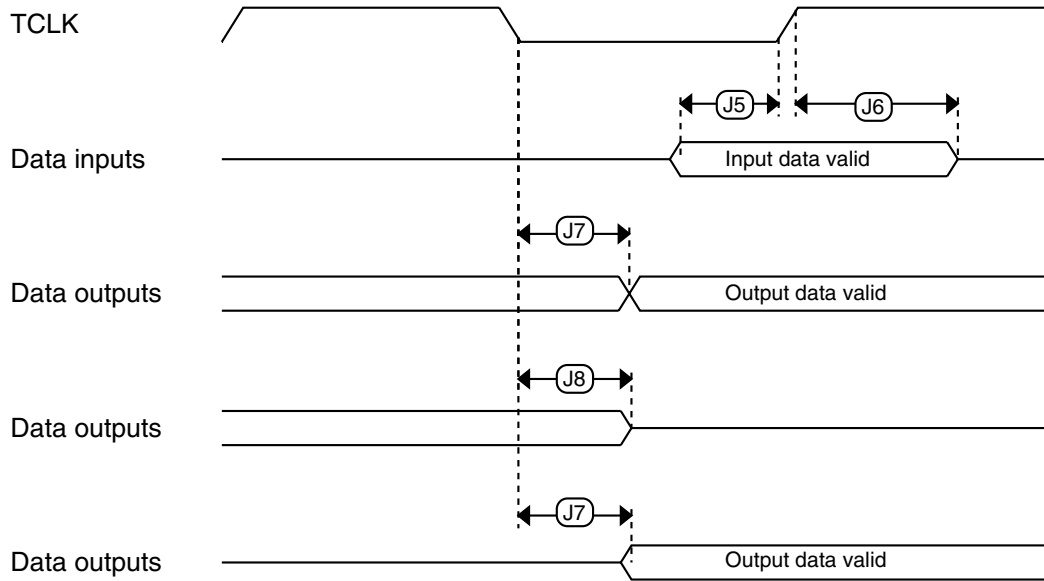**K53 Sub-Family Data Sheet Data Sheet, Rev. 7, 02/2013.**

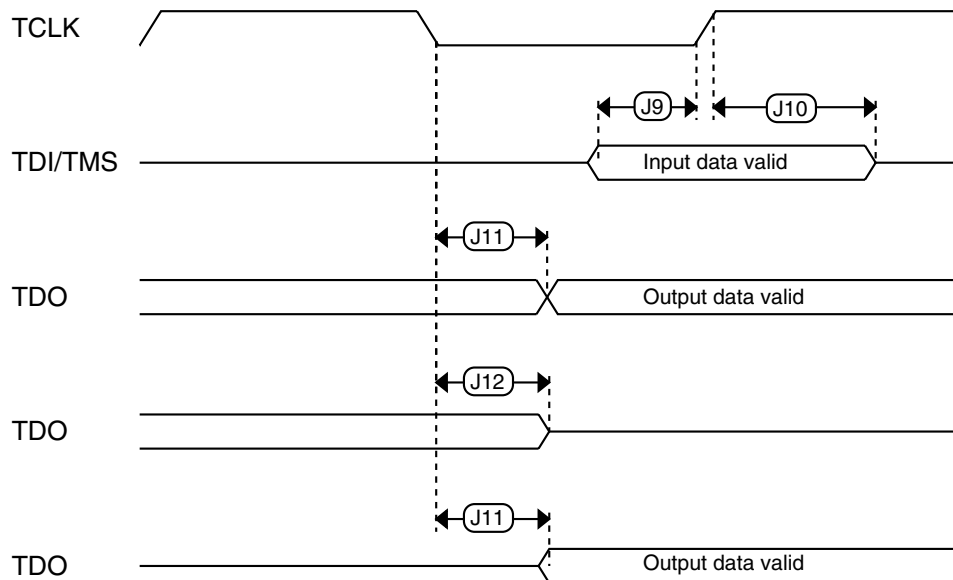**Figure 6. Boundary scan (JTAG) timing**



**Figure 7. Test Access Port timing**

## 6.3.3.2   32 kHz oscillator frequency specifications

**Table 19.   32 kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $f_{ec\_extal32}$ | Externally provided input clock frequency | — | 32.768 | — | kHz | 2 |
| $v_{ec\_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1.  Proper PC board layout procedures must be followed to achieve specifications.
2.  This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3.  The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

# 6.4   Memories and memory interfaces

## 6.4.1   Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.4.1.1   Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 20.   NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk256k}$ | Erase Block high-voltage time for 256 KB | — | 416 | 3616 | ms | 1 |

1.  Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2   Flash timing specifications — commands

**Table 21.   Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1blk256k}$ | Read 1s Block execution time<br><br>• 256 KB program/data flash | — | — | 1.7 | ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |

*Table continues on the next page...*

**Table 23. NVM reliability specifications (continued)**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 35 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 315 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 1.27 M | 6.4 M | — | writes | |
| $n_{nvmwree4k}$ | • EEPROM backup to FlexRAM ratio = 4096 | 10 M | 50 M | — | writes | |
| $n_{nvmwree32k}$ | • EEPROM backup to FlexRAM ratio = 32,768 | 80 M | 400 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ $T_j$ ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤ Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

## 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)

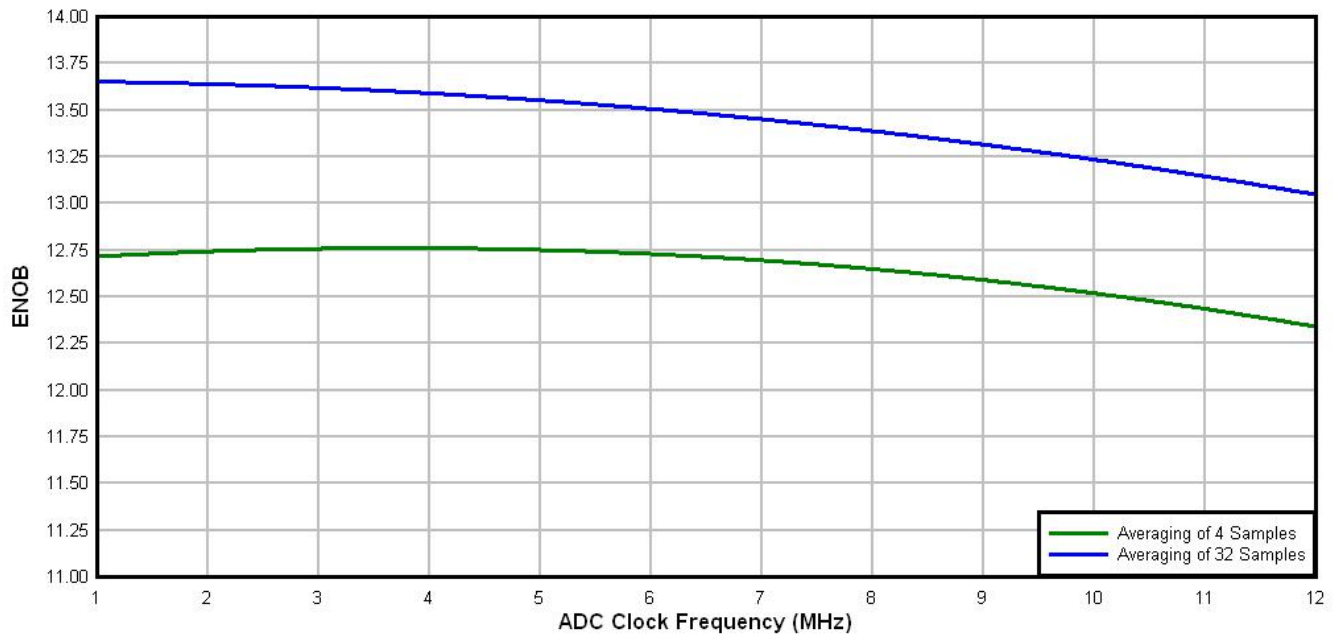**K53 Sub-Family Data Sheet Data Sheet, Rev. 7, 02/2013.**

## Figure 15. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

## 6.6.1.3   16-bit ADC with PGA operating conditions
### Table 29.   16-bit ADC with PGA operating conditions

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8 | — | 128 | — | kΩ | IN+ to IN-[4] |
| | | Gain = 16, 32 | — | 64 | — | | |
| | | Gain = 64 | — | 32 | — | | |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_{S}$ | ADC sampling time | | 1.25 | — | — | µs | 6 |

*Table continues on the next page...*

**Table 29. 16-bit ADC with PGA operating conditions (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br><br>No ADC hardware averaging<br><br>Continuous conversions enabled<br><br>Peripheral clock = 50 MHz | 18.484 | — | 450 | Ksps | 7 |
| | | 16 bit modes<br><br>No ADC hardware averaging<br><br>Continuous conversions enabled<br><br>Peripheral clock = 50 MHz | 37.037 | — | 250 | Ksps | 8 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}$/2
5. The analog source resistance ($R_{AS}$), external to MCU, should be kept as minimum as possible. Increased $R_{AS}$ causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for $F_{in}$=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

## 6.6.1.4  16-bit ADC with PGA characteristics
### Table 30.  16-bit ADC with PGA characteristics

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_PGA}$ | Supply current | Low power (ADC_PGA[PGALPb]=0) | — | 420 | 644 | µA | 2 |
| $I_{DC\_PGA}$ | Input DC current | | | $\frac{2}{R_{PGAD}}\left(\frac{\left(V_{REFPGA}\times0.583\right)-V_{CM}}{(Gain+1)}\right)$ | | A | 3 |
| | | Gain =1, $V_{REFPGA}$=1.2V, $V_{CM}$=0.5V | — | 1.54 | — | µA | |
| | | Gain =64, $V_{REFPGA}$=1.2V, $V_{CM}$=0.1V | — | 0.57 | — | µA | |

*Table continues on the next page...*

**Table 30. 16-bit ADC with PGA characteristics (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|--------|-------------|------------|------|---------|------|------|-------|
| ENOB | Effective number of bits | • Gain=1, Average=4 | 11.6 | 13.4 | — | bits | 16-bit differential mode, $f_{in}$=100Hz |
| | | • Gain=64, Average=4 | 7.2 | 9.6 | — | bits | |
| | | • Gain=1, Average=32 | 12.8 | 14.5 | — | bits | |
| | | • Gain=2, Average=32 | 11.0 | 14.3 | — | bits | |
| | | • Gain=4, Average=32 | 7.9 | 13.8 | — | bits | |
| | | • Gain=8, Average=32 | 7.3 | 13.1 | — | bits | |
| | | • Gain=16, Average=32 | 6.8 | 12.5 | — | bits | |
| | | • Gain=32, Average=32 | 6.8 | 11.5 | — | bits | |
| | | • Gain=64, Average=32 | 7.5 | 10.6 | — | bits | |
| SINAD | Signal-to-noise plus distortion ratio | See ENOB | $6.02 \times$ ENOB $+ 1.76$ | | | dB | |

1. Typical values assume $V_{DDA}$ =3.0V, Temp=25°C, $f_{ADCK}$=6MHz unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage ($V_{CM}$) and the PGA gain.
4. Gain = $2^{PGAG}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

## 6.6.2 CMP and 6-bit DAC electrical specifications

### Table 31. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS} - 0.3$ | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD} - 0.5$ | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |

*Table continues on the next page...*

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# 6.6.3.2   12-bit DAC operating behaviors

## Table 33.   12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 150 | µA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 700 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance load = 3 kΩ | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

### Table 38. TRIAMP limited range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $V_{OS}$ | Input offset voltage | — | ±3 | ±5 | mV | |
| $\alpha_{VOS}$ | Input offset voltage temperature coefficient | — | 4.8 | — | μV/C | |
| $I_{OS}$ | Input offset current | — | ±300 | ±600 | pA | |
| $I_{BIAS}$ | Input bias current | — | ±300 | ±600 | pA | |
| $R_{OUT}$ | Output AC impedance | — | — | 1500 | Ω | @ 100kHz, High speed mode |
| $|X_{IN}|$ | AC input impedance ($f_{IN}$=100kHz) | — | 159 | — | kΩ | |
| CMRR | Input common mode rejection ratio | — | 70 | — | dB | |
| PSRR | Power supply rejection ratio | — | 70 | — | dB | |
| SR | Slew rate ($\Delta V_{IN}$=500mV) — Low-power mode | 0.1 | — | — | V/μs | |
| SR | Slew rate ($\Delta V_{IN}$=500mV) — High speed mode | 1.5 | 3.5 | — | V/μs | |
| GBW | Unity gain bandwidth — Low-power mode 50pF | 0.15 | — | — | MHz | |
| GBW | Unity gain bandwidth — High speed mode 50pF | 1 | — | — | MHz | |
| $A_V$ | DC open-loop voltage gain | 80 | — | — | dB | |
| GM | Gain margin | — | 20 | — | dB | |
| PM | Phase margin | 60 | 69 | — | deg | |

## 6.6.7 Voltage reference electrical specifications

### Table 39. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1, 2 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified $C_L$ value over the operating temperature range of the device.

### Table 40. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C | 1.1915 | 1.195 | 1.1977 | V | |
| $V_{out}$ | Voltage reference output — factory trim | 1.1584 | — | 1.2376 | V | |
| $V_{step}$ | Voltage reference trim step | — | 0.5 | — | mV | |

*Table continues on the next page...*

## Table 40.   VREF full-range operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{tdrift}$ | Temperature drift (Vmax -Vmin across the full temperature range) | — | — | 80 | mV | |
| $I_{bg}$ | Bandgap only current | — | — | 80 | μA | 1 |
| $I_{lp}$ | Low-power buffer current | — | — | 360 | uA | 1 |
| $I_{hp}$ | High-power buffer current | — | — | 1 | mA | 1 |
| $\Delta V_{LOAD}$ | Load regulation | | | | mV | 1, 2 |
| | • current = + 1.0 mA | — | 2 | — | | |
| | • current = - 1.0 mA | — | 5 | — | | |
| $T_{stup}$ | Buffer startup time | — | — | 100 | μs | |
| $V_{vdrift}$ | Voltage drift (Vmax -Vmin across the full voltage range) | — | 2 | — | mV | 1 |

1.  See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2.  Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

## Table 41.   VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_A$ | Temperature | 0 | 50 | °C | |

## Table 42.   VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim | 1.173 | 1.225 | V | |

# 6.7   Timers

See General switching specifications.

# 6.8   Communication interfaces

## 6.8.1   Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.
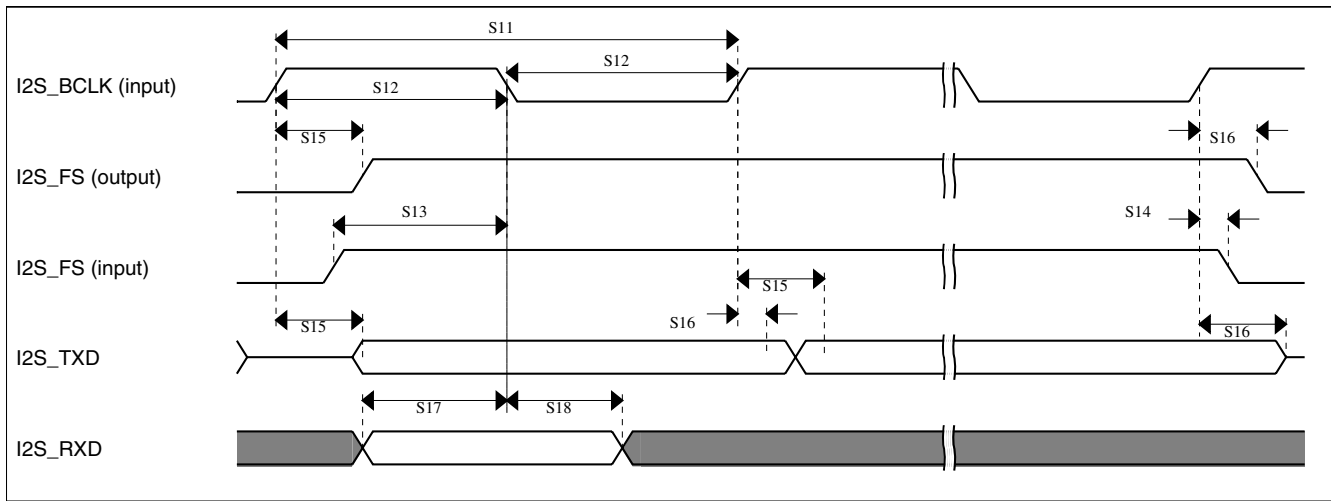
**Figure 29. I²S timing — slave modes**

**Table 55.  I²S master mode timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
|  | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 2 x $t_{SYS}$ |  | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_BCLK cycle time | 5 x $t_{SYS}$ | — | ns |
| S4 | I2S_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_BCLK to I2S_FS output valid | — | 15 | ns |
| S6 | I2S_BCLK to I2S_FS output invalid | -4.3 | — | ns |
| S7 | I2S_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_BCLK to I2S_TXD invalid | -4.6 | — | ns |
| S9 | I2S_RXD/I2S_FS input setup before I2S_BCLK | 23.9 | — | ns |
| S10 | I2S_RXD/I2S_FS input hold after I2S_BCLK | 0 | — | ns |

**Table 56.  I²S slave mode timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
|  | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_BCLK cycle time (input) | 8 x $t_{SYS}$ | — | ns |
| S12 | I2S_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_FS input setup before I2S_BCLK | 10 | — | ns |
| S14 | I2S_FS input hold after I2S_BCLK | 3.5 | — | ns |
| S15 | I2S_BCLK to I2S_TXD/I2S_FS output valid | — | 28.6 | ns |
| S16 | I2S_BCLK to I2S_TXD/I2S_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_BCLK | 2 | — | ns |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 80 | H11 | PTA29 | DISABLED | | PTA29 | | | MII0_COL | FB_AD19 | | | |
| 81 | H10 | PTB0/ LLWU_P5 | LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | RMII0_MDIO/ MII0_MDIO | | FTM1_QD_ PHA | LCD_P0 | |
| 82 | H9 | PTB1 | LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | PTB1 | I2C0_SDA | FTM1_CH1 | RMII0_MDC/ MII0_MDC | | FTM1_QD_ PHB | LCD_P1 | |
| 83 | G12 | PTB2 | LCD_P2/ ADC0_SE12/ TSI0_CH7 | LCD_P2/ ADC0_SE12/ TSI0_CH7 | PTB2 | I2C0_SCL | UART0_RTS_ b | ENET0_1588_ TMR0 | | FTM0_FLT3 | LCD_P2 | |
| 84 | G11 | PTB3 | LCD_P3/ ADC0_SE13/ TSI0_CH8 | LCD_P3/ ADC0_SE13/ TSI0_CH8 | PTB3 | I2C0_SDA | UART0_CTS_ b | ENET0_1588_ TMR1 | | FTM0_FLT0 | LCD_P3 | |
| 85 | G10 | PTB4 | LCD_P4/ ADC1_SE10 | LCD_P4/ ADC1_SE10 | PTB4 | | | ENET0_1588_ TMR2 | | FTM1_FLT0 | LCD_P4 | |
| 86 | G9 | PTB5 | LCD_P5/ ADC1_SE11 | LCD_P5/ ADC1_SE11 | PTB5 | | | ENET0_1588_ TMR3 | | FTM2_FLT0 | LCD_P5 | |
| 87 | F12 | PTB6 | LCD_P6/ ADC1_SE12 | LCD_P6/ ADC1_SE12 | PTB6 | | | | | | LCD_P6 | |
| 88 | F11 | PTB7 | LCD_P7/ ADC1_SE13 | LCD_P7/ ADC1_SE13 | PTB7 | | | | | | LCD_P7 | |
| 89 | F10 | PTB8 | LCD_P8 | LCD_P8 | PTB8 | | UART3_RTS_ b | | | | LCD_P8 | |
| 90 | F9 | PTB9 | LCD_P9 | LCD_P9 | PTB9 | SPI1_PCS1 | UART3_CTS_ b | | | | LCD_P9 | |
| 91 | E12 | PTB10 | LCD_P10/ ADC1_SE14 | LCD_P10/ ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | | | FTM0_FLT1 | LCD_P10 | |
| 92 | E11 | PTB11 | LCD_P11/ ADC1_SE15 | LCD_P11/ ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | | | FTM0_FLT2 | LCD_P11 | |
| 93 | H7 | VSS | VSS | VSS | | | | | | | | |
| 94 | F5 | VDD | VDD | VDD | | | | | | | | |
| 95 | E10 | PTB16 | LCD_P12/ TSI0_CH9 | LCD_P12/ TSI0_CH9 | PTB16 | SPI1_SOUT | UART0_RX | | | EWM_IN | LCD_P12 | |
| 96 | E9 | PTB17 | LCD_P13/ TSI0_CH10 | LCD_P13/ TSI0_CH10 | PTB17 | SPI1_SIN | UART0_TX | | | EWM_OUT_b | LCD_P13 | |
| 97 | D12 | PTB18 | LCD_P14/ TSI0_CH11 | LCD_P14/ TSI0_CH11 | PTB18 | | FTM2_CH0 | I2S0_TX_ BCLK | | FTM2_QD_ PHA | LCD_P14 | |
| 98 | D11 | PTB19 | LCD_P15/ TSI0_CH12 | LCD_P15/ TSI0_CH12 | PTB19 | | FTM2_CH1 | I2S0_TX_FS | | FTM2_QD_ PHB | LCD_P15 | |
| 99 | D10 | PTB20 | LCD_P16 | LCD_P16 | PTB20 | SPI2_PCS0 | | | | CMP0_OUT | LCD_P16 | |
| 100 | D9 | PTB21 | LCD_P17 | LCD_P17 | PTB21 | SPI2_SCK | | | | CMP1_OUT | LCD_P17 | |
| 101 | C12 | PTB22 | LCD_P18 | LCD_P18 | PTB22 | SPI2_SOUT | | | | CMP2_OUT | LCD_P18 | |
| 102 | C11 | PTB23 | LCD_P19 | LCD_P19 | PTB23 | SPI2_SIN | SPI0_PCS5 | | | | LCD_P19 | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 127 | C5 | PTC18 | LCD_P38 | LCD_P38 | PTC18 | | UART3_RTS_b | ENET0_1588_TMR2 | | | LCD_P38 | |
| 128 | B5 | PTC19 | LCD_P39 | LCD_P39 | PTC19 | | UART3_CTS_b | ENET0_1588_TMR3 | | | LCD_P39 | |
| 129 | A5 | PTD0/ LLWU_P12 | LCD_P40 | LCD_P40 | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_RTS_b | | | | LCD_P40 | |
| 130 | D4 | PTD1 | LCD_P41/ ADC0_SE5b | LCD_P41/ ADC0_SE5b | PTD1 | SPI0_SCK | UART2_CTS_b | | | | LCD_P41 | |
| 131 | C4 | PTD2/ LLWU_P13 | LCD_P42 | LCD_P42 | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | | | | LCD_P42 | |
| 132 | B4 | PTD3 | LCD_P43 | LCD_P43 | PTD3 | SPI0_SIN | UART2_TX | | | | LCD_P43 | |
| 133 | A4 | PTD4/ LLWU_P14 | LCD_P44 | LCD_P44 | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_RTS_b | FTM0_CH4 | | EWM_IN | LCD_P44 | |
| 134 | A3 | PTD5 | LCD_P45/ ADC0_SE6b | LCD_P45/ ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_CTS_b | FTM0_CH5 | | EWM_OUT_b | LCD_P45 | |
| 135 | A2 | PTD6/ LLWU_P15 | LCD_P46/ ADC0_SE7b | LCD_P46/ ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | | FTM0_FLT0 | LCD_P46 | |
| 136 | M10 | VSS | VSS | VSS | | | | | | | | |
| 137 | F8 | VDD | VDD | VDD | | | | | | | | |
| 138 | A1 | PTD7 | LCD_P47 | LCD_P47 | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | LCD_P47 | |
| 139 | B3 | PTD10 | DISABLED | | PTD10 | | UART5_RTS_b | | FB_AD9 | | | |
| 140 | B2 | PTD11 | DISABLED | | PTD11 | SPI2_PCS0 | UART5_CTS_b | SDHC0_CLKIN | FB_AD8 | | | |
| 141 | B1 | PTD12 | DISABLED | | PTD12 | SPI2_SCK | | SDHC0_D4 | FB_AD7 | | | |
| 142 | C3 | PTD13 | DISABLED | | PTD13 | SPI2_SOUT | | SDHC0_D5 | FB_AD6 | | | |
| 143 | C2 | PTD14 | DISABLED | | PTD14 | SPI2_SIN | | SDHC0_D6 | FB_AD5 | | | |
| 144 | C1 | PTD15 | DISABLED | | PTD15 | SPI2_PCS1 | | SDHC0_D7 | FB_RW_b | | | |

## 8.2  K53 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |   |
|---|---|---|---|---|---|---|---|---|---|----|----|----|---|
| A | PTD7 | PTD6 | PTD5 | PTD4 | PTD0 | PTC16 | PTC12 | PTC8 | PTC4 | VCAP1 | PTC3 | PTC2 | A |
| B | PTD12 | PTD11 | PTD10 | PTD3 | PTC19 | PTC15 | PTC11 | PTC7 | VLL1 | VCAP2 | PTC1 | PTC0 | B |
| C | PTD15 | PTD14 | PTD13 | PTD2 | PTC18 | PTC14 | PTC10 | PTC6 | VLL2 | VLL3 | PTB23 | PTB22 | C |
| D | PTE2 | PTE1 | PTE0 | PTD1 | PTC17 | PTC13 | PTC9 | PTC5 | PTB21 | PTB20 | PTB19 | PTB18 | D |
| E | PTE6 | PTE5 | PTE4 | PTE3 | VDD | VDD | VDD | VDD | PTB17 | PTB16 | PTB11 | PTB10 | E |
| F | PTE10 | PTE9 | PTE8 | PTE7 | VDD | VSS | VSS | VDD | PTB9 | PTB8 | PTB7 | PTB6 | F |
| G | VOUT33 | VREGIN | PTE12 | PTE11 | VREFH | VREFL | VSS | VSS | PTB5 | PTB4 | PTB3 | PTB2 | G |
| H | USB0_DP | USB0_DM | VSS | PTE28 | VDDA | VSSA | VSS | VSS | PTB1 | PTB0 | PTA29 | PTA28 | H |
| J | ADC0_DP1/ OP0_DP0 | ADC0_DM1/ OP0_DM0 | ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1 | DAC1_OUT/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5 | PTA0 | PTA1 | PTA6 | PTA7 | PTA13 | PTA27 | PTA26 | PTA25 | J |
| K | ADC1_DP1/ OP1_DP0/ OP1_DM1 | ADC1_DM1/ OP1_DM0 | ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4 | TRI1_OUT/ CMP2_IN5/ ADC1_SE22 | PTA2 | PTA3 | PTA8 | PTA12 | PTA16 | PTA17 | PTA24 | K |
| L | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | TRI0_OUT/ OP1_DM2 | TRI0_DM | TRI1_DM | VBAT | PTA4 | PTA9 | PTA11 | PTA14 | PTA15 | RESET_b | L |
| M | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | TRI0_DP | TRI1_DP | EXTAL32 | XTAL32 | PTA5 | PTA10 | VSS | PTA19 | PTA18 | M |
|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |   |

**Figure 31. K53 144 MAPBGA Pinout Diagram**

# 9  Revision History

The following table provides a revision history for this document.

**Table 59.   Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 3/2011 | Initial public revision |

*Table continues on the next page...*