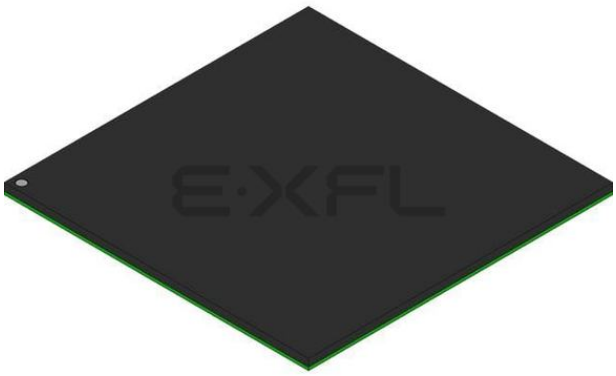

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC 603e |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 200MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 352-LBGA |
| Supplier Device Package | 352-TBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=xpc8240lvv200e |

### 1.4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8240.

**Table 2. Recommended Operating Conditions [1]**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ | 2.5 ± 5% | V | 4, 6 |
| Supply voltage for PCI and standard bus standards | | $OV_{DD}$ | 3.3 ± 0.3 | V | 6 |
| Supply voltages for memory bus drivers | | $GV_{DD}$ | 3.3 ± 5% | V | 8 |
| PLL supply voltage—CPU core logic | | $AV_{DD}$ | 2.5 ± 5% | V | 4, 6 |
| PLL supply voltage—peripheral logic | | $AV_{DD}2$ | 2.5 ± 5% | V | 4, 7 |
| DLL supply voltage | | $LAV_{DD}$ | 2.5 ± 5% | V | 4, 7 |
| PCI reference | | $LV_{DD}$ | 5.0 ± 5% | V | 9, 10 |
| | | | 3.3 ± 0.3 | V | 9, 10 |
| Input voltage | $LV_{DD}$ input-tolerant signals | $V_{in}$ | 0 to 3.6 or 5.75 | V | 2, 3 |
| | All other inputs | | 0 to 3.6 | V | 5 |
| Die-junction temperature | | $T_j$ | 0 to 105 | °C | |

**Notes:**

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. These signals are designed to withstand $LV_{DD}$ + 0.5 V DC when $LV_{DD}$ is connected to a 3.3- or 5.0-V DC power supply.
3. $LV_{DD}$ input tolerant signals: PCI interface, PIC control, and OSC_IN signals.
4. See Section 1.9, “Ordering Information,” for details on a modified voltage ($V_{DD}$) version device.

**Cautions:**

5. Input voltage ($V_{in}$) must not be greater than the supply voltage ($V_{DD}$/$AV_{DD}$/$AV_{DD}2$/$LAV_{DD}$) by more than 2.5 V at all times, including during power-on reset.
6. $OV_{DD}$ must not exceed $V_{DD}$/$AV_{DD}$/$AV_{DD}2$/$LAV_{DD}$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. $V_{DD}$/$AV_{DD}$/$AV_{DD}2$/$LAV_{DD}$ must not exceed $OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. $GV_{DD}$ must not exceed $V_{DD}$/$AV_{DD}$/$AV_{DD}2$/$LAV_{DD}$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. $LV_{DD}$ must not exceed $V_{DD}$/$AV_{DD}$/$AV_{DD}2$/$LAV_{DD}$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. $LV_{DD}$ must not exceed $OV_{DD}$ by more than 3.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

**Table 3. DC Electrical Specifications (continued)**

At recommended operating conditions (see Table 2)

| Characteristic | Condition [3] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Capacitance | $V_{in}$ = 0 V, f = 1 MHz | $C_{in}$ | — | 7.0 | pF |

**Notes:**
1. See Table 17 for pins with internal pull-up resistors.
2. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 17.
3. These specifications are for the default driver strengths indicated in Table 4.
4. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal $OV_{DD}/LV_{DD}$, and $V_{DD}$ or both $OV_{DD}/LV_{DD}$ and $V_{DD}$ must vary in the same direction.
5. The minimum input high voltage is not compliant with the *PCI Local Bus Specification* (Rev 2.1), which specifies $0.5 \times OV_{DD}$ for minimum input high voltage.

## 1.4.1.4 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 17. The values are from the MPC8240 IBIS model (v1.1 IBIS, v1.2 file) and are untested. For additional detailed information, see the complete IBIS model listing at: http://www.mot.com/SPS/PowerPC/teksupport/tools/IBIS/kahlua_1.ibs.txt

**Table 4. Drive Capability of MPC8240 Output Pins**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | $I_{OH}$ | $I_{OL}$ | Unit | Notes |
|---|---|---|---|---|---|---|
| DRV_STD | 20 | $OV_{DD}$ = 3.3 V | 36.7 | 30.0 | mA | 2, 4 |
| | 40 (default) | $OV_{DD}$ = 3.3 V | 18.7 | 15.0 | mA | 2, 4 |
| DRV_PCI | 25 | $OV_{DD}$ = 3.3 V | 11.0 | 20.6 | mA | 1, 3 |
| | 50 (default) | $OV_{DD}$ = 3.3 V | 5.6 | 10.3 | mA | 1, 3 |
| DRV_MEM_ADDR DRV_PCI_CLK | 8 (default) | $GV_{DD}$ = 3.3 V | 89.0 | 76.3 | mA | 2, 4 |
| | 13.3 | $GV_{DD}$ = 3.3 V | 55.9 | 46.4 | mA | 2, 4 |
| | 20 | $GV_{DD}$ = 3.3 V | 36.7 | 30.0 | mA | 2, 4 |
| | 40 | $GV_{DD}$ = 3.3 V | 18.7 | 15.0 | mA | 2, 4 |
| DRV_MEM_DATA | 20 (default) | $GV_{DD}$ = 3.3 V | 36.7 | 30.0 | mA | 2, 4 |
| | 40 | $GV_{DD}$ = 3.3 V | 18.7 | 15.0 | mA | 2, 4 |

**Notes:**
1. For DRV_PCI, $I_{OH}$ read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries' current values that correspond to the PCI $V_{OH} = 2.97 = 0.9 \times OV_{DD}$ ($OV_{DD}$ = 3.3 V) where table entry voltage = $OV_{DD}$ – PCI $V_{OH}$.
2. For all others with $GV_{DD}$ or $OV_{DD}$ = 3.3 V, $I_{OH}$ read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry thatcorresponds to the $V_{OH}$ = 2.4 V where table entry voltage = $GV_{DD}/OV_{DD} – V_{OH}$.
3. For DRV_PCI, $I_{OL}$ read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI $V_{OL} = 0.1 \times OV_{DD}$ ($OV_{DD}$ = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.

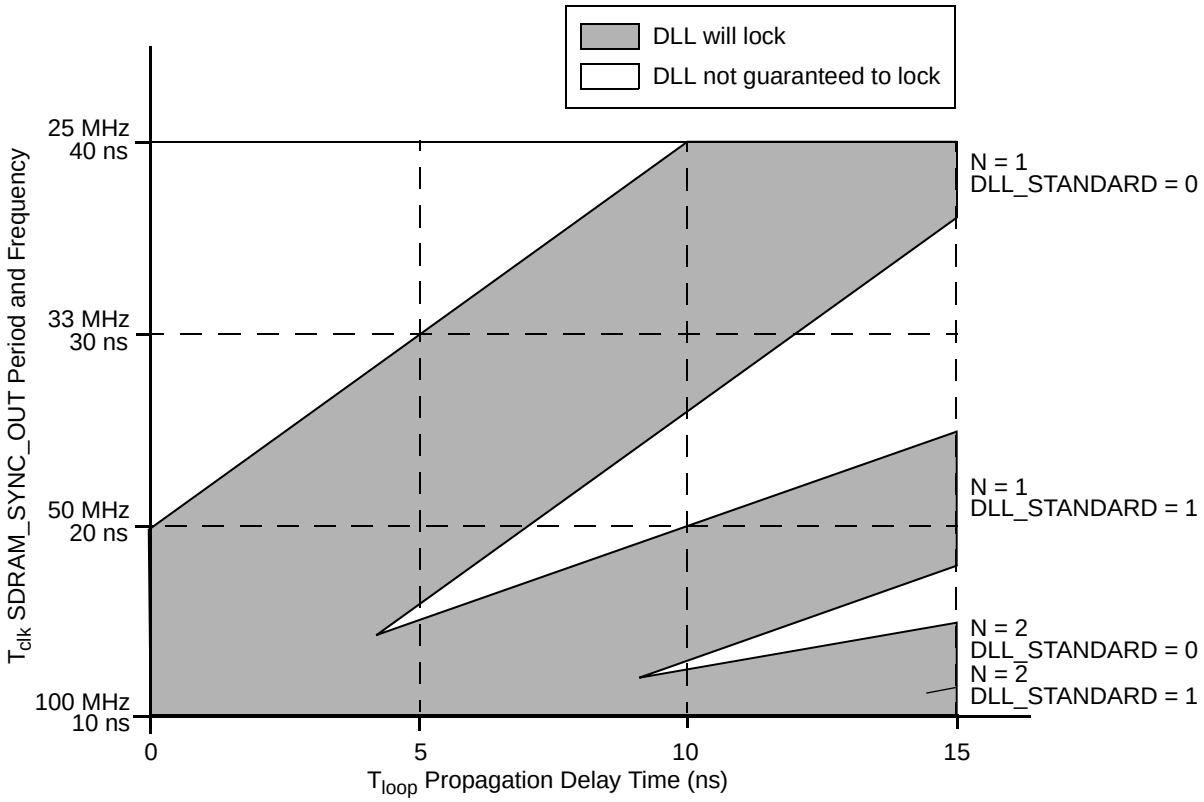



**Figure 7. DLL Locking Range Loop Delay vs. Frequency of Operation**

### 1.4.2.3 Input AC Timing Specifications

Table 8 provides the input AC timing specifications. See Figure 8 and Figure 9 for the input-output timing diagrams referenced to SDRAM_SYNC_IN and PCI_SYNC_IN, respectively.

**Table 8. Input AC Timing Specifications**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 10a | PCI input signals valid to PCI_SYNC_IN (input setup) | 2.0 | — | ns | 2, 3 |
| 10b1 | Memory control and data input signals in flow through mode valid to SDRAM_SYNC_IN (input setup) | 3.0 | — | ns | 1, 3 |
| 10b2 | Memory control and data input signals in registered/in-line mode valid to SDRAM_SYNC_IN (input setup) | 2.5 | — | ns | 1, 3 |
| 10b3 | Memory control and data signals accessing non-DRAM valid to SDRAM_SYNC_IN (input setup) | 3.0 | — | ns | 1, 3 |
| 10c | PIC, miscellaneous debug input signals valid to SDRAM_SYNC_IN (input setup) | 3.0 | — | ns | 1, 3 |
| 10d | $I^2C$ input signals valid to SDRAM_SYNC_IN (input setup) | 2.0 | — | ns | 1, 3 |
| 10e | Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup) | $9 \times t_{CLK}$ | — | ns | 1, 3–5 |

**Table 8. Input AC Timing Specifications (continued)**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 11a | PCI_SYNC_IN (SDRAM_SYNC_IN) to inputs invalid (input hold) | 1.0 | — | ns | 1, 2, 3 |
| 11b | $\overline{\text{HRST\_CPU}}/\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold) | 0 | — | ns | 1, 3, 5 |

**Notes:**

1. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 8.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 9.
3. Input timings are measured at the pin.
4. $t_{CLK}$ is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}/\overline{\text{HRST\_CTRL}}$ signal. See Figure 10.

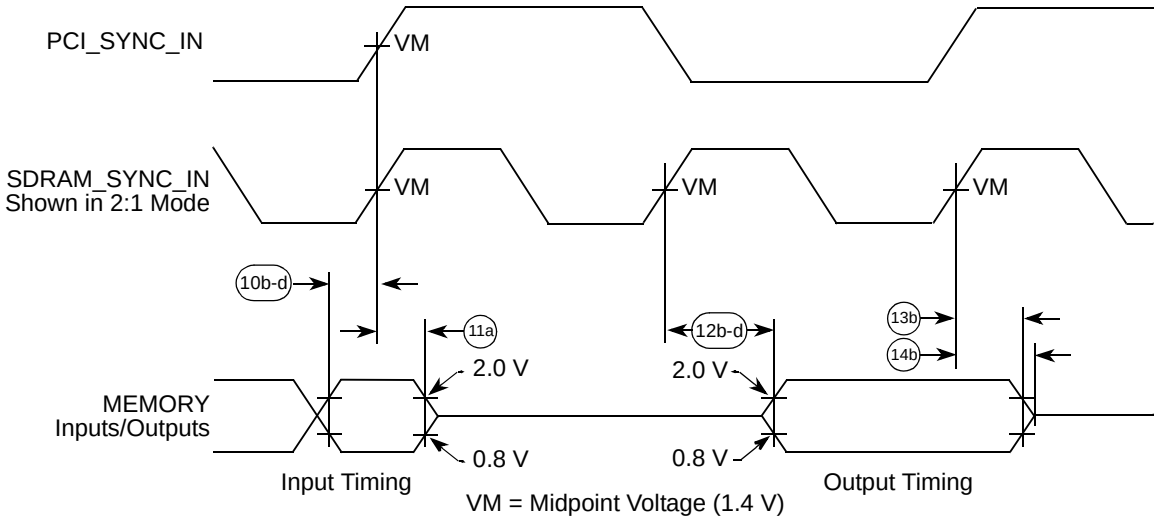



**Figure 8. Input-Output Timing Diagram Referenced to SDRAM_SYNC_IN**

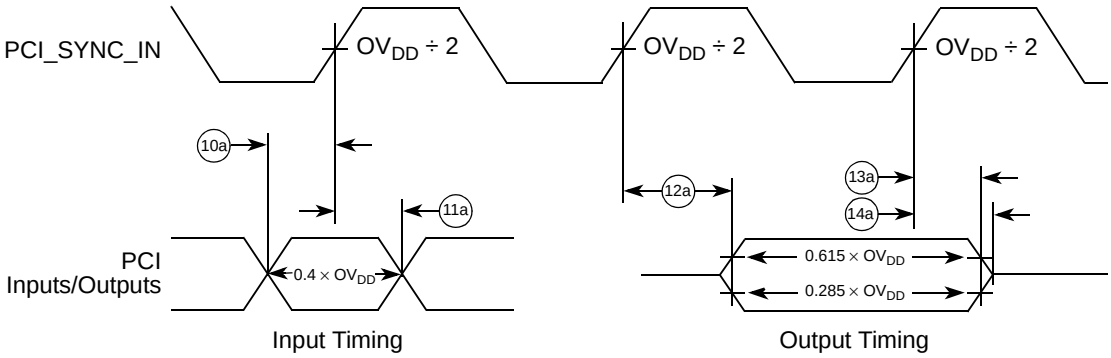



**Figure 9. Input-Output Timing Diagram Referenced to PCI_SYNC_IN**

Figure 10 shows the input timing diagram for mode select signals.

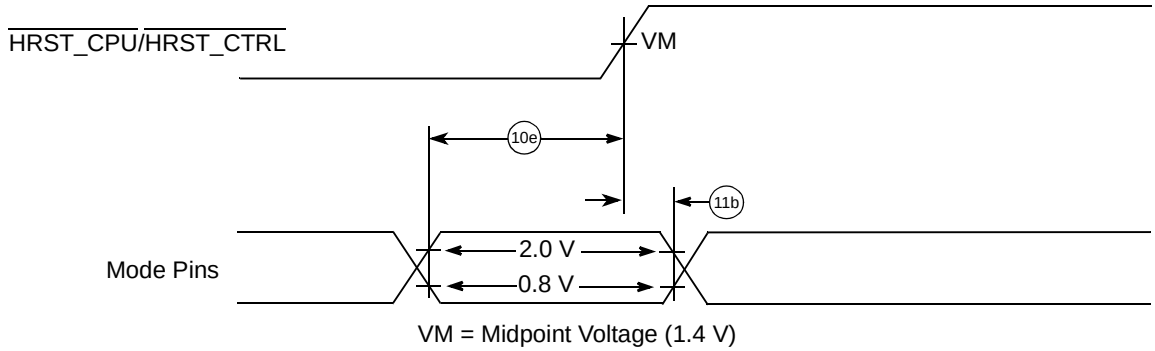



**Figure 10. Input Timing Diagram for Mode Select Signals**

### 1.4.2.4 Output AC Timing Specification

Table 9 provides the processor bus AC timing specifications for the MPC8240. See Figure 8 and Figure 9 for the input-output timing diagrams referenced to SDRAM_SYNC_IN and PCI_SYNC_IN, respectively. Figure 11 shows the AC test load for the MPC8240.

**Table 9. Output AC Timing Specifications**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic [3, 6] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 12a | PCI_SYNC_IN to output valid, 66 MHz PCI, with $\overline{\text{MCP}}$ in the default logic 1 state and CKE pulled down to logic 0 state (see Figure 10) | — | 6.0 | ns | 2, 4 |
| | PCI_SYNC_IN to output valid, 33 MHz PCI, with $\overline{\text{MCP}}$ and CKE in the default logic 1 state (see Figure 10) | — | 8.0 | ns | 2, 4 |
| 12b1 | SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing DRAM in flow-through mode) | — | 7.0 | ns | 1 |
| 12b2 | SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing DRAM in registered mode) | — | 6.0 | ns | 1 |
| 12b3 | SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing non-DRAM) | — | 7.0 | ns | 1 |
| 12c | SDRAM_SYNC_IN to output valid (for all others) | — | 7.0 | ns | 1 |
| 12d | SDRAM_SYNC_IN to output valid (for $I^2C$) | — | 5.0 | ns | 1 |
| 13a | Output hold, 66 MHz PCI, with $\overline{\text{MCP}}$ in the default logic 1 state and CKE pulled down to logic 0 state (see Figure 10) | 1.0 | — | ns | 2, 4, 5 |
| | Output hold, 33 MHz PCI, with $\overline{\text{MCP}}$ and CKE in the default logic 1 state (see Figure 10) | 2.0 | — | ns | 2, 4, 5 |
| 13b | Output hold (all others) | 0 | — | ns | 1 |
| 14a | PCI_SYNC_IN to output high impedance (for PCI) | — | 14.0 | ns | 2, 4 |

**Table 9. Output AC Timing Specifications (continued)**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic [3, 6] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 14b | SDRAM_SYNC_IN to output high impedance (for all others) | — | 4.0 | ns | 1 |

**Notes:**

1. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 8.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times OV_{DD}$ or $0.615 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 9.
3. All output timings assume a purely resistive 50-Ω load (see Figure 11). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[0:3], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[0:31], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
5. PCI hold times can be varied; see Section 1.4.2.4.1, “PCI Signal Output Hold Timing,” for information on programmable PCI output hold times. The values shown for item 13a are for PCI compliance.
6. These specifications are for the default driver strengths indicated in Table 4.

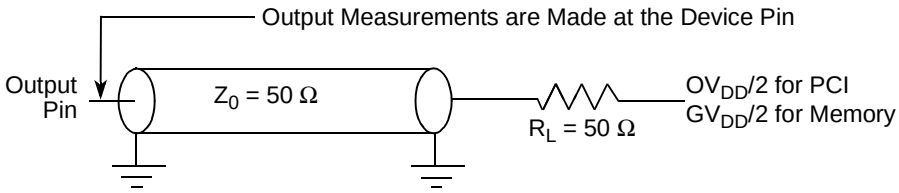



**Figure 11. AC Test Load for the MPC8240**

### 1.4.2.4.1 PCI Signal Output Hold Timing

In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8240 has a programmable output hold delay for PCI signals. The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals. Further output hold delay values are available through programming the PCI_HOLD_DEL value of the PMCR2 configuration register.

**Table 12. MPC8240 Maximum $I^2C$ Input Frequency (continued)**

| FDR Hex [2] | Divider [3] (Dec) | Maximum $I^2C$ Input Frequency [1] | | |
|---|---|---|---|---|
| | | SDRAM_CLK @ 33 MHz | SDRAM_CLK @ 50 MHz | SDRAM_CLK @ 100 MHz |
| 14, 15 | 9216, 10240 | 21 | 32 | 64 |
| 16, 17, 3A, 3B, 3C, 3D | 12288, 14336, 15360, 16384, 20480, 24576 | 16 | 24 | 48 |
| 18, 19 | 18432, 20480 | 10 | 16 | 32 |
| 1A, 1B, 3E, 3F | 24576, 28672, 30720, 32768 | 8 | 12 | 24 |
| 1C, 1D | 36864, 40960 | 5 | 8 | 16 |
| 1E, 1F | 49152, 61440 | 4 | 6 | 12 |

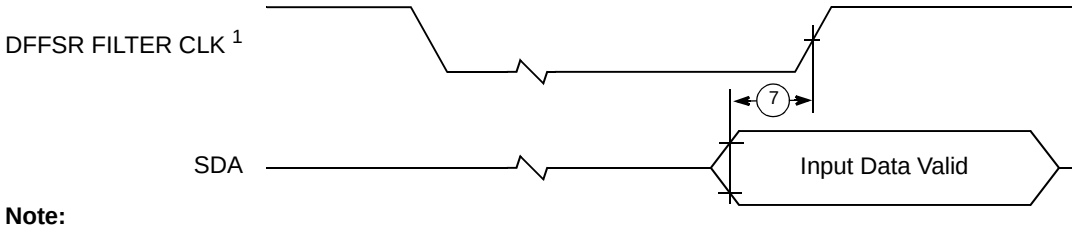
**Notes:**
1. Values are in KHz, unless otherwise specified.
2. FDR Hex and Divider (Dec) values are listed in corresponding order.
3. Multiple Divider (Dec) values will generate the same input frequency, but each Divider (Dec) value will generate a unique output frequency as shown in Table 13.

Table 13 provides the $I^2C$ output AC timing specifications for the MPC8240.

**Table 13. $I^2C$ Output AC Timing Specifications**

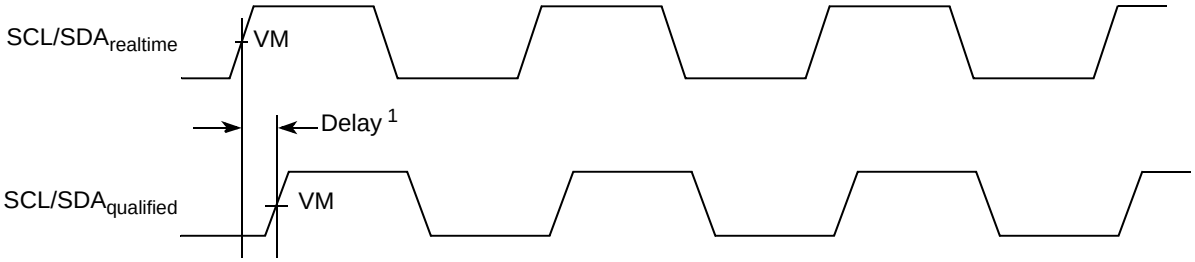
At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 1 | Start condition hold time | (FDR[5] == 0) × ($D_{FDR}$/16)/2N + (FDR[5] == 1) × ($D_{FDR}$/16)/2M | — | CLKs | 1, 2, 5 |
| 2 | Clock low period | $D_{FDR}$/2 | — | CLKs | 1, 2, 5 |
| 3 | SCL/SDA rise time (from 0.5 to 2.4 V) | — | — | ms | 3 |
| 4 | Data hold time | 8.0 + (16 × $2^{FDR[4:2]}$) × (5 – 4({FDR[5],FDR[1]} == b'10) – 3({FDR[5],FDR[1]} == b'11) – 2({FDR[5],FDR[1]} == b'00) – 1({FDR[5],FDR[1]} == b'01)) | — | CLKs | 1, 2, 5 |
| 5 | SCL/SDA fall time (from 2.4 to 0.5 V) | — | < 5 | ns | 4 |
| 6 | Clock high time | $D_{FDR}$/2 | — | CLKs | 1, 2, 5 |
| 7 | Data setup time (MPC8240 as a master only) | ($D_{FDR}$/2) – (Output data hold time) | — | CLKs | 1, 5 |
| 8 | Start condition setup time (for repeated start condition only) | $D_{FDR}$ + (Output start condition hold time) | — | CLKs | 1, 2, 5 |




**Note:**
1. DFFSR filter clock is the SDRAM_CLK clock times DFFSR value.

**Figure 15. I²C Timing Diagram III**




**Note:**
1. The delay is the local memory clock times DFFSR times 2 plus 1 local memory clock.

**Figure 16. I²C Timing Diagram IV (Qualified Signal)**

### 1.4.2.6 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8240.

**Table 14. PIC Serial Interrupt Mode AC Timing Specifications**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 1 | S_CLK frequency | 1/14 SDRAM_SYNC_IN | 1/2 SDRAM_SYNC_IN | MHz | 1 |
| 2 | S_CLK duty cycle | 40 | 60 | % | |
| 3 | S_CLK output valid time | — | 6 | ns | |
| 4 | Output hold time | 0 | — | ns | |
| 5 | $\overline{\text{S\_FRAME}}$, S_RST output valid time | — | 1 *sys_logic_clk* period + 6 | ns | 2 |
| 6 | S_INT input setup time to S_CLK | 1 *sys_logic_clk* period + 2 | — | ns | 2 |

### 1.4.2.7 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8240 while in the JTAG operating mode.

**Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)**

At recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V

| Num | Characteristic [4] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| | TCK frequency of operation | 0 | 25 | MHz | |
| 1 | TCK cycle time | 40 | — | ns | |
| 2 | TCK clock pulse width measured at 1.5 V | 20 | — | ns | |
| 3 | TCK rise and fall times | 0 | 3 | ns | |
| 4 | $\overline{\text{TRST}}$ setup time to TCK falling edge | 10 | — | ns | 1 |
| 5 | $\overline{\text{TRST}}$ assert time | 10 | — | ns | |
| 6 | Input data setup time | 5 | — | ns | 2 |
| 7 | Input data hold time | 15 | — | ns | 2 |
| 8 | TCK to output data valid | 0 | 30 | ns | 3 |
| 9 | TCK to output high impedance | 0 | 30 | ns | 3 |
| 10 | TMS, TDI data setup time | 5 | — | ns | |
| 11 | TMS, TDI data hold time | 15 | — | ns | |
| 12 | TCK to TDO data valid | 0 | 15 | ns | |
| 13 | TCK to TDO high impedance | 0 | 15 | ns | |

**Notes:**
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test (other than TDI and TMS) signal input timing with respect to TCK.
3. Non-test (other than TDO) signal output timing with respect to TCK.
4. Timings are independent of the system clock (PCI_SYNC_IN).

Figure 19 shows the JTAG clock input timing diagram.

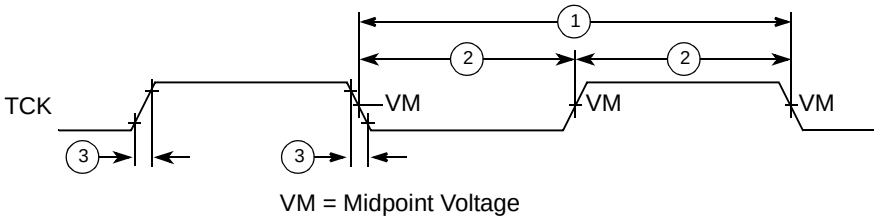



**Figure 19. JTAG Clock Input Timing Diagram**

### 1.4.3 Thermal Characteristics

Table 16 provides the package thermal characteristics for the MPC8240.

**Table 16. Package Thermal Characteristics**

| Characteristic [1] | Symbol | Value | Unit |
|---|---|---|---|
| Die junction-to-case thermal resistance | $R_{\theta JC}$ | 1.8 | °C/W |
| Die junction-to-board thermal resistance | $R_{\theta JB}$ | 4.8 | °C/W |

**Note:**
1. Refer to Section 1.7, “System Design Information,” for details about thermal management.

## 1.5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC8240, 352 TBGA package.

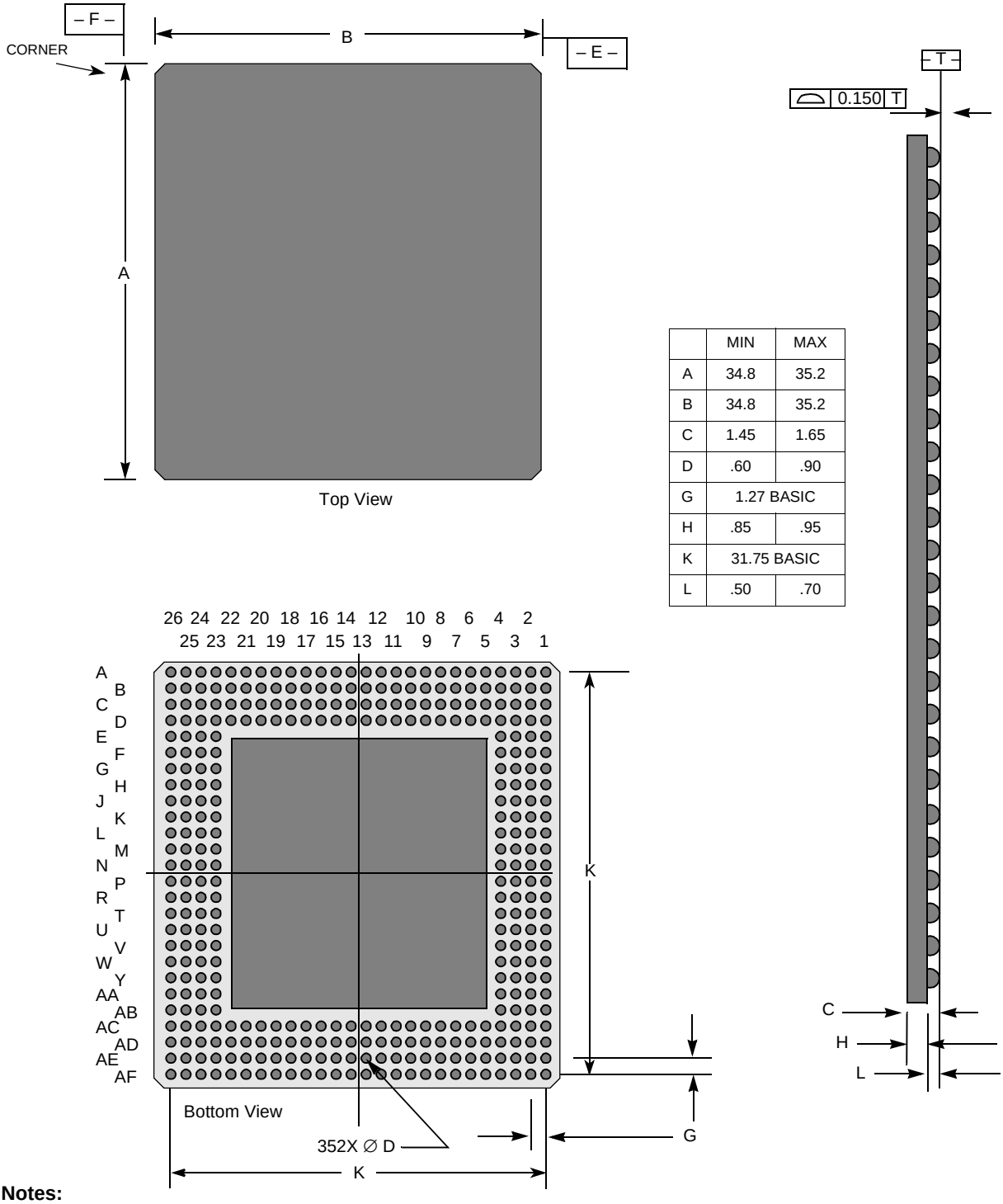
### 1.5.1 Package Parameters

The MPC8240 uses a 35 mm × 35 mm, cavity-down, 352 pin tape ball grid array (TBGA) package. The package parameters are as provided in the following list.

| | |
|---|---|
| Package outline | 35 mm × 35 mm |
| Interconnects | 352 |
| Pitch | 1.27 mm |
| Solder balls | ZU (TBGA)—62 Sn/36 Pb/2 Ag |
| | VV (Lead free version of TBGA package)—95.5 Sn/4.0 Ag/0.5 Cu |
| Solder ball diameter | 0.75 mm |
| Maximum module height | 1.65 mm |
| Co-planarity specification | 0.15 mm |
| Maximum force | 6.0 lbs. total, uniformly distributed over package (8 grams/ball) |

## 1.5.2 Mechanical Dimensions

Figure 23 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC8240, 352 TBGA package.




| | MIN | MAX |
|---|---|---|
| A | 34.8 | 35.2 |
| B | 34.8 | 35.2 |
| C | 1.45 | 1.65 |
| D | .60 | .90 |
| G | 1.27 BASIC | |
| H | .85 | .95 |
| K | 31.75 BASIC | |
| L | .50 | .70 |

**Notes:**
1. Drawing not to scale.
2. All measurements are in millimeters (mm).

**Figure 23. Mechanical Dimensions and Pinout Assignments for the MPC8240, 352 TBGA**

Table 17. MPC8240 Pinout Listing (continued)

| Name | Pin Number | Pin Type | Power Supply | Output Driver Type | Notes |
|---|---|---|---|---|---|
| $\overline{\text{CAS}}$/DQM[0:7] | AB1 AB2 K3 K2 AC1 AC2 K1 J1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 6 |
| $\overline{\text{RAS}}$/$\overline{\text{CS}}$[0:7] | Y4 AA3 AA4 AC4 M2 L2 M1 L1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 6 |
| $\overline{\text{FOE}}$ | H1 | I/O | $GV_{DD}$ | DRV_MEM_ADDR | 3, 4 |
| $\overline{\text{RCS0}}$ | N4 | I/O | $GV_{DD}$ | DRV_MEM_ADDR | 3, 4 |
| $\overline{\text{RCS1}}$ | N2 | Output | $GV_{DD}$ | DRV_MEM_ADDR | |
| SDMA[11:0] | N1 R1 R2 T1 T2 U4 U2 U1 V1 V3 W1 W2 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 6, 14 |
| SDMA12/SDBA1 | P1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 14 |
| SDBA0 | P2 | Output | $GV_{DD}$ | DRV_MEM_ADDR | |
| PAR[0:7] | AF3 AE3 G4 E2 AE4 AF4 D2 C2 | I/O | $GV_{DD}$ | DRV_MEM_DATA | 6, 13, 14 |
| $\overline{\text{SDRAS}}$ | AD1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 3 |
| $\overline{\text{SDCAS}}$ | AD2 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 3 |
| CKE | H2 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 3, 4 |
| $\overline{\text{WE}}$ | AA1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | |
| $\overline{\text{AS}}$ | Y1 | Output | $GV_{DD}$ | DRV_MEM_ADDR | 3, 4 |
| **PIC Control Signals** | | | | | |
| IRQ_0/S_INT | C19 | Input | $OV_{DD}$ | — | 19 |
| IRQ_1/S_CLK | B21 | I/O | $OV_{DD}$ | DRV_PCI | 19 |
| IRQ_2/S_RST | AC22 | I/O | $OV_{DD}$ | DRV_PCI | 19 |
| IRQ_3/$\overline{\text{S_FRAME}}$ | AE24 | I/O | $OV_{DD}$ | DRV_PCI | 19 |
| IRQ_4/$\overline{\text{L_INT}}$ | A23 | I/O | $OV_{DD}$ | DRV_PCI | 19 |
| **$I^2C$ Control Signals** | | | | | |
| SDA | AE20 | I/O | $OV_{DD}$ | DRV_STD | 10, 16 |

Table 17. MPC8240 Pinout Listing (continued)

| Name | Pin Number | Pin Type | Power Supply | Output Driver Type | Notes |
|---|---|---|---|---|---|
| **Test/Configuration Signals** | | | | | |
| PLL_CFG[0:4]/ DA[10:6] | A22 B19 A21 B18 B17 | I/O | $OV_{DD}$ | — | 4, 6 |
| $\overline{\text{TEST0}}$ | AD22 | Input | $OV_{DD}$ | — | 1, 9 |
| $\overline{\text{TEST1}}$ | B20 | Input | $OV_{DD}$ | — | 9, 10 |
| $\overline{\text{TEST2}}$ | Y2 | Input | $GV_{DD}$ | — | 11 |
| TCK | AF22 | Input | $OV_{DD}$ | — | 9, 12 |
| TDI | AF23 | Input | $OV_{DD}$ | — | 9, 12 |
| TDO | AC21 | Output | $OV_{DD}$ | DRV_PCI | |
| TMS | AE22 | Input | $OV_{DD}$ | — | 9, 12 |
| $\overline{\text{TRST}}$ | AE23 | Input | $OV_{DD}$ | — | 9, 12 |
| **Power and Ground Signals** | | | | | |
| GND | AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3 | Ground | — | — | |
| $LV_{DD}$ | AC20 AC23 D20 D23 G23 P23 Y23 | Reference voltage 3.3 V, 5.0 V | $LV_{DD}$ | — | |
| $GV_{DD}$ | AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3 | Power for memory drivers 2.5 V, 3.3 V | $GV_{DD}$ | — | |
| $OV_{DD}$ | AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24 | PCI/Stnd 3.3 V | $OV_{DD}$ | — | |
| $V_{DD}$ | AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4 | Power for core 2.5 V | $V_{DD}$ | — | |
| $LAV_{DD}$ | D17 | Power for DLL 2.5 V | $LAV_{DD}$ | — | |
| $AV_{DD}$ | C17 | Power for PLL (CPU core logic) 2.5 V | $AV_{DD}$ | — | |

# 1.6 PLL Configurations

The MPC8240 internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations for the MPC8240 is shown in Table 18.

**Table 18. MPC8240 Microprocessor PLL Configurations**

| Ref. No. | PLL_CFG [0:4] [2] | CPU [1] HID1 [0:4] | 200 MHz Part [8,9] | | | Ratios [3,4] | |
|---|---|---|---|---|---|---|---|
| | | | PCI Clock Input (PCI_SYNC_IN) Range (MHz) | Peripheral Logic/ Mem Bus Clock Range (MHz) | CPU Clock Range (MHz) | PCI-to-Mem (Mem VCO) Multiplier | Mem-to-CPU (CPU VCO) Multiplier |
| 0 | 00000 | 00110 | 25–26 | 75–80 | 188–200 | 3 (6) | 2.5 (5) |
| 1 | 00001 | 11000 | Not usable | | | 3 (6) | 3 (6) |
| 2 | 00010 | 00101 | 50–56 [5] | 50 – 56 | 100–112 | 1 (4) | 2 (8) |
| 3 | 00011 | 00101 | Bypass | | | Bypass | 2 (8) |
| 4 | 00100 | 00101 | 25–28 [5] | 50–56 | 100–113 | 2 (8) | 2 (8) |
| 5 | 00101 | 00110 | Bypass | | | Bypass | 2.5 (5) |
| 7 | 00111 | 11000 | Bypass | | | Bypass | 3 (6) |
| 8 | 01000 | 11000 | 33 [6]–56 [5] | 33–56 | 100–168 | 1 (4) | 3 (6) |
| A | 01010 | 00111 | Not usable | | | 2 (4) | 4.5 (9) |
| C | 01100 | 00110 | 25–40 | 50–80 | 125–200 | 2 (4) | 2.5 (5) |
| E | 01110 | 11000 | 25–33 | 50–66 | 150–200 | 2 (4) | 3 (6) |
| 10 | 10000 | 00100 | 25–33 | 75–100 | 150–200 | 3 (6) | 2 (4) |
| 12 | 10010 | 00100 | 33 [7]–66 | 50–100 | 100–200 | 1.5 (3) | 2 (4) |
| 14 | 10100 | 11110 | 25–28 | 50–56 | 175–200 | 2 (4) | 3.5 (7) |
| 16 | 10110 | 11010 | 25 | 50 | 200 | 2 (4) | 4 (8) |
| 18 | 11000 | 11000 | 25–26 | 62–65 | 186–200 | 2.5 (5) | 3 (6) |
| 1A | 11010 | 11010 | 50 | 50 | 200 | 1 (2) | 4 (8) |
| 1C | 11100 | 11000 | 33 [7]–44 | 50–66 | 150–200 | 1.5 (3) | 3 (6) |
| 1D | 11101 | 00110 | 33 [7]–53 | 50–80 | 125–200 | 1.5 (3) | 2.5 (5) |

Table 18. MPC8240 Microprocessor PLL Configurations (continued)

| Ref. No. | PLL_CFG [0:4] [2] | CPU [1] HID1 [0:4] | 200 MHz Part [8,9] | | | Ratios [3,4] | |
|---|---|---|---|---|---|---|---|
| | | | PCI Clock Input (PCI_SYNC_IN) Range (MHz) | Peripheral Logic/ Mem Bus Clock Range (MHz) | CPU Clock Range (MHz) | PCI-to-Mem (Mem VCO) Multiplier | Mem-to-CPU (CPU VCO) Multiplier |
| 1E | 11110 | 01111 | Not usable | | | Off | Off |
| 1F | 11111 | 11111 | | | | Off | Off |

**Notes:**

1. The processor HID1 values only represent the multiplier of the processor's PLL (memory-to-processor multiplier); thus, multiple MPC8240 PLL_CFG[0:4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0:4] value.
2. PLL_CFG[0:4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.
3. In PLL-bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in the PLL-bypass mode.
4. In clock-off mode, no clocking occurs inside the MPC8240 regardless of the PCI_SYNC_IN input.
5. Limited due to maximum memory VCO = 225 MHz.
6. Limited due to minimum CPU VCO = 200 MHz.
7. Limited due to minimum memory VCO = 100 MHz.
8. For clarity, range values are shown rounded down to the nearest whole number (decimal place accuracy removed).
9. Note that the 250-MHz part is available only in the XPC8240RZU*nnnx* number series.

# 1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8240.

## 1.7.1 PLL Power Supply Filtering

The $AV_{DD}$, $AV_{DD}2$, and $LAV_{DD}$ power signals on the MPC8240 provide power to the peripheral logic/memory bus PLL, MPC603e processor PLL, and SDRAM clock delay-locked loop (DLL), respectively. To ensure stability of the internal clocks, the power supplied to the $AV_{DD}$, $AV_{DD}2$, and $LAV_{DD}$ input signals should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLLs. Three separate circuits similar to the one shown in Figure 24 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for $AV_{DD}$, $AV_{DD}2$, and $LAV_{DD}$ power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), using multiple small capacitors of equal value is recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important.

interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 25 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on.

The COP header shown in Figure 25 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 25; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

| | |
|---|---|
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| Thermagon Inc.<br>4707 Detroit Ave.<br>Cleveland, OH 44102<br>Internet: www.thermagon.com | 888-246-9050 |

The following section provides a heat sink selection example using one of the commercially-available heat sinks.

### 1.7.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature, $T_{J,}$ can be expressed as follows:

$$T_J = T_A + T_R + (R_{\theta JC} + R_{\theta INT} + R_{\theta SA}) \times P_D$$

where

$T_J$ is the die-junction temperature

$T_A$ is the inlet cabinet ambient temperature

$T_R$ is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta INT}$ is the adhesive or interface material thermal resistance

$R_{\theta SA}$ is the heat sink base-to-ambient thermal resistance

$P_D$ is the power dissipated by the device

During operation, the die-junction temperatures ($T_J$) should be maintained at less than the value specified in Table 2. The temperature of the air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_A$) may range from 30° to 40°C. The air temperature rise within a cabinet ($T_R$) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta INT}$) is typically about 1°C/W. Assuming a $T_A$ of 30°C, a $T_R$ of 5°C, a TBGA package $R_{\theta JC}$ = 1.8, and a power consumption ($P_D$) of 5.0 watts, the following expression for $T_J$ is obtained for die-junction temperature:

$$T_J = 30°C + 5°C + (1.8°C/W + 1.0°C/W + R_{\theta SA}) \times 5.0\ W$$

For preliminary heat sink sizing, the heat sink base-to-ambient thermal resistance is needed from the heat sink manufacturer.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure of merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when using only this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and the many variations of system-level boundary conditions for today’s microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection,

and conduction) may vary widely. For these reasons, it is recommended that conjugate heat-transfer models for the board, as well as system-level designs, be used.

## 1.8 Document Revision History

Table 19 provides a revision history for this hardware specification.

**Table 19. Document Revision History**

| Revision Number | Substantive Change(s) |
|---|---|
| 0 | Preliminary release with some TBDs in the spec tables. |
| 0.1 | Updated notes for Table 2.<br>Replaced TBDs in Table 3 with values for output high and low voltages.<br>Deleted 25/25/75 column from Table 5; inconsistent with PLL encoding 01000.<br>Updated minimum processor frequencies in Table 6 from 80 to 100 MHz.<br>Updated values in Table 8. Spec 10b split for flow through and registered modes.<br>Updated values in Table 9.<br>Updated PCI_HOLD_DEL value guidelines in Table 10 and Figure 10.<br>Relabeled DA[0:15] pins in opposite order and added Note 11 for $\overline{\text{TEST2}}$ in Table 17.<br>Changed PLL configurations 01001 and 10001 in Table 18 to reserved configurations.<br>Updated PLL configuration 00010's operation ranges in Table 18.<br>Revised $\overline{\text{TRST}}$ connection recommendations in Figure 22 for COP interface. |
| 0.2 | Added Note 4 to Table 2, updated Note and Caution numbers in Table 2 and Figure 2.<br>Modified Table 6:<br>—Added 250 MHz column.<br>—Changed Maximum PCI Input Frequency for 200 MHz part from 33 to 66 MHz.<br>—Made one column common entries for Memory Bus and PCI Input Frequencies.<br>Revised Note 7 of Table 7 to indicate a feedback loop length of 6.25 inches (formerly 11.8 inches) corresponding to approximately 1 ns of delay.<br>Added 250 MHz column to Table 18.<br>Corrected document revision number for previous version of this document in Table 19. Document revision was indicated as 1, should have been 0.1.<br>Removed P = Reduced Spec information from Figure 28; does not apply to MPC8240.<br>Added R = Modified Voltage Spec information to Figure 28. |

**Table 19. Document Revision History (continued)**

| Revision Number | Substantive Change(s) |
|---|---|
| 0.5 | Removed references to $GV_{DD}$ = 2.5 V until characterization of the memory interface at this voltage has been completed.<br>Corrected Figure 2 power supply ramp-up time to be before the 100 ms PLL relock time.<br>Table 3:<br>• Deleted input leakage specification @ $LV_{DD}$ = 5.5 V.<br>• Changed minimum 'Input High Voltage for PCI only' from 0.5*OVDodaoD to 0.65*OVDD and added Note 6.<br>• Changed condition on 'Input Low Voltage,' $V_{IL}$, from 'All inputs except OSC_IN' to 'All inputs except PCI_SYNC_IN.'<br>• Replaced minimum $CV_{IH}$ formula, 0.5*OVDD, with 2.4-V value.<br>• Replaced maximum $CV_{IL}$ formula, 0.3*OVDD, with 0.4-V value.<br>Added Note 10 to Table 5.<br>Changed minimum memory bus frequency of operation from 25 to 33 MHz in Table 6 to coincide with information shown in PLL_CFG Table 18.<br>Updated clock specifications in Table 7.<br>Updated input AC timing specifications in Table 8.<br>Updated output AC timing specifications in Table 9.<br>Replaced TBDs in Table 14 for specs 3, 5, and 6.<br>Table 17 renamed TEST3 (pin AF20) to TRIG_IN and renamed TEST4 (pin AC18) to TRIG_OUT; moved both pins from Test/Configuration Signals group to Miscellaneous Signals group.<br>Added external pull-up resistor to LVDD recommendation for $\overline{\text{INTA}}$ signal in Table 17 and Section 1.7.5.<br>Added Note 19 to Table 17 about AVDD and LAVDD being internally connected; revised Section 1.7.1, on filtering these pins.<br>Replaced HID1 column TBDs in Table 18 and deleted Note 1 resulting in renumbering notes throughout Table 18.<br>Added Section 1.7.7, about PCI reference voltage.<br>Added note in Section 1.9, indicating 'L=Standard Spec.' part is only available in 200 MHz version of the device. Changed 'XPC' to 'MPC' for consistency with other references in the document. |

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