# Renesas Electronics America Inc - M30260F6AGP#U5A Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IEBus, SIO, UART/USART |
| Peripherals | DMA, PWM, Voltage Detect, WDT |
| Number of I/O | 39 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30260f6agp-u5a |

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# 1. Overview

The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M16C/60 Series CPU core. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is housed in 42-pin and 48-pin plastic molded packages. With a 1M byte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

## 1.1 Applications

Audio, cameras, office/communications/portable/ equipment, air-conditioning equipment, home appliances, etc.

**Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin device)**

| | Item | Performance |
|---|---|---|
| CPU | Basic instructions | 91 instructions |
| | Minimun instruction execution time | 41.7 ns (f(BCLK) = 24 MHz (4), VCC = 4.2 to 5.5 V (M16C/26B)<br>50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B)<br>100 ns (f(BCLK) = 10 MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B) |
| | Operation mode | Single-chip mode |
| | Address space | 1M byte |
| | Memory capacity | See **1.4 Product Information** |
| Peripheral function | Port | 33 I/O pins |
| | Multifunction timer | Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels<br>Three-phase motor control timer |
| | Serial I/O | 1 channel (UART, clock synchronous serial I/O)<br>1 channel (UART, clock synchronous, $I^2C$ bus(1) , or IEBus(2)) |
| | A/D converter | 10 bit A/D converter: 1 circuit, 10 channels |
| | DMAC | 2 channels |
| | CRC calcuration circuit | 1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable |
| | Watchdog timer | 15 bits x 1 channel (with prescaler) |
| | Interrupt | 18 internal and 8 external sources, 4 software sources,<br>Interrupt priority level: 7 |
| | Clock generation circuit | 4 circuits<br>Main clock(*), Sub-clock(*)<br>On-chip oscillator, PLL frequency synthesizer<br>(*)Equipped with a built-in feedback resister. |
| | Oscillation stop detection | Main clock oscillation stop, re-oscillation detection function |
| | Voltage detection circuit | On-chip |
| Electrical Characteristics | Supply voltage | Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(4) (M16C/26B)<br>Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B)<br>Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz) |
| | Power Consumption | 16 mA (Vcc = 5 V, f(BCLK) = 20 MHz)<br>25 μA (f(XCIN) = 32 KHz on RAM)<br>3 μA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode)<br>0.7 μA (Vcc = 3 V, in stop mode) |
| Flash memory | Programming/erasure voltage | 2.7 to 5.5 V |
| | Programming/erasure endurance | 100 times (all area) or 1,000 times (block 0 to 3)<br>/ 10,000 times (block A, block B)(3) |
| Operating Ambient Temperature | | -20 to 85°C / -40 to 85°C (3) |
| Package | | 42-pin plastic molded SSOP |

NOTES:
1. $I^2C$ bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

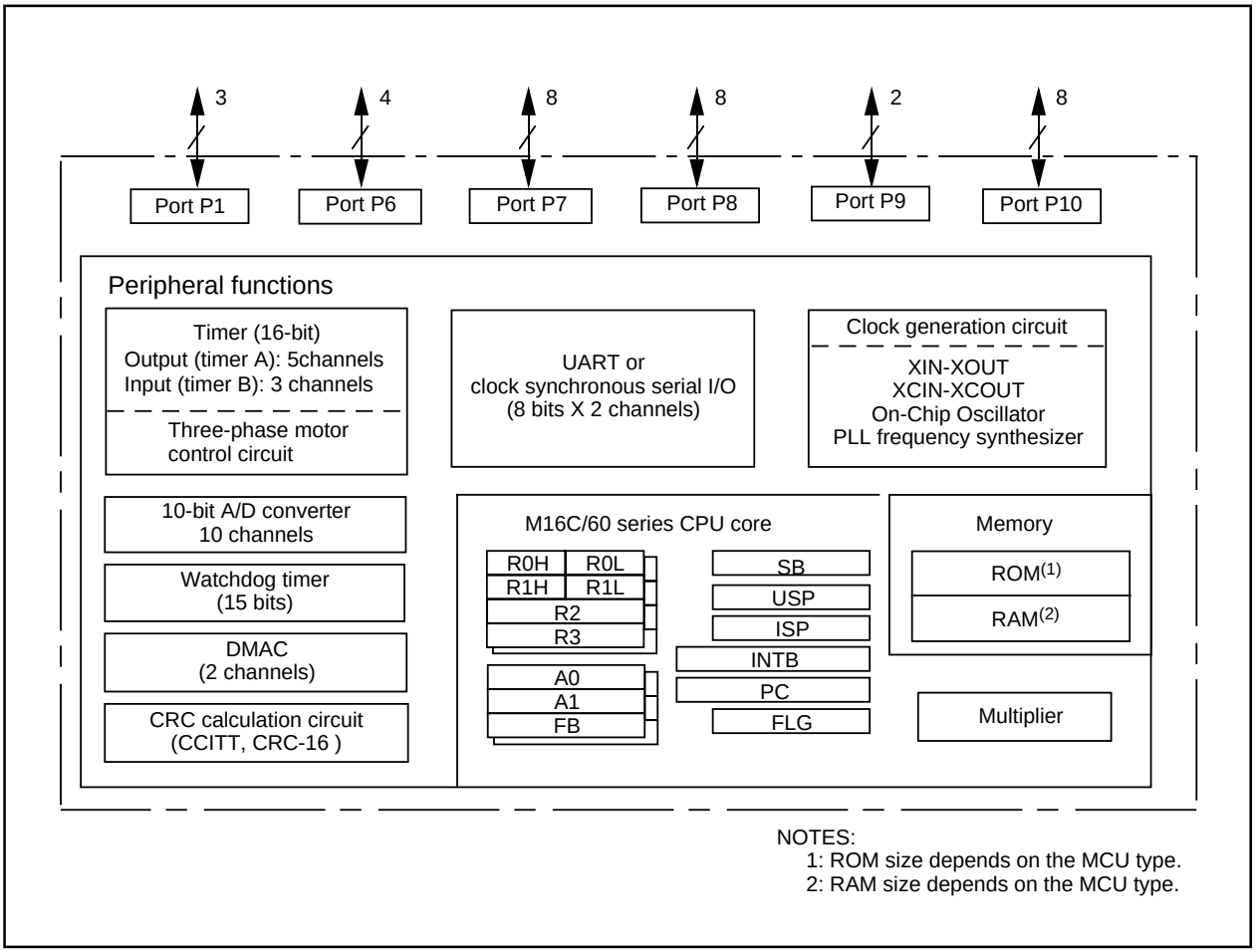



**Figure 1.2 Block Diagram( 42-pin Package)**

**Table 1.7 Product Code (Flash Memory Version) - M16C/26A, M16C/26B**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|
| | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| U3 | Lead free | 100 | 0 to 60°C | 100 | 0 to 60°C | -40 to 85°C |
| U5 | | | | | | -20 to 85°C |
| U7 | | 1,000 | | 10,000 | -40 to 85°C | -40 to 85°C |
| U9 | | | | | -20 to 85°C | -20 to 85°C |

**Table 1.8 Product Code (Mask ROM Version - M16C/26A)**

| Product Code | Package | Operating Ambient Temperature |
|---|---|---|
| U3 | Lead free | -40°C to 85°C |
| U5 | | -20°C to 85°C |

NOTE:

1. The lead contained products, D3, D5, D7, and D9 are put together with U3, U5, U7, and U9 respectively. Lead-free products can be mounted by both conventional Sn-Pb paste and Lead-free paste (Sn-Ag-Cu plating).

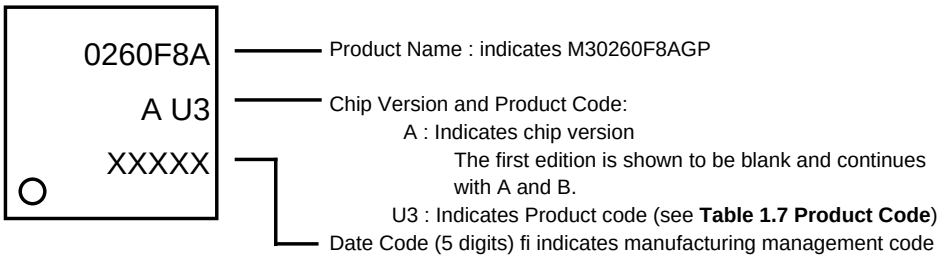
**Table 1.9 Product Code (Flash Memory Version) - M16C/26T T-ver.**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temerature |
|---|---|---|---|---|---|---|
| | | Programming and erasure endurance | Temperature range | Programming and erasure endurance | Temperature range | |
| U3 | Lead free | 100 | 0°C to 60°C | 100 | -40°C to 85°C | -40°C to 85°C |
| U7 | | 1,000 | | 10,000 | | |

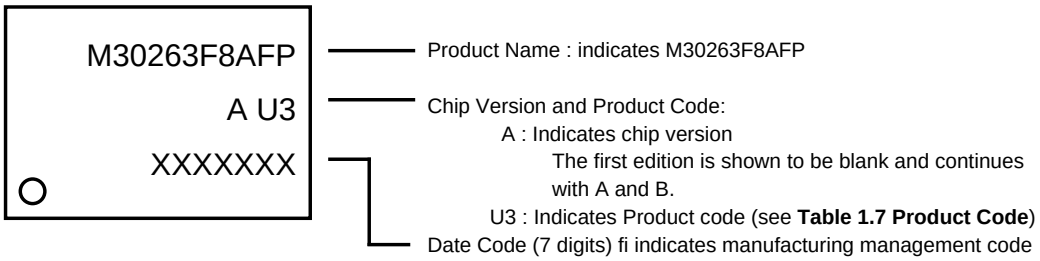
**Table 1.10 Product Code (Flash Memory Version) - M16C/26T V-ver.**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temerature |
|---|---|---|---|---|---|---|
| | | Programming and erasure endurance | Temperature range | Programming and erasure endurance | Temperature range | |
| U3 | Lead free | 100 | 0°C to 60°C | 100 | -40°C to 125°C | -40°C to 125°C |
| U7 | | 1,000 | | 10,000 | | |

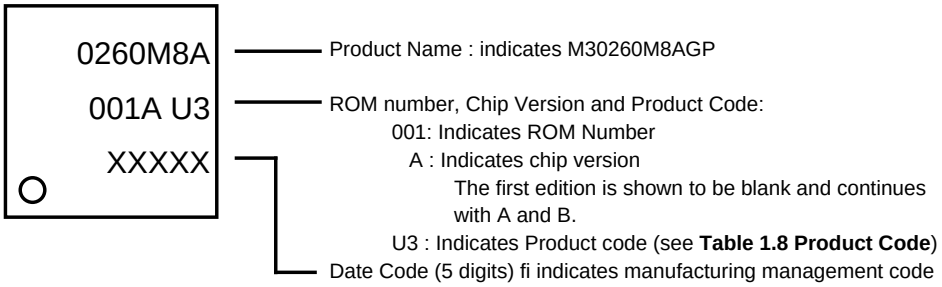
(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26A, M16C/26B




(2) Flash memory version, PRSP0042GA-B (42P2R), M16C/26A, M16C/26B




(3) MASK ROM version, PLQP0048KB-A (48P6Q), M16C/26A




(4) MASK ROM version, PRSP0042GA-B (42P2R), M16C/26A

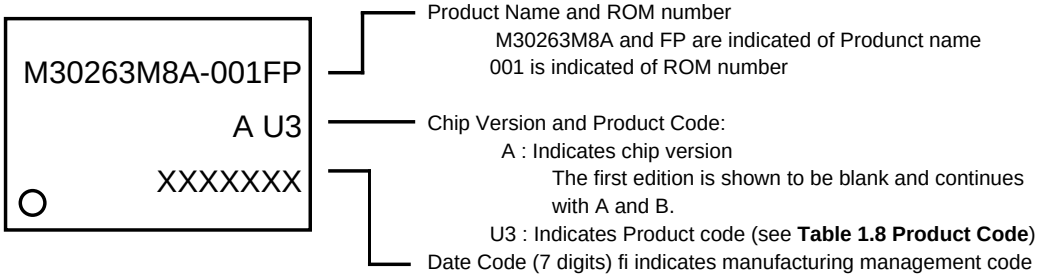
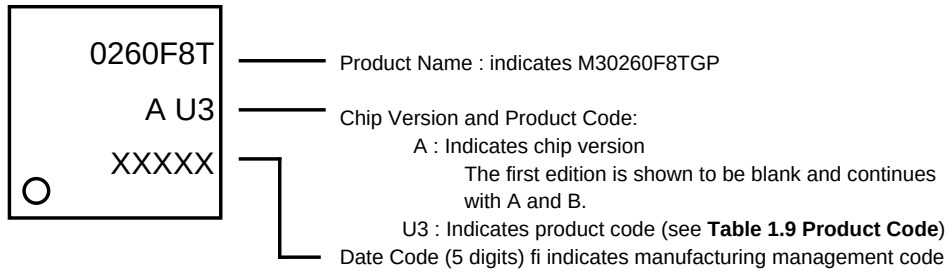



**Figure 1.4 Marking Diagram (M16C/26A , M16C/26B)**

(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T T-ver.




(2) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T V-ver.

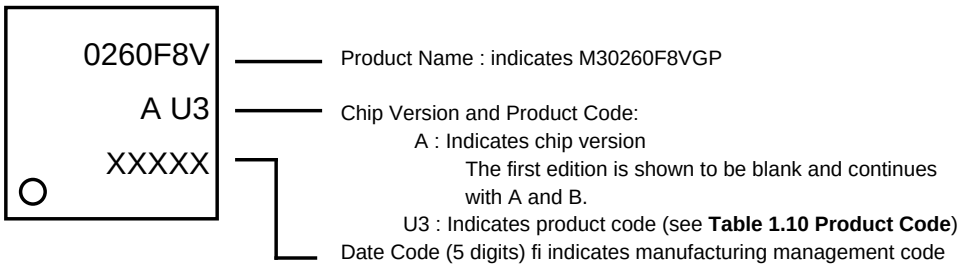



**Figure 1.5 Marking Diagram (M16C/26T)**

## 1.5 Pin Assignments

**Figures 1.6** and **1.7** show the Pin Assignments (top view).

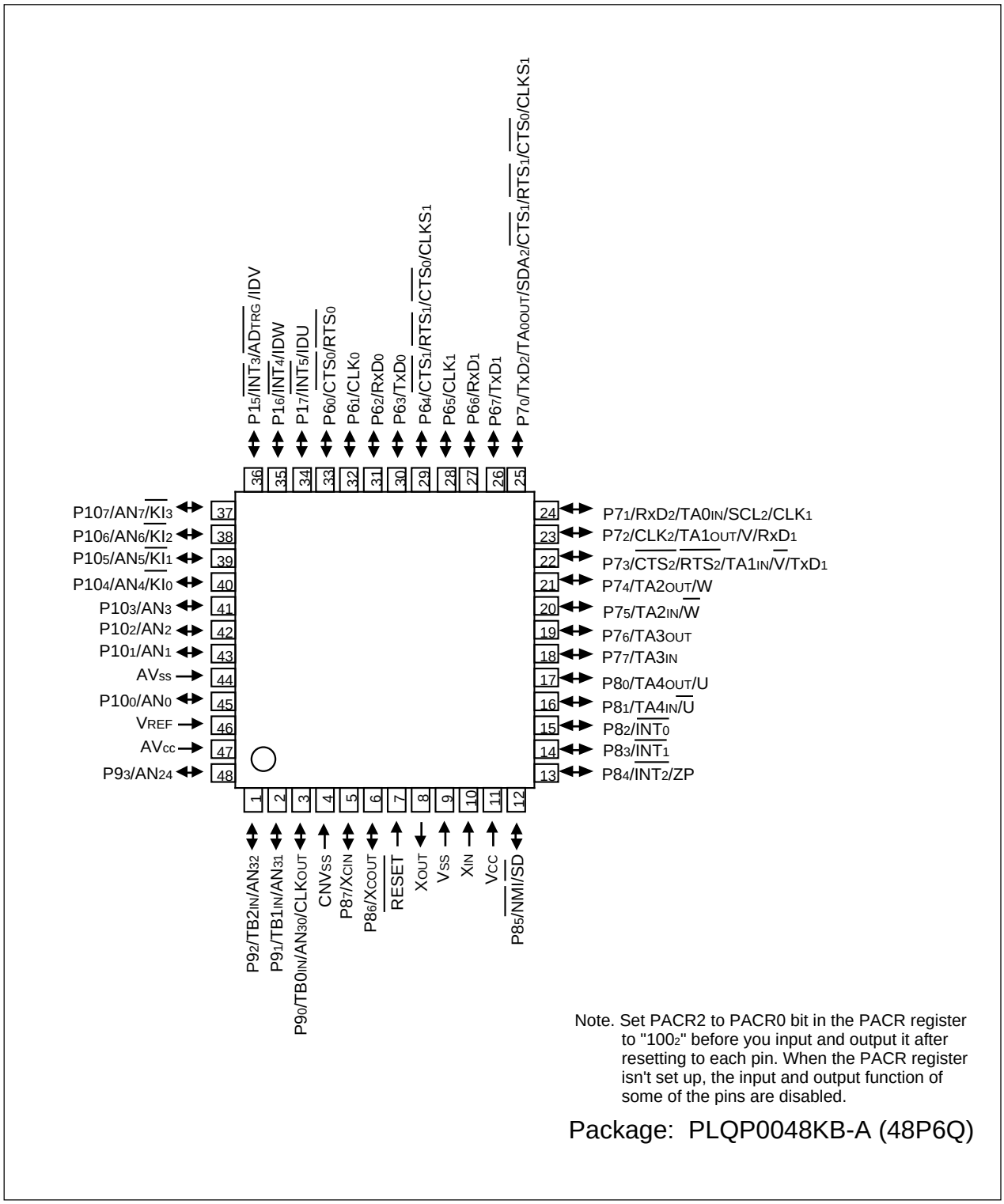
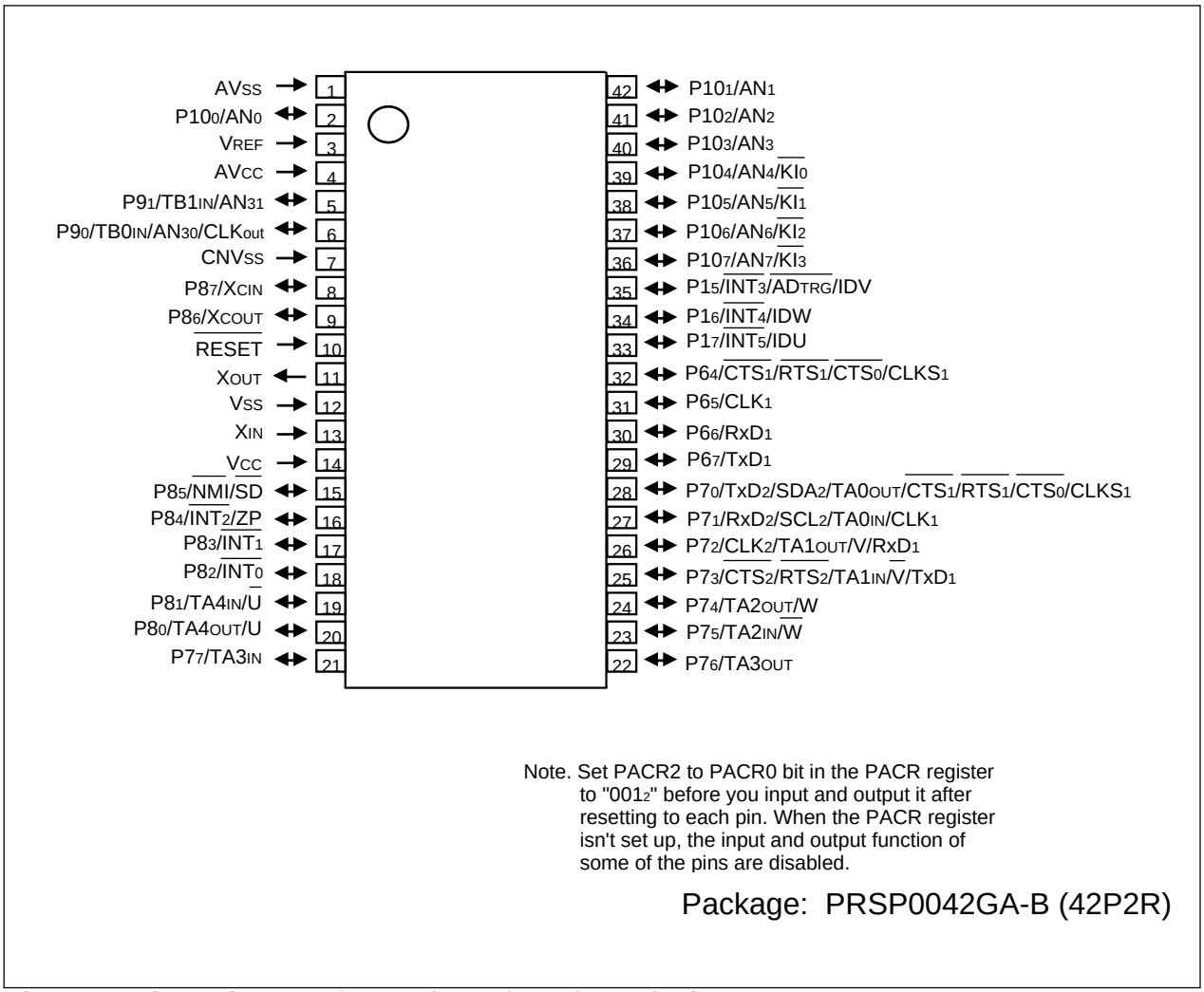



**Figure 1.6 Pin Assignment for 48-Pin Package (Top View)**

**Table 1.11 Pin Characteristics for 48-Pin Package**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin |
|---|---|---|---|---|---|---|
| 1 | | $P9_2$ | | $TB_{2IN}$ | | $AN3_2$ |
| 2 | | $P9_1$ | | $TB_{1IN}$ | | $AN3_1$ |
| 3 | | $P9_0$ | | $TB_{0IN}$ | $CLK_{OUT}$ | $AN3_0$ |
| 4 | CNVss | | | | | |
| 5 | $X_{CIN}$ | $P8_7$ | | | | |
| 6 | $X_{COUT}$ | $P8_6$ | | | | |
| 7 | $\overline{RESET}$ | | | | | |
| 8 | $X_{OUT}$ | | | | | |
| 9 | Vss | | | | | |
| 10 | $X_{IN}$ | | | | | |
| 11 | Vcc | | | | | |
| 12 | | $P8_5$ | $\overline{NMI}$ | $\overline{SD}$ | | |
| 13 | | $P8_4$ | $\overline{INT_2}$ | ZP | | |
| 14 | | $P8_3$ | $\overline{INT_1}$ | | | |
| 15 | | $P8_2$ | $\overline{INT_0}$ | | | |
| 16 | | $P8_1$ | | $TA_{4IN}$ / $\overline{U}$ | | |
| 17 | | $P8_0$ | | $TA_{4OUT}$ / U | | |
| 18 | | $P7_7$ | | $TA_{3IN}$ | | |
| 19 | | $P7_6$ | | $TA_{3OUT}$ | | |
| 20 | | $P7_5$ | | $TA_{2IN}$ / $\overline{W}$ | | |
| 21 | | $P7_4$ | | $TA_{2OUT}$ / W | | |
| 22 | | $P7_3$ | | $TA_{1IN}$ / $\overline{V}$ | $\overline{CTS_2}$ / $\overline{RTS_2}$ / $TxD_1$ | |
| 23 | | $P7_2$ | | $TA_{1OUT}$ / V | $CLK_2$ / $RxD_1$ | |
| 24 | | $P7_1$ | | $TA_{0IN}$ | $RxD_2$ / $SCL_2$ / $CLK_1$ | |
| 25 | | $P7_0$ | | $TA_{0OUT}$ | $TxD_2$ / $SDA_2$ / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$ | |
| 26 | | $P6_7$ | | | $TxD_1$ | |
| 27 | | $P6_6$ | | | $RxD_1$ | |
| 28 | | $P6_5$ | | | $CLK_1$ | |
| 29 | | $P6_4$ | | | $\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$ | |
| 30 | | $P6_3$ | | | $TxD_0$ | |
| 31 | | $P6_2$ | | | $RxD_0$ | |
| 32 | | $P6_1$ | | | $CLK_0$ | |
| 33 | | $P6_0$ | | | $\overline{RTS_0}$ / $\overline{CTS_0}$ | |
| 34 | | $P1_7$ | $\overline{INT_5}$ | IDU | | |
| 35 | | $P1_6$ | $\overline{INT_4}$ | IDW | | |
| 36 | | $P1_5$ | $\overline{INT_3}$ | IDV | | $\overline{ADTRG}$ |
| 37 | | $P10_7$ | $\overline{KI_3}$ | | | $AN_7$ |
| 38 | | $P10_6$ | $\overline{KI_2}$ | | | $AN_6$ |
| 39 | | $P10_5$ | $\overline{KI_1}$ | | | $AN_5$ |
| 40 | | $P10_4$ | $\overline{KI_0}$ | | | $AN_4$ |
| 41 | | $P10_3$ | | | | $AN_3$ |
| 42 | | $P10_2$ | | | | $AN_2$ |
| 43 | | $P10_1$ | | | | $AN_1$ |
| 44 | AVss | | | | | |
| 45 | | $P10_0$ | | | | $AN_0$ |
| 46 | $V_{REF}$ | | | | | |
| 47 | AVcc | | | | | |
| 48 | | $P9_3$ | | | | $AN2_4$ |




Note. Set PACR2 to PACR0 bit in the PACR register to "$001_2$" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PRSP0042GA-B (42P2R)

**Figure 1.7 Pin Assignment for 42-Pin Package (Top View)**

**Table 1.12 Pin Characteristics for 42-Pin Package**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin |
|---|---|---|---|---|---|---|
| 1 | AVss | | | | | |
| 2 | | P10$_0$ | | | | AN$_0$ |
| 3 | VREF | | | | | |
| 4 | AVCC | | | | | |
| 5 | | P9$_1$ | | TB$_{1IN}$ | | AN3$_1$ |
| 6 | | P9$_0$ | | TB$_{0IN}$ | CLK$_{OUT}$ | AN3$_0$ |
| 7 | CNVss | | | | | |
| 8 | XCIN | P8$_7$ | | | | |
| 9 | XCOUT | P8$_6$ | | | | |
| 10 | $\overline{\text{RESET}}$ | | | | | |
| 11 | XOUT | | | | | |
| 12 | Vss | | | | | |
| 13 | XIN | | | | | |
| 14 | VCC | | | | | |
| 15 | | P8$_5$ | $\overline{\text{NMI}}$ | $\overline{\text{SD}}$ | | |
| 16 | | P8$_4$ | $\overline{\text{INT}}_2$ | ZP | | |
| 17 | | P8$_3$ | $\overline{\text{INT}}_1$ | | | |
| 18 | | P8$_2$ | $\overline{\text{INT}}_0$ | | | |
| 19 | | P8$_1$ | | TA$_{4IN}$ / $\overline{\text{U}}$ | | |
| 20 | | P8$_0$ | | TA$_{4OUT}$ / U | | |
| 21 | | P7$_7$ | | TA$_{3IN}$ | | |
| 22 | | P7$_6$ | | TA$_{3OUT}$ | | |
| 23 | | P7$_5$ | | TA$_{2IN}$ / $\overline{\text{W}}$ | | |
| 24 | | P7$_4$ | | TA$_{2OUT}$ / W | | |
| 25 | | P7$_3$ | | TA$_{1IN}$ / $\overline{\text{V}}$ | $\overline{\text{CTS}}_2$ / $\overline{\text{RTS}}_2$ / TxD$_1$ | |
| 26 | | P7$_2$ | | TA$_{1OUT}$ / V | CLK$_2$ / RxD$_1$ | |
| 27 | | P7$_1$ | | TA$_{0IN}$ | RxD$_2$ / SCL$_2$ / CLK$_1$ | |
| 28 | | P7$_0$ | | TA$_{0OUT}$ | TxD$_2$ / SDA$_2$ / $\overline{\text{RTS}}_1$ / $\overline{\text{CTS}}_1$ / $\overline{\text{CTS}}_0$ / CLKS$_1$ | |
| 29 | | P6$_7$ | | | TxD$_1$ | |
| 30 | | P6$_6$ | | | RxD$_1$ | |
| 31 | | P6$_5$ | | | CLK$_1$ | |
| 32 | | P6$_4$ | | | $\overline{\text{RTS}}_1$ / $\overline{\text{CTS}}_1$/ $\overline{\text{CTS}}_0$ / CLKS$_1$ | |
| 33 | | P1$_7$ | $\overline{\text{INT}}_5$ | IDU | | |
| 34 | | P1$_6$ | $\overline{\text{INT}}_4$ | IDW | | |
| 35 | | P1$_5$ | $\overline{\text{INT}}_3$ | IDV | | $\overline{\text{ADTRG}}$ |
| 36 | | P10$_7$ | $\overline{\text{KI}}_3$ | | | AN$_7$ |
| 37 | | P10$_6$ | $\overline{\text{KI}}_2$ | | | AN$_6$ |
| 38 | | P10$_5$ | $\overline{\text{KI}}_1$ | | | AN$_5$ |
| 39 | | P10$_4$ | $\overline{\text{KI}}_0$ | | | AN$_4$ |
| 40 | | P10$_3$ | | | | AN$_3$ |
| 41 | | P10$_2$ | | | | AN$_2$ |
| 42 | | P10$_1$ | | | | AN$_1$ |

## 1.6 Pin Description

**Table 1.13 Pin Description (48-Pin and 42-Pin Packages)**

| Classification | Pin Name | I/O Type | Description |
|---|---|---|---|
| Power Supply | VCC, VSS | I | Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (M16C/26A, M16C/26B), 3.0 to 5.5 V (M16C/26T T-ver.), 4.2 to 5.5 V (M16C/26T V-ver.) |
| Analog Power Supply | AVCC<br>AVSS | I | Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS |
| Reset Input | $\overline{\text{RESET}}$ | I | The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin |
| CNVSS | CNVSS | I | Connect the CNVSS pin to VSS |
| Main Clock Input | XIN | I | I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock), connect XIN pin to VCC and leave XOUT open |
| Main Clock Output | XOUT | O | |
| Sub Clock Input | XCIN | I | I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT |
| Sub Clock Output | XCOUT | O | |
| Clock Output | CLKOUT | O | Outputs the clock having the same frequency as f1, f8, f32, or fC |
| $\overline{\text{INT}}$ Interrupt Input | $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ | I | Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function |
| $\overline{\text{NMI}}$ Interrupt Input | $\overline{\text{NMI}}$ | I | $\overline{\text{NMI}}$ interrupt input pin. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled |
| Key Input Interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Input pins for the key input interrupt |
| Timer A | TA0OUT to TA4OUT | I/O | I/O pins for the timer A0 to A4 |
| | TA0IN to TA4IN | I | Input pins for the timer A0 to A4 |
| | ZP | I | Input pin for Z-phase |
| Timer B | TB0IN to TB1IN | I | Timer B0 to B1 input pins |
| Three-Phase Motor Control Timer Output | U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$ | O | Output pins for the three-phase motor control timer |
| | IDU, IDW, IDV, $\overline{\text{SD}}$ | I/O | I/O pins for the three-phase motor control timer |
| Serial I/O | $\overline{\text{CTS1}}$ to $\overline{\text{CTS2}}$ | I | Input pins to control data transmission |
| | $\overline{\text{RTS1}}$ to $\overline{\text{RTS2}}$ | O | Output pins to control data reception |
| | CLK1 to CLK2 | I/O | Inputs and outputs the transfer clock |
| | RxD1 to RxD2 | I | Inputs serial data |
| | TxD1 to TxD2 | O | Outputs serial data |
| | CLKS1 | O | Output pin for transfer clock |
| Reference Voltage Input | VREF | I | Applies reference voltage to the A/D converter |
| A/D Converter | AN0 to AN7<br>AN30 to AN31 | I | Analog input pins for the A/D converter |
| | $\overline{\text{ADTRG}}$ | I | Input pin for an external A/D trigger |
| I/O Ports | P15 to P17 | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 3-bit units |
| | P64 to P67<br>P70 to P77<br>P80 to P87<br>P100 to P107<br>P90 to P91 | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units |

I : Input O : Output I/O : Input and output

**Table 1.13 Pin Description ( 48-pin packages only) (Continued)**

| Classification | Pin Name | I/O Type | Description |
|---|---|---|---|
| Serial I/O | $\overline{CTS0}$ | I | Inputs pin to control data transmission |
| | $\overline{RTS0}$ | O | Output pin to control data reception |
| | CLK0 | I/O | Inputs and outputs the transfer clock |
| | RxD0 | I | Inputs serial data |
| | TxD0 | O | Outputs serial data |
| Timer B | TB2IN | I | Timer B2 input pin |
| A/D Converter | $AN2_4$<br>$AN3_2$ | I | Analog input pins for the A/D converter |
| I/O Ports | $P6_0$ to $P6_3$<br>$P9_2$ to $P9_3$ | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units |

I : Input O : Output I/O : Input and output

# 2. Central Processing Unit (CPU)

**Figure 2.1** shows the CPU registers. The register bank is comprised of seven registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 registers. There are two sets of register bank.

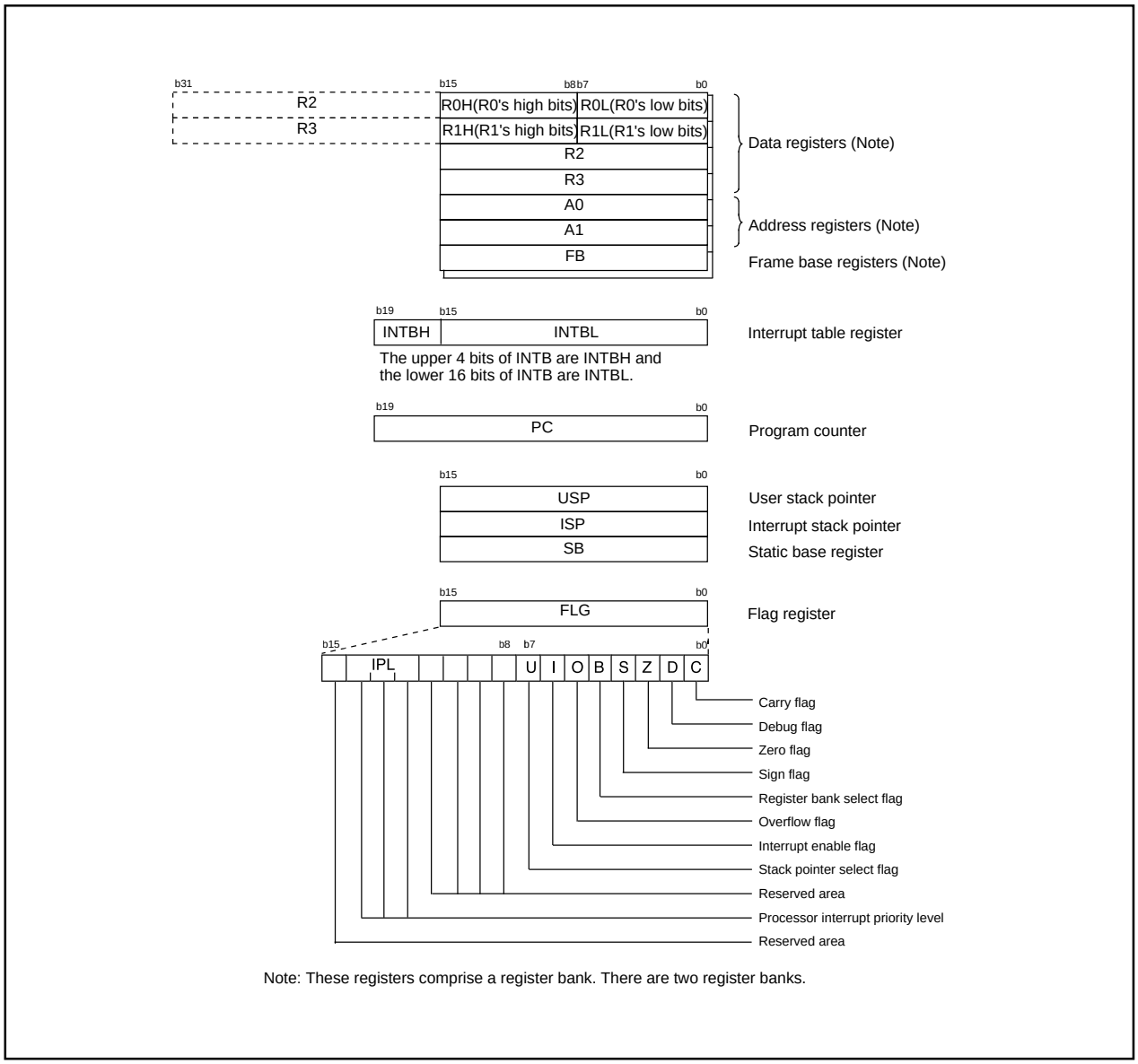



**Figure 2.1. CPU Register**

## 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

### 2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

# 4. Special Function Register (SFR)

### Table 4.1 SFR Information(1)[1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0000₁₆ | | | |
| 0001₁₆ | | | |
| 0002₁₆ | | | |
| 0003₁₆ | | | |
| 0004₁₆ | Processor mode register 0 | PM0 | 00₁₆ |
| 0005₁₆ | Processor mode register 1 | PM1 | 00001000₂ |
| 0006₁₆ | System clock control register 0 | CM0 | 01001000₂(M16C/26A)<br>01101000₂(M16C/26T) |
| 0007₁₆ | System clock control register 1 | CM1 | 00100000₂ |
| 0008₁₆ | | | |
| 0009₁₆ | Address match interrupt enable register | AIER | XXXXXX00₂ |
| 000A₁₆ | Protect register | PRCR | XX000000₂ |
| 000B₁₆ | | | |
| 000C₁₆ | Oscillation stop detection register[2] | CM2 | 0X000000₂ |
| 000D₁₆ | | | |
| 000E₁₆ | Watchdog timer start register | WDTS | XX₁₆ |
| 000F₁₆ | Watchdog timer control register | WDC | 00XXXXX2 [3] |
| 0010₁₆ | Address match interrupt register 0 | RMAD0 | 00₁₆ |
| 0011₁₆ | | | 00₁₆ |
| 0012₁₆ | | | X0₁₆ |
| 0013₁₆ | | | |
| 0014₁₆ | Address match interrupt register 1 | RMAD1 | 00₁₆ |
| 0015₁₆ | | | 00₁₆ |
| 0016₁₆ | | | X0₁₆ |
| 0017₁₆ | | | |
| 0018₁₆ | | | |
| 0019₁₆ | Voltage detection register 1 [4, 5] | VCR1 | 00001000₂ |
| 001A₁₆ | Voltage detection register 2 [4, 5] | VCR2 | 00₁₆ |
| 001B₁₆ | | | |
| 001C₁₆ | PLL control register 0 | PLC0 | 0001X010₂ |
| 001D₁₆ | | | |
| 001E₁₆ | Processor mode register 2 | PM2 | XXX00000₂ |
| 001F₁₆ | Low voltage detection interrupt register[5] | D4INT | 00₁₆ |
| 0020₁₆ | DMA0 source pointer | SAR0 | XX₁₆ |
| 0021₁₆ | | | XX₁₆ |
| 0022₁₆ | | | XX₁₆ |
| 0023₁₆ | | | |
| 0024₁₆ | DMA0 destination pointer | DAR0 | XX₁₆ |
| 0025₁₆ | | | XX₁₆ |
| 0026₁₆ | | | XX₁₆ |
| 0027₁₆ | | | |
| 0028₁₆ | DMA0 transfer counter | TCR0 | XX₁₆ |
| 0029₁₆ | | | XX₁₆ |
| 002A₁₆ | | | |
| 002B₁₆ | | | |
| 002C₁₆ | DMA0 control register | DM0CON | 00000X00₂ |
| 002D₁₆ | | | |
| 002E₁₆ | | | |
| 002F₁₆ | | | |
| 0030₁₆ | DMA1 source pointer | SAR1 | XX₁₆ |
| 0031₁₆ | | | XX₁₆ |
| 0032₁₆ | | | XX₁₆ |
| 0033₁₆ | | | |
| 0034₁₆ | DMA1 destination pointer | DAR1 | XX₁₆ |
| 0035₁₆ | | | XX₁₆ |
| 0036₁₆ | | | XX₁₆ |
| 0037₁₆ | | | |
| 0038₁₆ | DMA1 transfer counter | TCR1 | XX₁₆ |
| 0039₁₆ | | | XX₁₆ |
| 003A₁₆ | | | |
| 003B₁₆ | | | |
| 003C₁₆ | DMA1 control register | DM1CON | 00000X00₂ |
| 003D₁₆ | | | |
| 003E₁₆ | | | |
| 003F₁₆ | | | |

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. Bits CM27, CM21, and CM20 do not change at oscillation stop detection reset.
3. The WDC5 bit is 0 (cold start) immediately after power-on. It can only be set to 1 by program. The WDC5 bit cannot be used in M16C/26T.
4. The VCR1 and VCR2 registers do not change at software reset, watchdog timer reset, and oscillation stop detection reset.
5. Registers VCR1, VCR2, and D4INT cannot be used in M16C/26T.

X : Undefined

**Table 4.2 SFR Information(2)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0040₁₆ | | | |
| 0041₁₆ | | | |
| 0042₁₆ | | | |
| 0043₁₆ | | | |
| 0044₁₆ | INT3 interrupt control register | INT3IC | XX00X000₂ |
| 0045₁₆ | | | |
| 0046₁₆ | | | |
| 0047₁₆ | | | |
| 0048₁₆ | INT5 interrupt control register | INT5IC | XX00X000₂ |
| 0049₁₆ | INT4 interrupt control register | INT4IC | XX00X000₂ |
| 004A₁₆ | UART2 Bus collision detection interrupt control register | BCNIC | XXXXX000₂ |
| 004B₁₆ | DMA0 interrupt control register | DM0IC | XXXXX000₂ |
| 004C₁₆ | DMA1 interrupt control register | DM1IC | XXXXX000₂ |
| 004D₁₆ | Key input interrupt control register | KUPIC | XXXXX000₂ |
| 004E₁₆ | A/D conversion interrupt control register | ADIC | XXXXX000₂ |
| 004F₁₆ | UART2 transmit interrupt control register | S2TIC | XXXXX000₂ |
| 0050₁₆ | UART2 receive interrupt control register | S2RIC | XXXXX000₂ |
| 0051₁₆ | UART0 transmit interrupt control register | S0TIC | XXXXX000₂ |
| 0052₁₆ | UART0 receive interrupt control register | S0RIC | XXXXX000₂ |
| 0053₁₆ | UART1 transmit interrupt control register | S1TIC | XXXXX000₂ |
| 0054₁₆ | UART1 receive interrupt control register | S1RIC | XXXXX000₂ |
| 0055₁₆ | TimerA0 interrupt control register | TA0IC | XXXXX000₂ |
| 0056₁₆ | TimerA1 interrupt control register | TA1IC | XXXXX000₂ |
| 0057₁₆ | TimerA2 interrupt control register | TA2IC | XXXXX000₂ |
| 0058₁₆ | TimerA3 interrupt control register | TA3IC | XXXXX000₂ |
| 0059₁₆ | TimerA4 interrupt control register | TA4IC | XXXXX000₂ |
| 005A₁₆ | TimerB0 interrupt control register | TB0IC | XXXXX000₂ |
| 005B₁₆ | TimerB1 interrupt control register | TB1IC | XXXXX000₂ |
| 005C₁₆ | TimerB2 interrupt control register | TB2IC | XXXXX000₂ |
| 005D₁₆ | INT0 interrupt control register | INT0IC | XX00X000₂ |
| 005E₁₆ | INT1 interrupt control register | INT1IC | XX00X000₂ |
| 005F₁₆ | INT2 interrupt control register | INT2IC | XX00X000₂ |
| 0060₁₆ | | | |
| 0061₁₆ | | | |
| 0062₁₆ | | | |
| 0063₁₆ | | | |
| 0064₁₆ | | | |
| 0065₁₆ | | | |
| 0066₁₆ | | | |
| 0067₁₆ | | | |
| 0068₁₆ | | | |
| 0069₁₆ | | | |
| 006A₁₆ | | | |
| 006B₁₆ | | | |
| 006C₁₆ | | | |
| 006D₁₆ | | | |
| 006E₁₆ | | | |
| 006F₁₆ | | | |
| 0070₁₆ | | | |
| 0071₁₆ | | | |
| 0072₁₆ | | | |
| 0073₁₆ | | | |
| 0074₁₆ | | | |
| 0075₁₆ | | | |
| 0076₁₆ | | | |
| 0077₁₆ | | | |
| 0078₁₆ | | | |
| 0079₁₆ | | | |
| 007A₁₆ | | | |
| 007B₁₆ | | | |
| 007C₁₆ | | | |
| 007D₁₆ | | | |
| 007E₁₆ | | | |
| 007F₁₆ | | | |

NOTE:
1. Blank spaces are reserved. No access is allowed.

X: Undefined

**Table 4.5 SFR Information(5)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 038016 | Count start flag | TABSR | 0016 |
| 038116 | Clock prescaler reset flag | CPSRF | 0XXXXXXX2 |
| 038216 | One-shot start flag | ONSF | 0016 |
| 038316 | Trigger select register | TRGSR | 0016 |
| 038416 | Up-dowm flag | UDF | 0016 |
| 038516 | | | |
| 038616 | Timer A0 register | TA0 | XX16 |
| 038716 | | | XX16 |
| 038816 | Timer A1 register | TA1 | XX16 |
| 038916 | | | XX16 |
| 038A16 | Timer A2 register | TA2 | XX16 |
| 038B16 | | | XX16 |
| 038C16 | Timer A3 register | TA3 | XX16 |
| 038D16 | | | XX16 |
| 038E16 | Timer A4 register | TA4 | XX16 |
| 038F16 | | | XX16 |
| 039016 | Timer B0 register | TB0 | XX16 |
| 039116 | | | XX16 |
| 039216 | Timer B1 register | TB1 | XX16 |
| 039316 | | | XX16 |
| 039416 | Timer B2 register | TB2 | XX16 |
| 039516 | | | XX16 |
| 039616 | Timer A0 mode register | TA0MR | 0016 |
| 039716 | Timer A1 mode register | TA1MR | 0016 |
| 039816 | Timer A2 mode register | TA2MR | 0016 |
| 039916 | Timer A3 mode register | TA3MR | 0016 |
| 039A16 | Timer A4 mode register | TA4MR | 0016 |
| 039B16 | Timer B0 mode register | TB0MR | 00XX00002 |
| 039C16 | Timer B1 mode register | TB1MR | 00XX00002 |
| 039D16 | Timer B2 mode register | TB2MR | 00XX00002 |
| 039E16 | Timer B2 special mode register | TB2SC | X00000002 |
| 039F16 | | | |
| 03A016 | UART0 transmit/receive mode register | U0MR | 0016 |
| 03A116 | UART0 bit rate register | U0BRG | XX16 |
| 03A216 | UART0 transmit buffer register | U0TB | XXXXXXXX2 |
| 03A316 | | | XXXXXXXX2 |
| 03A416 | UART0 transmit/receive control register 0 | U0C0 | 000010002 |
| 03A516 | UART0 transmit/receive control register 1 | U0C1 | 000000102 |
| 03A616 | UART0 receive buffer register | U0RB | XXXXXXXX2 |
| 03A716 | | | XXXXXXXX2 |
| 03A816 | UART1 transmit/receive mode register | U1MR | 0016 |
| 03A916 | UART1 bit rate register | U1BRG | XX16 |
| 03AA16 | UART1 transmit buffer register | U1TB | XXXXXXXX2 |
| 03AB16 | | | XXXXXXXX2 |
| 03AC16 | UART1 transmit/receive control register 0 | U1C0 | 000010002 |
| 03AD16 | UART1 transmit/receive control register 1 | U1C1 | 000000102 |
| 03AE16 | UART1 receive buffer register | U1RB | XXXXXXXX2 |
| 03AF16 | | | XXXXXXXX2 |
| 03B016 | UART transmit/receive control register 2 | UCON | X00000002 |
| 03B116 | | | |
| 03B216 | | | |
| 03B316 | | | |
| 03B416 | CRC snoop address register | CRCSAR | XX16 |
| 03B516 | | | 00XXXXXX2 |
| 03B616 | CRC mode register | CRCMR | 0XXXXXX02 |
| 03B716 | | | |
| 03B816 | DMA0 request cause select register | DM0SL | 0016 |
| 03B916 | | | |
| 03BA16 | DMA1 request cause select register | DM1SL | 0016 |
| 03BB16 | | | |
| 03BC16 | CRC data register | CRCD | XX16 |
| 03BD16 | | | XX16 |
| 03BE16 | CRC input register | CRCIN | XX16 |
| 03BF16 | | | |

NOTE:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.6 SFR Information(6)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 03C0₁₆ | A/D register 0 | AD0 | XXXXXXXX₂ |
| 03C1₁₆ | | | XXXXXXXX₂ |
| 03C2₁₆ | A/D register 1 | AD1 | XXXXXXXX2 |
| 03C3₁₆ | | | XXXXXXXX₂ |
| 03C4₁₆ | A/D register 2 | AD2 | XXXXXXXX₂ |
| 03C5₁₆ | | | XXXXXXXX₂ |
| 03C6₁₆ | A/D register 3 | AD3 | XXXXXXXX₂ |
| 03C7₁₆ | | | XXXXXXXX₂ |
| 03C8₁₆ | A/D register 4 | AD4 | XXXXXXXX₂ |
| 03C9₁₆ | | | XXXXXXXX₂ |
| 03CA₁₆ | A/D register 5 | AD5 | XXXXXXXX₂ |
| 03CB₁₆ | | | XXXXXXXX₂ |
| 03CC₁₆ | A/D register 6 | AD6 | XXXXXXXX₂ |
| 03CD₁₆ | | | XXXXXXXX₂ |
| 03CE₁₆ | A/D register 7 | AD7 | XXXXXXXX₂ |
| 03CF₁₆ | | | XXXXXXXX₂ |
| 03D0₁₆ | | | |
| 03D1₁₆ | | | |
| 03D2₁₆ | A/D trigger control register | ADTRGCON | 00₁₆ |
| 03D3₁₆ | A/D status register 0 | ADSTAT0 | 00000X00₂ |
| 03D4₁₆ | A/D control register 2 | ADCON2 | 00₁₆ |
| 03D5₁₆ | | | |
| 03D6₁₆ | A/D control register 0 | ADCON0 | 00000XXX₂ |
| 03D7₁₆ | A/D control register 1 | ADCON1 | 00₁₆ |
| 03D8₁₆ | | | |
| 03D9₁₆ | | | |
| 03DA₁₆ | | | |
| 03DB₁₆ | | | |
| 03DC₁₆ | | | |
| 03DD₁₆ | | | |
| 03DE₁₆ | | | |
| 03DF₁₆ | | | |
| 03E0₁₆ | | | |
| 03E1₁₆ | Port P1 register | P1 | XX₁₆ |
| 03E2₁₆ | | | |
| 03E3₁₆ | Port P1 direction register | PD1 | 00₁₆ |
| 03E4₁₆ | | | |
| 03E5₁₆ | | | |
| 03E6₁₆ | | | |
| 03E7₁₆ | | | |
| 03E8₁₆ | | | |
| 03E9₁₆ | | | |
| 03EA₁₆ | | | |
| 03EB₁₆ | | | |
| 03EC₁₆ | Port P6 register | P6 | XX₁₆ |
| 03ED₁₆ | Port P7 register | P7 | XX₁₆ |
| 03EE₁₆ | Port P6 direction register | PD6 | 00₁₆ |
| 03EF₁₆ | Port P7 direction register | PD7 | 00₁₆ |
| 03F0₁₆ | Port P8 register | P8 | XX₁₆ |
| 03F1₁₆ | Port P9 register | P9 | XXXXXXXX₂ |
| 03F2₁₆ | Port P8 direction register | PD8 | 00₁₆ |
| 03F3₁₆ | Port P9 direction register | PD9 | XXXX0000₂ |
| 03F4₁₆ | Port P10 register | P10 | XX₁₆ |
| 03F5₁₆ | | | |
| 03F6₁₆ | Port P10 direction register | PD10 | 00₁₆ |
| 03F7₁₆ | | | |
| 03F8₁₆ | | | |
| 03F9₁₆ | | | |
| 03FA₁₆ | | | |
| 03FB₁₆ | | | |
| 03FC₁₆ | Pull-up control register 0 | PUR0 | 00₁₆ |
| 03FD₁₆ | Pull-up control register 1 | PUR1 | 00₁₆ |
| 03FE₁₆ | Pull-up control register 2 | PUR2 | 00₁₆ |
| 03FF₁₆ | Port control register | PCR | 00₁₆ |

NOTE:
1. Blank spaces are reserved. No access is allowed.

X: Undefined

| REVISION HISTORY | M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) Shortsheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.51 | 07/25/06 | - | First edition |