Renesas Electronics America Inc - M30260F8AGP#U3A Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, Voltage Detect, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30260f8agp-u3a

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1. Overview

The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M16C/60 Series CPU core. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is housed in 42-pin and 48-pin plastic molded packages. With a 1M byte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1 Applications

Audio, cameras, office/communications/portable/ equipment, air-conditioning equipment, home appliances, etc.

1.2 Performance Outline

Table 1.1 and **1.2** outline performance overview of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T).

Table 1.1. M16C/26A Group(M16C/26A, M16C/26B, M16C/26T) Performance (48-Pin Package)

Item		Specification
CPU	Basic instructions	91 instructions
	Minimun instruction execution time	41.7 ns (f(BCLK) = 24MHz(4), Vcc = 4.2 to 5.5 V) (M16C/26B) 50 ns (f(BCLK) = 20MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B, M16C/26T(T-ver.)) 100 ns (f(BCLK) = 10MHz, Vcc = 2.7 to 5.5 V) (M16C/26A , M16C/26B) 50 ns (f(BCLK) = 20MHz, Vcc = 4.2 to 5.5 V -40 to 105°C) (M16C/26T(V-ver.)) 62.5 ns (f(BCLK) = 16MHz, Vcc = 4.2 to 5.5 V -40 to 125°C) (M16C/26T(V-ver.))
	Operating mode	Single-chip mode
	Address space	1 Mbyte
	Memory capacity	See **1.4 Product Information**
Peripheral Function	I/O ports	39 I/O pins
	Multifunction timers	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase motor control timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I2C bus(1) , or IEBus(2))
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calcuration circuit	1 circuit (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupts	20 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock oscillation circuit(*), Sub-clock oscillation circuit(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip (M16C/26A, M16C/26B), not on-chip (M16C/26T)
Electrical Characteristics	Power supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(4) (M16C/26B) Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B) Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz) Vcc = 3.0 to 5.5 V (M16C/26T(T-ver.)) Vcc = 4.2 to 5.5 V (M16C/26T(V-ver.))
	Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3 V, in stop mode)
Flash Memory Version	Programming /erasure voltage	2.7 to 5.5 V (M16C/26A, M16C/26B) 3.0 to 5.5 V (M16C/26T(T-ver.)) 4.2 to 5.5 V (M16C/26T(V-ver.))
	Programming /erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B)(3)
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C (3) (M16C/26A , M16C/26B) -40 to 85°C (M16C/26T(T-ver.)) -40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package		48-pin plastic molded QFP

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin device)

	Item	Performance
CPU	Basic instructions	91 instructions
	Minimun instruction execution time	41.7 ns (f(BCLK) = 24 MHz (4), VCC = 4.2 to 5.5 V (M16C/26B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B) 100 ns (f(BCLK) = 10 MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
	Operation mode	Single-chip mode
	Address space	1M byte
	Memory capacity	See **1.4 Product Information**
Peripheral function	Port	33 I/O pins
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels Three-phase motor control timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I^2C bus(1) , or IEBus(2))
	A/D converter	10 bit A/D converter: 1 circuit, 10 channels
	DMAC	2 channels
	CRC calcuration circuit	1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip
Electrical Characteristics	Supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(4) (M16C/26B) Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B) Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
	Power Consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3 μA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (Vcc = 3 V, in stop mode)
Flash memory	Programming/erasure voltage	2.7 to 5.5 V
	Programming/erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B)(3)
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C (3)
Package		42-pin plastic molded SSOP

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 and **1.2** show block diagrams of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) 48-pin package and 42-pin package.

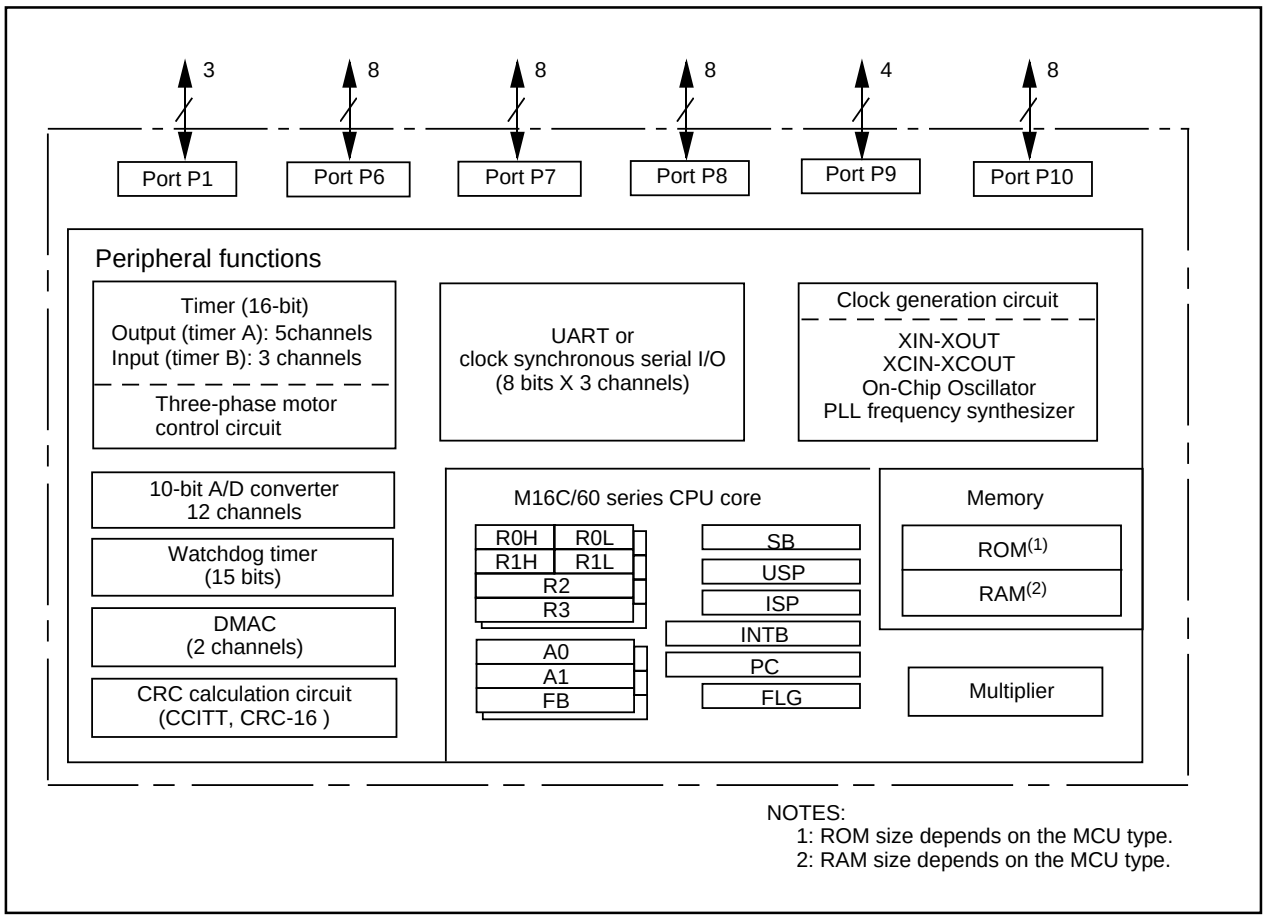


Figure 1.1 Block Diagram(48-pin Package)

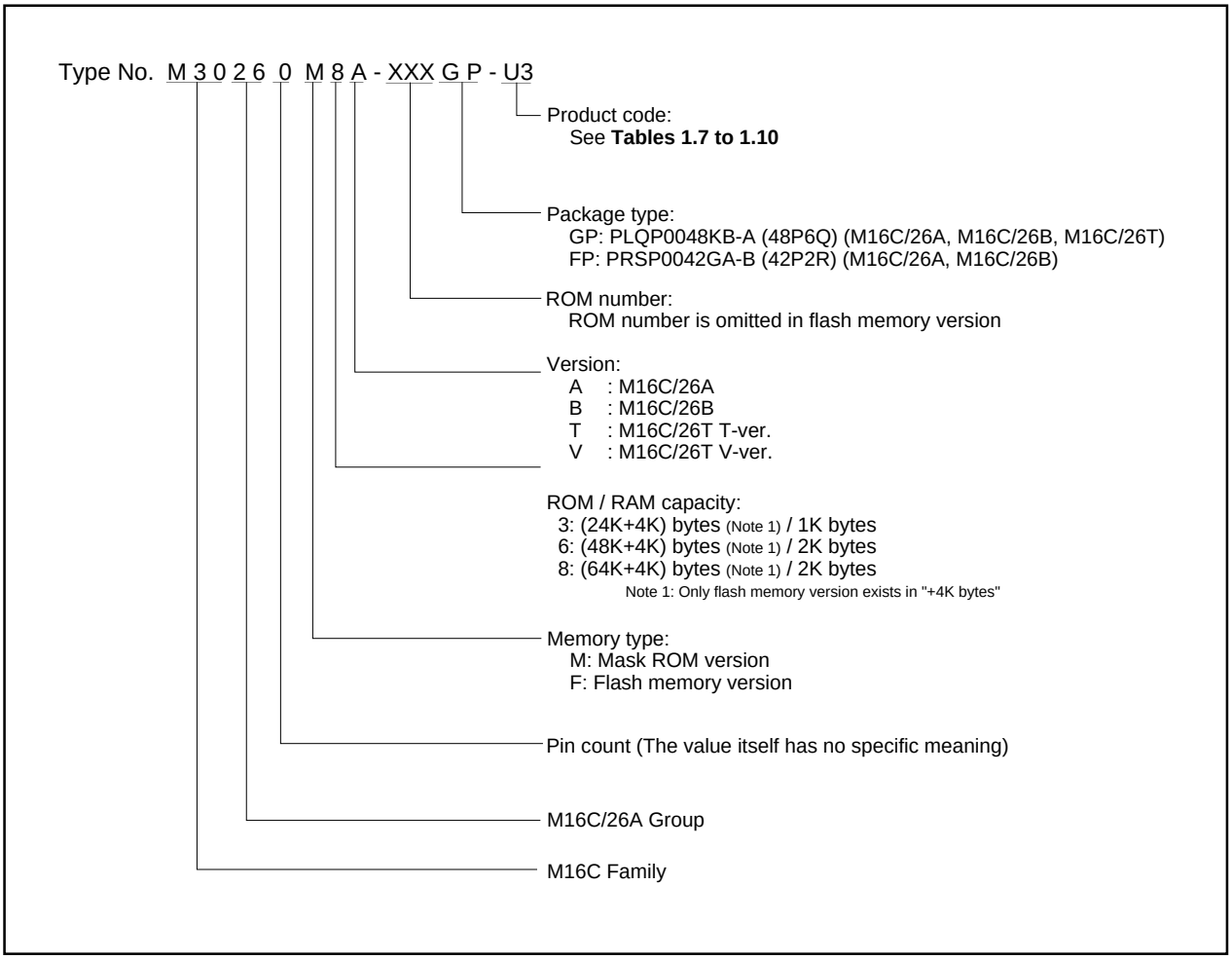


Figure 1.3 Product Numbering System

Table 1.7 Product Code (Flash Memory Version) - M16C/26A, M16C/26B

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5						-20 to 85°C
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

Table 1.8 Product Code (Mask ROM Version - M16C/26A)

Product Code	Package	Operating Ambient Temperature
U3	Lead free	-40°C to 85°C
U5		-20°C to 85°C

NOTE:

1. The lead contained products, D3, D5, D7, and D9 are put together with U3, U5, U7, and U9 respectively. Lead-free products can be mounted by both conventional Sn-Pb paste and Lead-free paste (Sn-Ag-Cu plating).

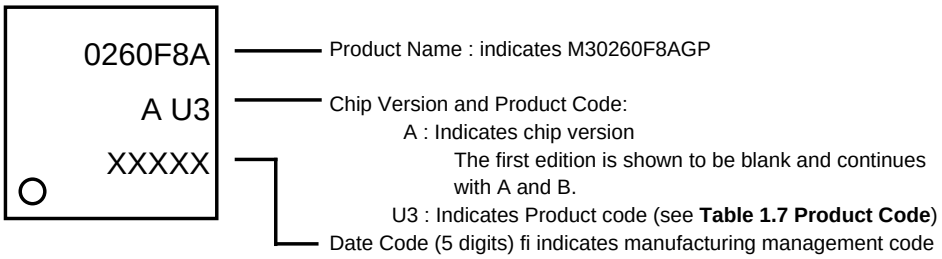
Table 1.9 Product Code (Flash Memory Version) - M16C/26T T-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temerature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 85°C	-40°C to 85°C
U7		1,000		10,000		

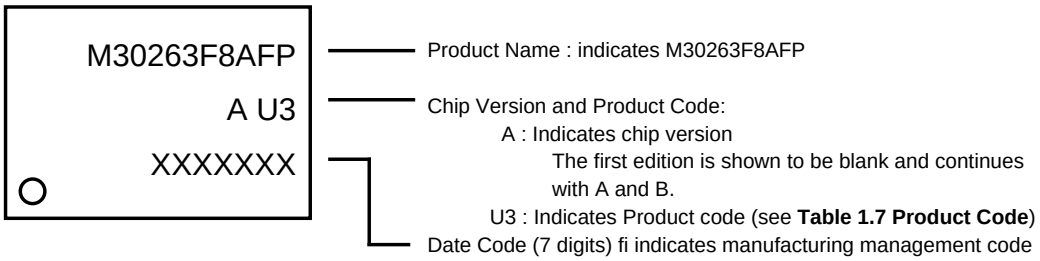
Table 1.10 Product Code (Flash Memory Version) - M16C/26T V-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temerature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 125°C	-40°C to 125°C
U7		1,000		10,000		

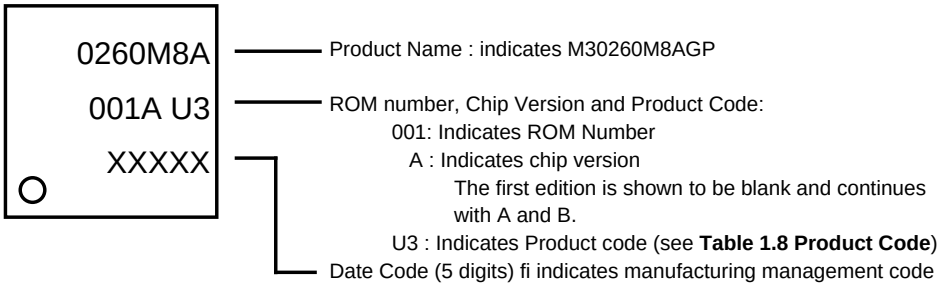
(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26A, M16C/26B



(2) Flash memory version, PRSP0042GA-B (42P2R), M16C/26A, M16C/26B



(3) MASK ROM version, PLQP0048KB-A (48P6Q), M16C/26A



(4) MASK ROM version, PRSP0042GA-B (42P2R), M16C/26A

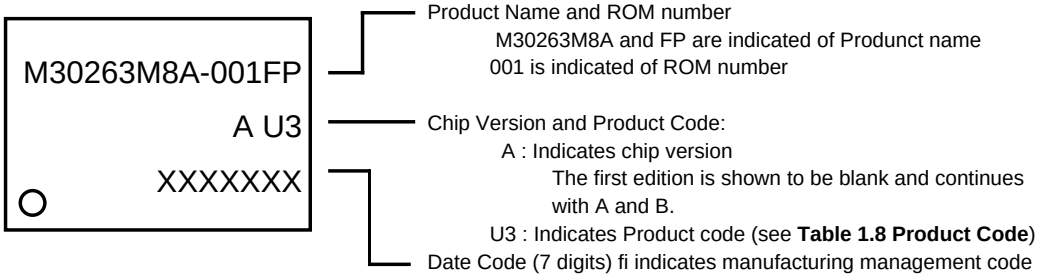
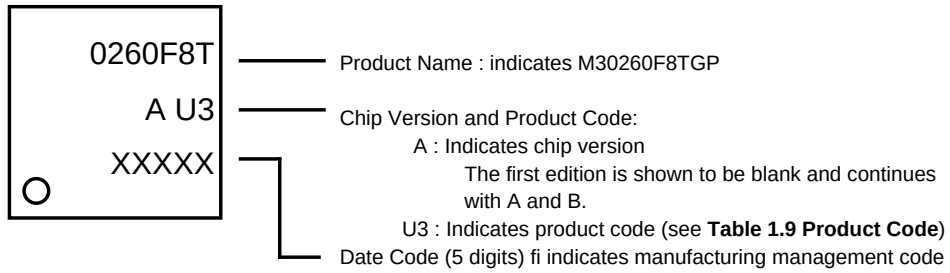


Figure 1.4 Marking Diagram (M16C/26A , M16C/26B)

(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T T-ver.



(2) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T V-ver.

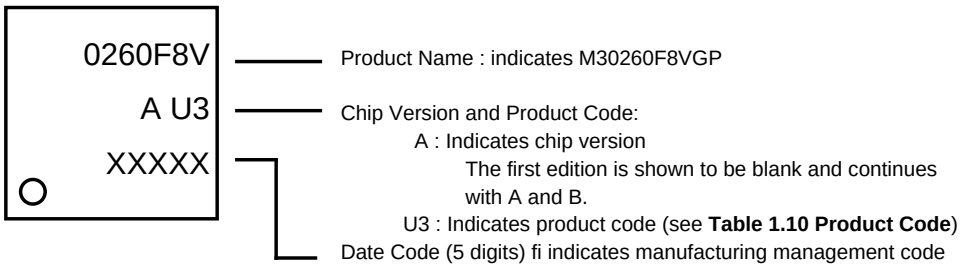


Figure 1.5 Marking Diagram (M16C/26T)

1.5 Pin Assignments

Figures 1.6 and **1.7** show the Pin Assignments (top view).

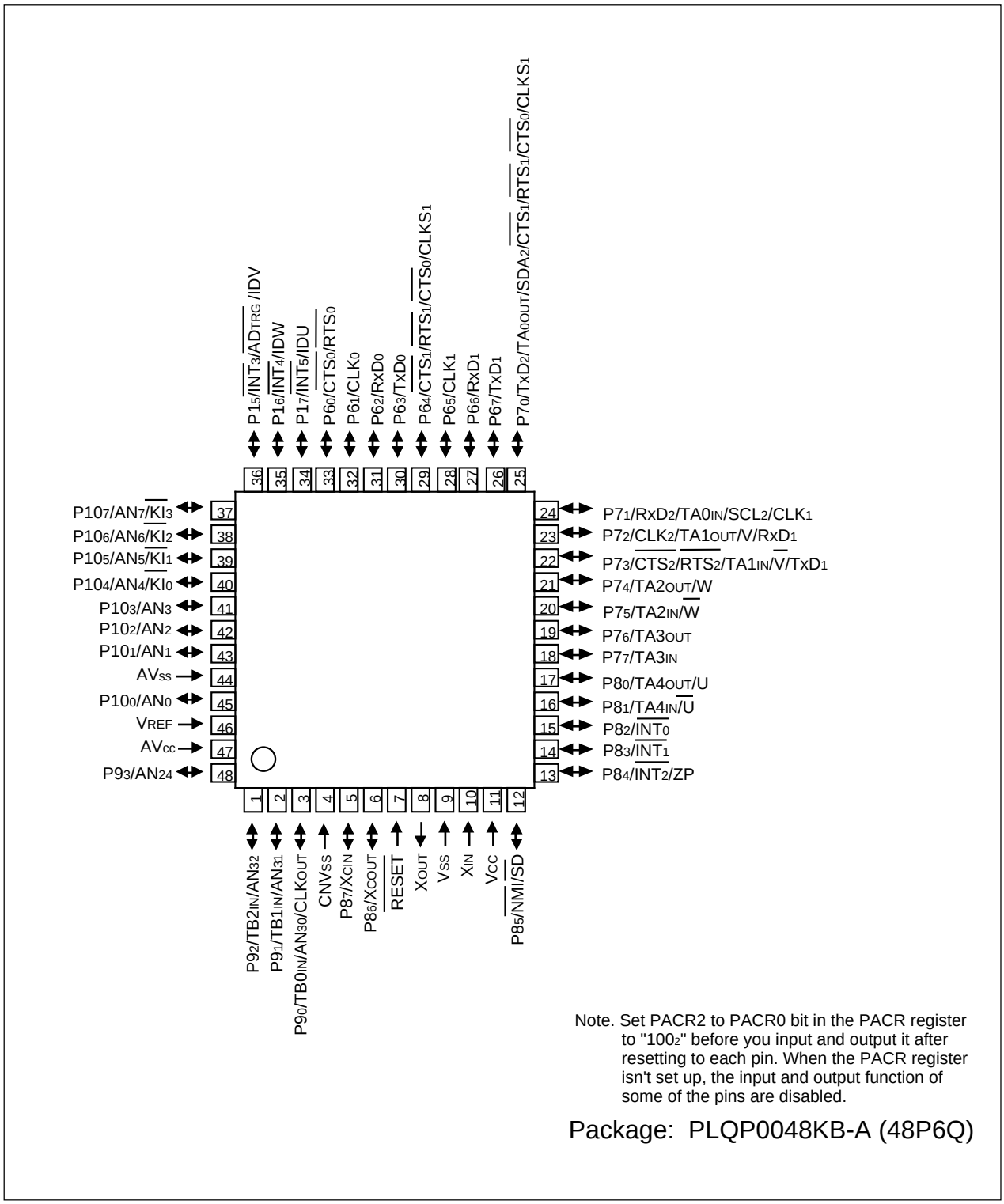
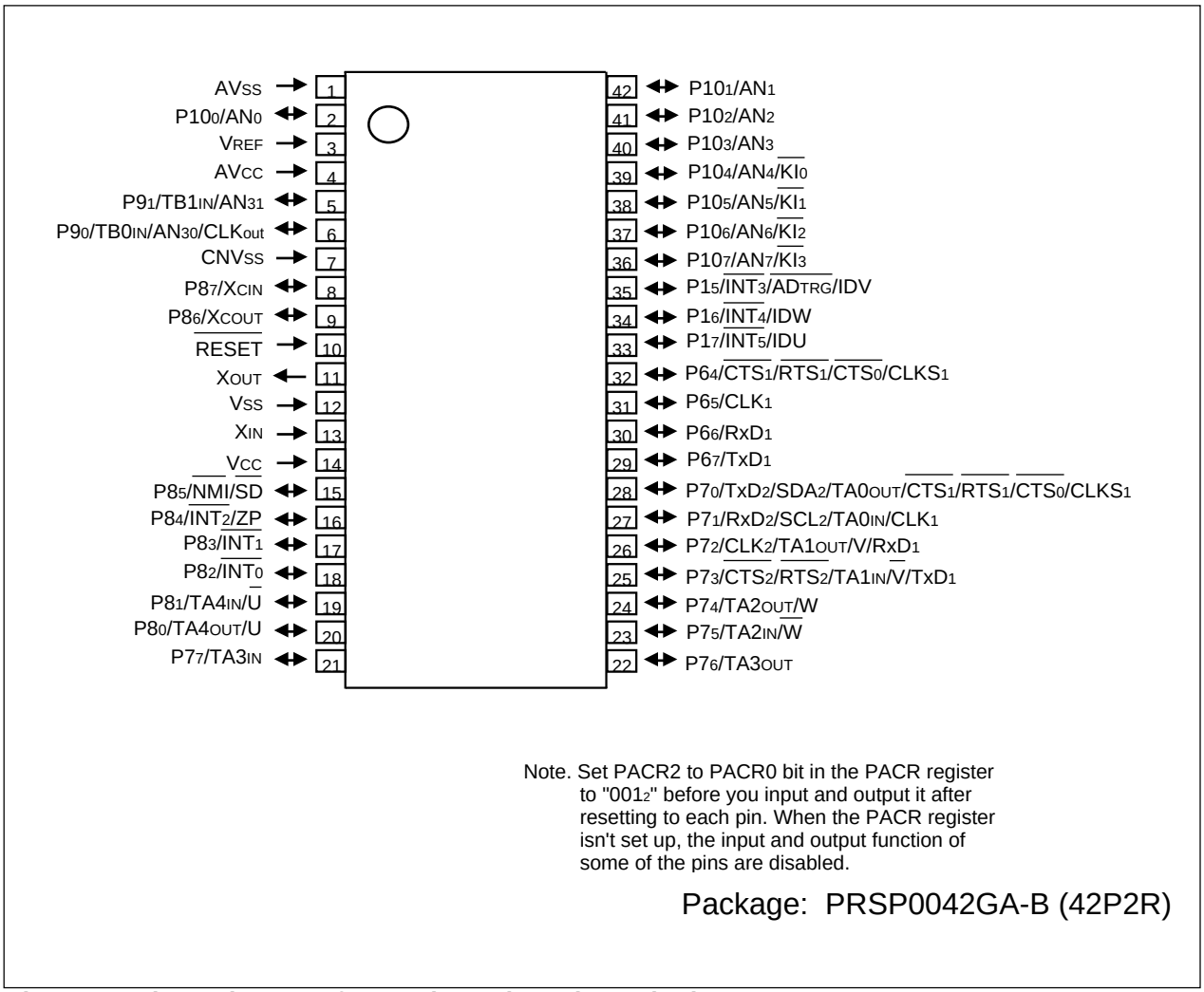


Figure 1.6 Pin Assignment for 48-Pin Package (Top View)



Note. Set PACR2 to PACR0 bit in the PACR register to "001_2" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PRSP0042GA-B (42P2R)

Figure 1.7 Pin Assignment for 42-Pin Package (Top View)

Table 1.12 Pin Characteristics for 42-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1	AVss					
2		P10$_0$				AN$_0$
3	VREF					
4	AVCC					
5		P9$_1$		TB$_{1IN}$		AN3$_1$
6		P9$_0$		TB$_{0IN}$	CLK$_{OUT}$	AN3$_0$
7	CNVss					
8	XCIN	P8$_7$				
9	XCOUT	P8$_6$				
10	$\overline{\text{RESET}}$					
11	XOUT					
12	Vss					
13	XIN					
14	VCC					
15		P8$_5$	$\overline{\text{NMI}}$	$\overline{\text{SD}}$		
16		P8$_4$	$\overline{\text{INT}}_2$	ZP		
17		P8$_3$	$\overline{\text{INT}}_1$			
18		P8$_2$	$\overline{\text{INT}}_0$			
19		P8$_1$		TA$_{4IN}$ / $\overline{\text{U}}$		
20		P8$_0$		TA$_{4OUT}$ / U		
21		P7$_7$		TA$_{3IN}$		
22		P7$_6$		TA$_{3OUT}$		
23		P7$_5$		TA$_{2IN}$ / $\overline{\text{W}}$		
24		P7$_4$		TA$_{2OUT}$ / W		
25		P7$_3$		TA$_{1IN}$ / $\overline{\text{V}}$	$\overline{\text{CTS}}_2$ / $\overline{\text{RTS}}_2$ / TxD$_1$	
26		P7$_2$		TA$_{1OUT}$ / V	CLK$_2$ / RxD$_1$	
27		P7$_1$		TA$_{0IN}$	RxD$_2$ / SCL$_2$ / CLK$_1$	
28		P7$_0$		TA$_{0OUT}$	TxD$_2$ / SDA$_2$ / $\overline{\text{RTS}}_1$ / $\overline{\text{CTS}}_1$ / $\overline{\text{CTS}}_0$ / CLKS$_1$	
29		P6$_7$			TxD$_1$	
30		P6$_6$			RxD$_1$	
31		P6$_5$			CLK$_1$	
32		P6$_4$			$\overline{\text{RTS}}_1$ / $\overline{\text{CTS}}_1$/ $\overline{\text{CTS}}_0$ / CLKS$_1$	
33		P1$_7$	$\overline{\text{INT}}_5$	IDU		
34		P1$_6$	$\overline{\text{INT}}_4$	IDW		
35		P1$_5$	$\overline{\text{INT}}_3$	IDV		$\overline{\text{ADTRG}}$
36		P10$_7$	$\overline{\text{KI}}_3$			AN$_7$
37		P10$_6$	$\overline{\text{KI}}_2$			AN$_6$
38		P10$_5$	$\overline{\text{KI}}_1$			AN$_5$
39		P10$_4$	$\overline{\text{KI}}_0$			AN$_4$
40		P10$_3$				AN$_3$
41		P10$_2$				AN$_2$
42		P10$_1$				AN$_1$

1.6 Pin Description

Table 1.13 Pin Description (48-Pin and 42-Pin Packages)

Classification	Pin Name	I/O Type	Description
Power Supply	VCC, VSS	I	Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (M16C/26A, M16C/26B), 3.0 to 5.5 V (M16C/26T T-ver.), 4.2 to 5.5 V (M16C/26T V-ver.)
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS
Reset Input	$\overline{\text{RESET}}$	I	The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock), connect XIN pin to VCC and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT
Sub Clock Output	XCOUT	O	
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as f1, f8, f32, or fC
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	$\overline{\text{NMI}}$ interrupt input pin. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB1IN	I	Timer B0 to B1 input pins
Three-Phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	I/O pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS1}}$ to $\overline{\text{CTS2}}$	I	Input pins to control data transmission
	$\overline{\text{RTS1}}$ to $\overline{\text{RTS2}}$	O	Output pins to control data reception
	CLK1 to CLK2	I/O	Inputs and outputs the transfer clock
	RxD1 to RxD2	I	Inputs serial data
	TxD1 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN30 to AN31	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$	I	Input pin for an external A/D trigger
I/O Ports	P15 to P17	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 3-bit units
	P64 to P67 P70 to P77 P80 to P87 P100 to P107 P90 to P91	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units

I : Input O : Output I/O : Input and output

Table 1.13 Pin Description (48-pin packages only) (Continued)

Classification	Pin Name	I/O Type	Description
Serial I/O	$\overline{CTS0}$	I	Inputs pin to control data transmission
	$\overline{RTS0}$	O	Output pin to control data reception
	CLK0	I/O	Inputs and outputs the transfer clock
	RxD0	I	Inputs serial data
	TxD0	O	Outputs serial data
Timer B	TB2IN	I	Timer B2 input pin
A/D Converter	$AN2_4$ $AN3_2$	I	Analog input pins for the A/D converter
I/O Ports	$P6_0$ to $P6_3$ $P9_2$ to $P9_3$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units

I : Input O : Output I/O : Input and output

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

3. Memory

Figure 3.1 is a memory map of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T). The M16C/26A Group provides 1-Mbyte address space addresses 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated lower address, beginning with address $FFFFF_{16}$. For example, a 64-Kbyte internal ROM area is allocated in addresses $F0000_{16}$ to $FFFFF_{16}$. The flash memory version has two sets of 2-Kbyte internal ROM area, block A and block B, for data space. These blocks are allocated addresses $F000_{16}$ to $FFFF_{16}$.

The fixed interrupt vectors are allocated addresses $FFFDC_{16}$ to $FFFFF_{16}$ and they store the start address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM area is allocated in addresses 00400_{16} to $007FF_{16}$. The internal RAM is used for temporarily storing data. The area is also used as stacks when subroutines are called or interrupt requests are acknowledged.

The SFR is allocated addresses 00000_{16} to $003FF_{16}$. The peripheral function control registers are allocated here. All blank spaces within SFR location are reserved and cannot be accessed by users.

The special page vectors are allocated addresses $FFE00_{16}$ to $FFFDB_{16}$. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M16C/60 and M16C/20 Series Software Manual** for details.

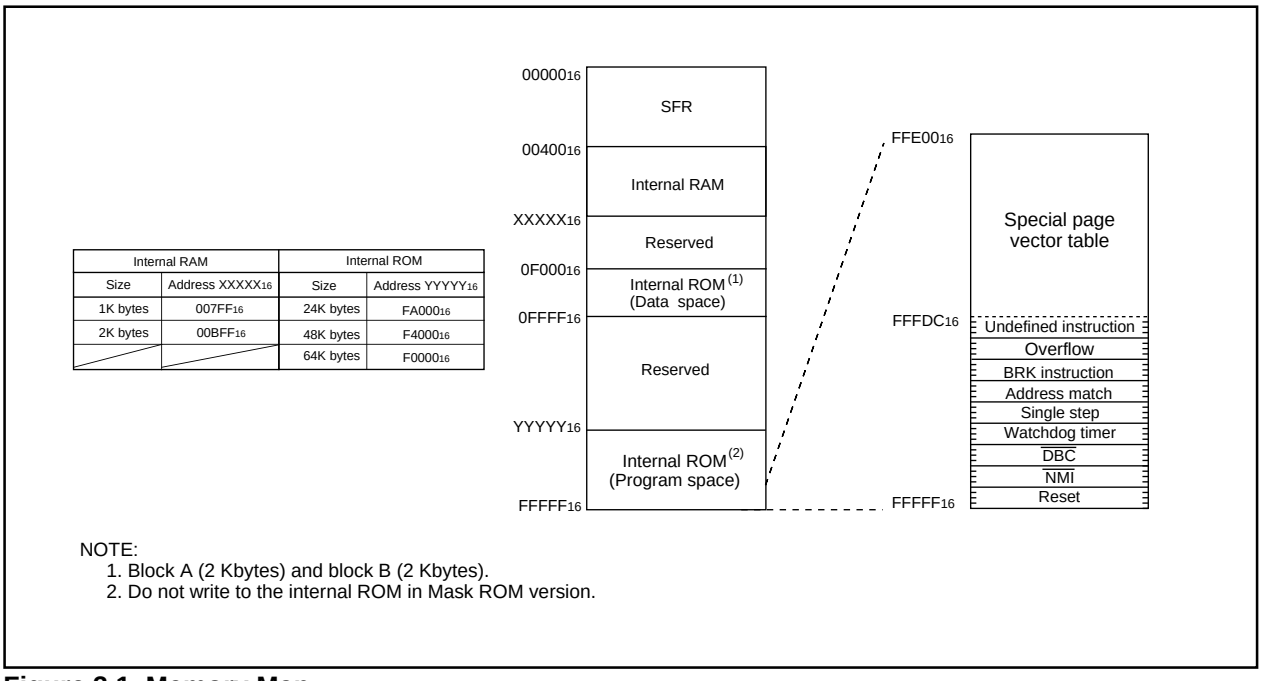


Figure 3.1 Memory Map

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	INT5 interrupt control register	INT5IC	XX00X000₂
0049₁₆	INT4 interrupt control register	INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A/D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	TimerA0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	TimerA1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	TimerA2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	TimerA3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	TimerA4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	TimerB0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	TimerB1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	TimerB2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00X000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

NOTE:
1. Blank spaces are reserved. No access is allowed.

X: Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
008016			
008116			
008216			
008316			
008416			
008516			
008616			
≈			≈
01B016			
01B116			
01B216			
01B316	Flash memory control register 4 (Note 2)	FMR4	010000002
01B416			
01B516	Flash memory control register 1 (Note 2)	FMR1	000XXX0X2
01B616			
01B716	Flash memory control register 0 (Note 2)	FMR0	0116
01B816			
01B916			
01BA16			
01BB16			
01BC16			
01BD16			
01BE16			
01BF16			
≈			≈
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16	Three phase protect control register	TPRC	0016
025B16			
025C16	On-chip oscillator control register	ROCR	000001012
025D16	Pin assignment control register	PACR	0016
025E16	Peripheral clock select register	PCLKR	000000112
025F16			
≈			≈
033016			
033116			
033216			
033316			
033416			
033516			
033616			
033716			
033816			
033916			
033A16			
033B16			
033C16			
033D16			
033E16	NMI digital debounce register	NDDR	FF16
033F16	Port17 digital debounce register	P17DDR	FF16

NOTES:
1. Blank spaces are reserved. No access is allowed.
2. This register is included in the flash memory version.

X: Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
034016			
034116			
034216	Timer A1-1 register	TA11	XX16
034316			XX16
034416	Timer A2-1 register	TA21	XX16
034516			XX16
034616	Timer A4-1 register	TA41	XX16
034716			XX16
034816	Three phase PWM control register 0	INVC0	0016
034916	Three phase PWM control register 1	INVC1	0016
034A16	Three phase output buffer register 0	IDB0	3F16
034B16	Three phase output buffer register 1	IDB1	3F16
034C16	Dead time timer	DTT	XX16
034D16	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX16
034E16	Position-data-retain function control register	PDRF	XXXX00002
034F16			
035016			
035116			
035216			
035316			
035416			
035516			
035616			
035716			
035816	Port function control register	PFCR	001111112
035916			
035A16			
035B16			
035C16			
035D16			
035E16	Interrupt request cause select register 2	IFSR2A	XXXXXXX02
035F16	Interrupt request cause select register	IFSR	0016
036016			
036116			
036216			
036316			
036416			
036516			
036616			
036716			
036816			
036916			
036A16			
036B16			
036C16			
036D16			
036E16			
036F16			
037016			
037116			
037216			
037316			
037416	UART2 special mode register 4	U2SMR4	0016
037516	UART2 special mode register 3	U2SMR3	000X0X0X2
037616	UART2 special mode register 2	U2SMR2	X00000002
037716	UART2 special mode register	U2SMR	X00000002
037816	UART2 transmit/receive mode register	U2MR	0016
037916	UART2 bit rate register	U2BRG	XX16
037A16	UART2 transmit buffer register	U2TB	XXXXXXXX2
037B16			XXXXXXXX2
037C16	UART2 transmit/receive control register 0	U2C0	000010002
037D16	UART2 transmit/receive control register 1	U2C1	000000102
037E16	UART2 receive buffer register	U2RB	XXXXXXXX2
037F16			XXXXXXXX2

NOTE:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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