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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f85j10t-i-pt

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4.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Two bits indicate the current clock source and its status: OSTS (OSCCON<3>) and T1RUN (T1CON<6>). In general, only one of these bits will be set while in a given power-managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock. If neither of these bits is set, INTRC is clocking the device.

Note: Executing a SLEEP instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode or one of the Idle modes, depending on the setting of the IDLEN bit.

4.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power-managed mode specified by the new setting.

4.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

4.2.1 PRI_RUN MODE

The PRI_RUN mode is the normal, full-power execution mode of the microcontroller. This is also the default mode upon a device Reset unless Two-Speed Start-up is enabled (see **Section 24.4 "Two-Speed Start-up"** for details). In this mode, the OSTS bit is set. (see **Section 3.6.1 "Oscillator Control Register"**).

4.2.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high-accuracy clock source.

SEC_RUN mode is entered by setting the SCS<1:0> bits to '01'. The device clock source is switched to the Timer1 oscillator (see Figure 4-1), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

TADLE V-2.				
Register	Applicable Devices	Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TRISJ	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	սսսս սսսս
TRISH	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	սսսս սսսս
TRISG	PIC18F6XJ1X PIC18F8XJ1X	1 1111	1 1111	u uuuu
TRISF	PIC18F6XJ1X PIC18F8XJ1X	1111 111-	1111 111-	นนนน นนน-
TRISE	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	นนนน นนนน
TRISD	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	นนนน นนนน
TRISC	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	นนนน นนนน
TRISB	PIC18F6XJ1X PIC18F8XJ1X	1111 1111	1111 1111	นนนน นนนน
TRISA	PIC18F6XJ1X PIC18F8XJ1X	11 1111	11 1111	uu uuuu
LATJ	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	นนนน นนนน	นนนน นนนน
LATH	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	นนนน นนนน	นนนน นนนน
LATG	PIC18F6XJ1X PIC18F8XJ1X	x xxxx	u uuuu	u uuuu
LATF	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXX-	uuuu uuu-	uuuu uuu-
LATE	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
LATD	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
LATC	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
LATB	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
LATA	PIC18F6XJ1X PIC18F8XJ1X	xx xxxx	uu uuuu	uu uuuu
PORTJ	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTH	PIC18F6XJ1X PIC18F8XJ1X	0000 xxxx	นนนน นนนน	นนนน นนนน
PORTG	PIC18F6XJ1X PIC18F8XJ1X	111x xxxx	111u uuuu	սսսս սսսս
PORTF	PIC18F6XJ1X PIC18F8XJ1X	x000 000-	x000 000-	uuuu uuu-
PORTE	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTD	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTC	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTB	PIC18F6XJ1X PIC18F8XJ1X	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTA	PIC18F6XJ1X PIC18F8XJ1X	0x 0000	0u 0000	uu uuuu
SPBRGH1	PIC18F6XJ1X PIC18F8XJ1X	0000 0000	0000 0000	นนนน นนนน
BAUDCON1	PIC18F6XJ1X PIC18F8XJ1X	01-0 0-00	01-0 0-00	uu-u u-uu
SPBRG2	PIC18F6XJ1X PIC18F8XJ1X	0000 0000	0000 0000	นนนน นนนน
BAUDCON2	PIC18F6XJ1X PIC18F8XJ1X	01-0 0-00	01-0 0-00	uu-u u-uu

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

- 3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
- 4: See Table 5-1 for Reset value for specific condition.

NOTES:

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
OSCFIE	CMIE	—	_	BCL1IE	_	TMR3IE	CCP2IE
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	Iown
bit 7	OSCFIE: Osc	cillator Fail Inter	rupt Enable b	it			
	1 = Enabled						
	0 = Disabled						
bit 6	CMIE: Compa	arator Interrupt	Enable bit				
	1 = Enabled						
	0 = Disabled						
bit 5-4	Unimplemen	ted: Read as '	0'				
bit 3	BCL1IE: Bus	Collision Interr	upt Enable bit	t (MSSP1 mod	lule)		
	1 = Enabled						
	0 = Disabled						
bit 2	bit 2 Unimplemented: Read as '0'						
bit 1	TMR3IE: TM	R3 Overflow Inf	errupt Enable	bit			
1 = Enabled							
	0 = Disabled						
bit 0	CCP2IE: ECO	CP2 Interrupt E	nable bit				
	1 = Enabled						
	0 = Disabled						

REGISTER 10-8: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

11.3 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). All pins on PORTB are digital only and tolerate voltages up to 5.5V.

The Output Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

EXAMPLE 11-2: INITIALIZING PORTB

CLRF	PORTB	; Initialize PORTB by
		; clearing output
		; data latches
CLRF	LATB	; Alternate method
		; to clear output
		; data latches
MOVLW	OCFh	; Value used to
		; initialize data
		; direction
MOVWF	TRISB	; Set RB<3:0> as inputs
		; RB<5:4> as outputs
		; RB<7:6> as inputs

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn <u>on all</u> the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of the PORTB pins (RB<7:4>) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB<7:4> pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

This interrupt can wake the device from power-managed modes. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB (except with the MOVFF (ANY), PORTB instruction). This will end the mismatch condition.
- b) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

For 80-pin devices, RB3 can be configured as the alternate peripheral pin for the ECCP2 module and Enhanced PWM Output 2A by clearing the CCP2MX Configuration bit. This applies only to 80-pin devices operating in Extended Microcontroller mode. If the device is in Microcontroller mode, the alternate assignment for ECCP2 is RE7. As with other ECCP2 configurations, the user must ensure that the TRISB<3> bit is set appropriately for the intended operation.

18.4.5 FULL-BRIDGE MODE

In Full-Bridge Output mode, four pins are used as outputs; however, only two outputs are active at a time. In the Forward mode, pin P1A is continuously active and pin P1D is modulated. In the Reverse mode, pin P1C is continuously active and pin P1B is modulated. These are illustrated in Figure 18-6. P1A, P1B, P1C and P1D outputs are multiplexed with the port pins as described in Table 18-1, Table 18-2 and Table 18-3. The corresponding TRIS bits must be cleared to make the P1A, P1B, P1C and P1D pins outputs.





The P1A, P1B, P1C and P1D output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pins for output at the same time as the ECCP1 module may cause damage to the application circuit. The ECCP1 module must be enabled in the proper output mode and complete a full PWM cycle before configuring the PWM pins as outputs. The completion of a full PWM cycle is indicated by the TMR2IF bit being set as the second PWM period begins.

FIGURE 18-10: PWM AUTO-SHUTDOWN (P1RSEN = 1, AUTO-RESTART ENABLED)



FIGURE 18-11: PWM AUTO-SHUTDOWN (P1RSEN = 0, AUTO-RESTART DISABLED)



REGISTER 19-5: SSPxCON2: MSSPx CONTROL REGISTER 2 (I²C[™] MODE) (CONTINUED)

bit 1	RSEN/ADMSK1: Repeated Start Condition Enable bit
	 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Automatically cleared by hardware. 0 = Repeated Start condition Idle
	In Slave mode (7-Bit Addressing mode): 1 = Address masking of ADD1 enabled 0 = Address masking of ADD1 disabled
	In Slave mode (10-Bit Addressing mode): 1 = Address masking of ADD1 and ADD0 enabled 0 = Address masking of ADD1 and ADD0 disabled
bit 0	SEN: Start Condition Enable/Stretch Enable bit ⁽²⁾
	In Master mode: 1 = Initiate Start condition on SDAx and SCLx pins. Automatically cleared by hardware. 0 = Start condition Idle
	In Slave mode: 1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled) 0 = Clock stretching is disabled

- **Note 1:** Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
 - 2: For bits, ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is active, these bits may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

19.4.2 OPERATION

The MSSP module functions are enabled by setting MSSP Enable bit, SSPEN (SSPxCON1<5>).

The SSPxCON1 register allows control of the I^2C operation. Four mode selection bits (SSPxCON1<3:0>) allow one of the following I^2C modes to be selected:

- I²C Master mode, clock
- I²C Slave mode (7-bit addressing)
- I²C Slave mode (10-bit addressing)
- I²C Slave mode (7-bit addressing) with Start and Stop bit interrupts enabled
- I²C Slave mode (10-bit addressing) with Start and Stop bit interrupts enabled
- I²C Firmware Controlled Master mode, slave is Idle

Selection of any I²C mode with the SSPEN bit set forces the SCLx and SDAx pins to be open-drain, provided these pins are programmed as inputs by setting the appropriate TRISC or TRISD bits. To ensure proper operation of the module, pull-up resistors must be provided externally to the SCLx and SDAx pins.

19.4.3 SLAVE MODE

In Slave mode, the SCLx and SDAx pins must be configured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

The I^2C Slave mode hardware will always generate an interrupt on an address match. Address masking will allow the hardware to generate an interrupt for more than one address (up to 31 in 7-bit addressing and up to 63 in 10-bit addressing). Through the mode select bits, the user can also choose to interrupt on Start and Stop bits.

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPxBUF register with the received value currently in the SSPxSR register.

Any combination of the following conditions will cause the MSSP module not to give this ACK pulse:

- The Buffer Full bit, BF (SSPxSTAT<0>), was set before the transfer was received.
- The overflow bit, SSPOV (SSPxCON1<6>), was set before the transfer was received.

In this case, the SSPxSR register value is not loaded into the SSPxBUF, but bit, SSPxIF, is set. The BF bit is cleared by reading the SSPxBUF register, while bit, SSPOV, is cleared through software.

The SCLx clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification, as well as the requirement of the MSSP module, are shown in timing parameter 100 and parameter 101.

19.4.3.1 Addressing

Once the MSSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8 bits are shifted into the SSPxSR register. All incoming bits are sampled with the rising edge of the clock (SCLx) line. The value of register, SSPxSR<7:1>, is compared to the value of the SSPxADD register. The address is compared on the falling edge of the eighth clock (SCLx) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

- 1. The SSPxSR register value is loaded into the SSPxBUF register.
- 2. The Buffer Full bit, BF, is set.
- 3. An ACK pulse is generated.
- 4. The MSSP Interrupt Flag bit, SSPxIF, is set (and interrupt is generated, if enabled) on the falling edge of the ninth SCLx pulse.

In 10-Bit Addressing mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit, R/\overline{W} (SSPxSTAT<2>), must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A9 A8 0', where 'A9' and 'A8' are the two MSbs of the address. The sequence of events for 10-bit addressing is as follows, with steps 7 through 9 for the slave-transmitter:

- 1. Receive first (high) byte of address (bits, SSPxIF, BF and UA, are set on address match).
- 2. Update the SSPxADD register with second (low) byte of address (clears bit, UA, and releases the SCLx line).
- 3. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.
- 4. Receive second (low) byte of address (bits, SSPxIF, BF and UA, are set).
- 5. Update the SSPxADD register with the first (high) byte of address. If match releases the SCLx line, this will clear bit, UA.
- 6. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.
- 7. Receive Repeated Start condition.
- 8. Receive first (high) byte of address (bits, SSPxIF and BF, are set).
- 9. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.

19.4.12 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit. ACKEN (SSPxCON2<4>). When this bit is set, the SCLx pin is pulled low and the contents of the Acknowledge data bit are presented on the SDAx pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCLx pin is deasserted (pulled high). When the SCLx pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCLx pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into an inactive state (Figure 19-25).

19.4.12.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

19.4.13 STOP CONDITION TIMING

A Stop bit is asserted on the SDAx pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN (SSPxCON2<2>). At the end of a receive/transmit, the SCLx line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDAx line low. When the SDAx line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCLx pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDAx pin will be deasserted. When the SDAx pin is sampled high while SCLx is high, the P bit (SSPxSTAT<4>) is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 19-26).

19.4.13.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 19-25: ACKNOWLEDGE SEQUENCE WAVEFORM



FIGURE 19-26: STOP CONDITION RECEIVE OR TRANSMIT MODE



19.4.14 SLEEP OPERATION

While in Sleep mode, the I^2C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

19.4.15 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

19.4.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit (SSPxSTAT<4>) is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the MSSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDAx line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- · Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

19.4.17 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDAx pin, arbitration takes place when the master outputs a '1' on SDAx, by letting SDAx float high and another master asserts a '0'. When the SCLx pin floats high, data should be stable. If the expected data on SDAx is a '1' and the data sampled on the SDAx pin = 0, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF, and reset the I²C port to its Idle state (Figure 19-27).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDAx and SCLx lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDAx and SCLx lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDAx and SCLx pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 19-27: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AVDD and AVSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF- pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of



FIGURE 21-1: A/D BLOCK DIAGRAM

the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted. The value in the ADRESH:ADRESL register pair is not modified for a Power-on Reset. These registers will contain unknown data after a Power-on Reset.

The block diagram of the A/D module is shown in Figure 21-1.

REGISTER 24-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

					•		,
R/WO-1	R/WO-1	R/WO-1	U-0	U-0	U-0	U-0	R/WO-1
DEBUG	XINST	STVREN	—	_	—	_	WDTEN
bit 7							bit 0
1							
Legena:							
R = Readable	bit	WO = Write-C	once bit	U = Unimpler	mented bit, read	as '0'	
-n = Value whe	en device is unp	programmed		'1' = Bit is se	t	'0' = Bit is clea	ared
bit 7	DEBUG: Bac	kground Debug	gger Enable bi	t			
	1 = Backgrou	and debugger o	lisabled; RB6	and RB7 confi	igured as genera	al purpose I/O	pins
	0 = Backgrou	and debugger e	enabled; RB6 a	and RB7 are d	ledicated to In-C	Circuit Debug	
bit 6	XINST: Exten	ded Instruction	Set Enable b	it			
	1 = Instructio	n set extensior	n and Indexed	Addressing m	ode enabled		
	0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)						
bit 5	STVREN: Sta	ck Overflow/U	nderflow Rese	t Enable bit			
	1 = Reset on stack overflow/underflow enabled						
	0 = Reset on stack overflow/underflow disabled						
bit 4-1 Unimplemented: Read as '0'							
bit 0 WDTEN: Watchdog Timer Enable bit							
	1 = WDT ena	abled					
	0 = WDT disa	abled (control i	s placed on S	WDTEN bit)			

REGISTER 24-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

U-0	U-0	U-0	U-0	U-0	R/WO-1	U-0	U-0
—	—	—	—	(1)	CP0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read	d as '0'
-n = Value when device is unprogrammed		'1' = Bit is set	'0' = Bit is cleared

bit 7-3 Unimplemented: Read as '0'

bit 2 CP0: Code Protection bit

- 1 = Program memory is not code-protected
- 0 = Program memory is code-protected
- bit 1-0 Unimplemented: Read as '0'

Note 1: This bit should always be maintained as '0'.

TABLE 25-2: PIC18F87J10 FAMILY INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	16-bit Instruction Word				Status	Notoo	
		Description	Cycles	MSb			LSb	Affected	Notes	
BYTE-OR	IENTED	OPERATIONS								
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2	
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2	
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1,2	
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2	
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2	
CPFSEQ	f, a	Compare f with WREG, Skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4	
CPFSGT	f, a	Compare f with WREG, Skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4	
CPFSLT	f, a	Compare f with WREG, Skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2	
DECF	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4	
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4	
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2	
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4	
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4	
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2	
IORWF	f, d, a	Inclusive OR WREG with f	1	0001	00da	ffff	ffff	Z, N	1, 2	
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z, N	1	
MOVFF	f_s, f_d	Move f _s (source) to 1st word	2	1100	ffff	ffff	ffff	None		
	5° u	f _d (destination) 2nd word		1111	ffff	ffff	ffff			
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None		
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1, 2	
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N		
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1, 2	
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	,	
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	Ć, Z, N		
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N		
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	1, 2	
SUBFWB	f, d, a	Subtract f from WREG with	1	0101	01da	ffff	ffff	C, DC, Z, OV, N	,	
		Borrow								
SUBWF	f. d. a	Subtract WREG from f	1	0101	11da	ffff	ffff	C. DC. Z. OV. N	1.2	
SUBWFB	f, d, a	Subtract WREG from f with	1	0101	10da	ffff	ffff	C, DC, Z, OV, N		
	, , -	Borrow								
SWAPF	f, d, a	Swap Nibbles in f	1	0011	10da	ffff	ffff	None	4	
TSTFSZ	f, a	Test f, Skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2	
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N		

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

TBLWT	Table Wri	te			
Syntax:	TBLWT (*	*; *+; *-; +*	f)		
Operands:	None				
Operation:	if TBLWT*, (TABLAT) \rightarrow Holding Register, TBLPTR – No Change; if TBLWT*+, (TABLAT) \rightarrow Holding Register, (TBLPTR) + 1 \rightarrow TBLPTR; if TBLWT*-, (TABLAT) \rightarrow Holding Register, (TBLPTR) – 1 \rightarrow TBLPTR; if TBLWT+*, (TBLPTR) + 1 \rightarrow TBLPTR,				
Status Affected:	None	·	0 0		
Encoding:	0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*	
Description:	This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to Section 6.0 "Memory Organization" for additional details on programming Flash memory.) The TBLPTR (a 21-bit pointer) points to each byte in the program memory.				
	The LSb of byte of the access.	of the TBLI e program	PTR select memory le	ets which ocation to	
	TBLPT	R[0] = 0:	Least Sigr of Prograr Word	nificant Byte m Memory	
	TBLPT	R[0] = 1:	Most Sign of Prograr Word	ificant Byte n Memory	
	The TBLWT instruction can modify the value of TBLPTR as follows: no change post-increment post-decrement pre-increment 				
Words:	1				
Cycles:	2				
Q Cycle Activity:					
	Q1	Q2	Q3	Q4	
	Decode	No operation	No operation	No operation	
	No	No	No	No	
	operation	operation (Read TABLAT)	operation	operation (Write to Holding Register)	

TBLWT Table Write (Continued)

Example 1: TBLWT *+;		
Before Instruction		
TABLAT	= 55	h
	= 00.	A356h
(00A356h)	.r. = FF	h
After Instructions (table w	rite completio	on)
TABLAT	= 55	h
	= 00.	A357h
(00A356h)	.r. = 55	h
Example 2: TBLWT +*;		
Before Instruction		
TABLAT	= 34	h
	= 01	389Ah
(01389Ah)	.r. = FF	h
HOLDING REGISTE	R	
(01389Bh)	= FF	h
After Instruction (table wri	te completion	ר)
TABLAT	= 34	h
	= 01	389Bh
(01389Ah)		h
HOLDING REGISTE	R	
(01389Bh)	= 34	n

FIGURE 27-2: PIC18F87J10 FAMILY VOLTAGE-FREQUENCY GRAPH, REGULATOR ENABLED (INDUSTRIAL)



27.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 27-5 apply to all timing specifications unless otherwise noted. Figure 27-3 specifies the load conditions for the timing specifications.

TABLE 27-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions (unless otherwise stated)			
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial			
	Operating voltage VDD range as described in DC spec Section 27.1 and			
	Section 27.3.			

FIGURE 27-3: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS





FIGURE 27-16: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)

TABLE 27-19: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{\operatorname{SSx}} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input		Тсү		ns	
71	TscH	SCKx Input High Time	Continuous	1.25 Tcy + 30	l	ns	
71A		(Slave mode)	Single Byte	40	—	ns	(Note 1)
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	_	ns	(Note 1)
73A	Тв2в	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 Tcy + 40	_	ns	(Note 2)
74	TscH2dlL, TscL2dlL	Hold Time of SDIx Data Input to SCKx Edge		20	-	ns	
75	TDOR	SDOx Data Output Rise Time		—	25	ns	
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	SSx ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge		—	50	ns	
82	TssL2DoV	SDOx Data Output Valid after $\overline{SSx} \downarrow Edge$		_	50	ns	
83	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge		1.5 Tcy + 40		ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

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PART NO.	<u>x /xx xxx</u>	Examples:
Device	Temperature Package Pattern Range	 a) PIC18F86J10-I/PT 301 = Industrial temp., TQFP package, QTP pattern #301. b) PIC18F65J15T-I/PT = Tape and reel, Industrial temp., TQFP package.
Device	PIC18F65J10/65J15/66J10/66J15/67J10 ⁽¹⁾ , PIC18F85J10/85J15/86J10/86J15/87J10 ⁽¹⁾ , PIC18F65J10/65J15/66J10/66J15/67J10T ⁽²⁾ , PIC18F85J10/85J15/86J10/86J15/87J10T ⁽²⁾	
Temperature Range	I = -40° C to $+85^{\circ}$ C (Industrial)	
Package	PT = TQFP (Thin Quad Flatpack)	
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	Note 1: F = Standard Voltage Range 2: T = in tape and reel