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Details

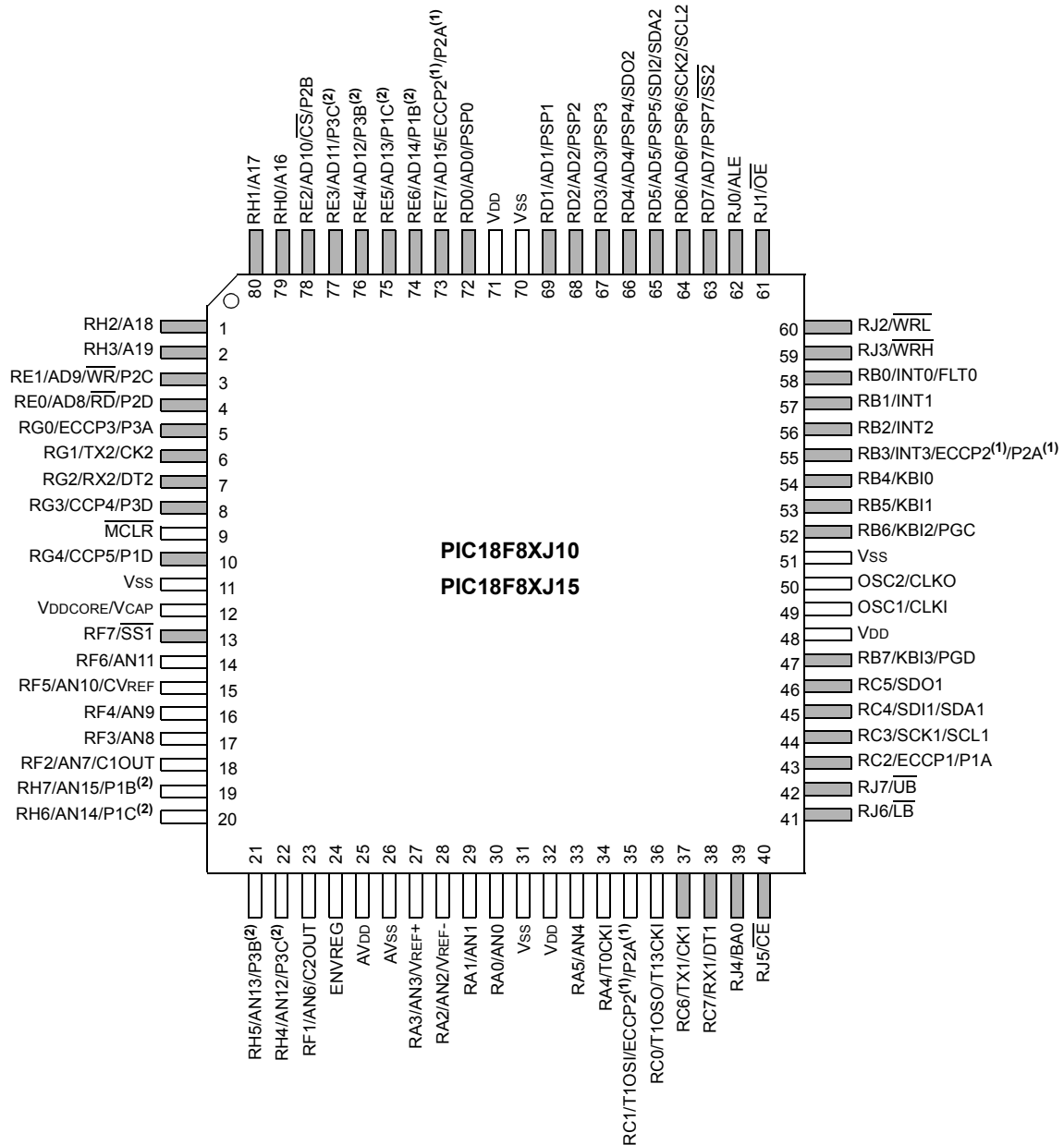
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f86j15-i-pt

PIC18F87J10 FAMILY

Pin Diagrams (Continued)

80-Pin TQFP

 Pins are up to 5.5V tolerant



Note 1: The ECCP2/P2A pin placement depends on the setting of the CCP2MX Configuration bit and the program memory mode.
Note 2: P1B, P1C, P3B and P3C pin placement depends on the setting of the ECCPMX Configuration bit.

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TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/ECCP3/P3A RG0 ECCP3 P3A	3	I/O I/O O	ST ST —	PORTG is a bidirectional I/O port. Digital I/O. Capture 3 input/Compare 3 output/PWM 3 output. ECCP3 PWM output A.
RG1/TX2/CK2 RG1 TX2 CK2	4	I/O O I/O	ST — ST	Digital I/O. EUSART2 asynchronous transmit. EUSART2 synchronous clock (see related RX2/DT2).
RG2/RX2/DT2 RG2 RX2 DT2	5	I/O I I/O	ST ST ST	Digital I/O. EUSART2 asynchronous receive. EUSART2 synchronous data (see related TX2/CK2).
RG3/CCP4/P3D RG3 CCP4 P3D	6	I/O I/O O	ST ST —	Digital I/O. Capture 4 input/Compare 4 output/PWM 4 output. ECCP3 PWM output D.
RG4/CCP5/P1D RG4 CCP5 P1D	8	I/O I/O O	ST ST —	Digital I/O. Capture 5 input/Compare 5 output/PWM 5 output. ECCP1 PWM output D.
Vss	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for peripheral digital logic and I/O pins.
AVss	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP VDDCORE VCAP	10	P P	— —	Core logic power or external filter capacitor connection. Positive supply for microcontroller core logic (regulator disabled). External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C/SMB = I²C™/SMBus input buffer

Note 1: Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.
2: Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

3.6.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 3-2) controls several aspects of the device clock's operation, both in full-power operation and in power-managed modes.

The System Clock Select bits, SCS<1:0>, select the clock source. The available clock sources are the primary clock (defined by the FOSC<2:0> Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator. The clock source changes after one or more of the bits are written to, following a brief clock transition interval.

The OSTS (OSCCON<3>) and T1RUN (T1CON<6>) bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer (OST) has timed out and the primary clock is providing the device clock in primary clock modes. The T1RUN bit indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these bits will be set at any time. If neither of these bits are set, the INTRC is providing the clock, or the internal oscillator has just started and is not yet stable.

The IDLEN bit determines if the device goes into Sleep mode or one of the Idle modes when the `SLEEP` instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 4.0 "Power-Managed Modes"**.

Note 1: The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source when executing a `SLEEP` instruction will be ignored.

2: It is recommended that the Timer1 oscillator be operating and stable before executing the `SLEEP` instruction or a very long delay may occur while the Timer1 oscillator starts.

3.6.1.1 System Clock Selection and the FOSC2 Configuration Bit

The SCS bits are cleared on all forms of Reset. In the device's default configuration, this means the primary oscillator defined by FOSC<1:0> (that is, one of the HC or EC modes) is used as the primary clock source on device Resets.

The default clock configuration on Reset can be changed with the FOSC2 Configuration bit. The effect of this bit is to set the clock source selected when SCS<1:0> = 00. When FOSC2 = 1 (default), the oscillator source defined by FOSC<1:0> is selected whenever SCS<1:0> = 00. When FOSC2 = 0, the INTRC oscillator is selected whenever SCS<1:2> = 00. Because the SCS bits are cleared on Reset, the FOSC2 setting also changes the default oscillator mode on Reset.

Regardless of the setting of FOSC2, INTRC will always be enabled on device power-up. It will serve as the clock source until the device has loaded its configuration values from memory. It is at this point that the FOSC Configuration bits are read and the oscillator selection of the operational mode is made.

Note that either the primary clock or the internal oscillator will have two bit setting options, at any given time, depending on the setting of FOSC2.

3.6.2 OSCILLATOR TRANSITIONS

PIC18F87J10 family devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 4.1.2 "Entering Power-Managed Modes"**.

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TABLE 6-4: REGISTER FILE SUMMARY (PIC18F87J10 FAMILY) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte								0000 0000	56, 243
BAUDCON1	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	56, 242
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte								0000 0000	56, 243
BAUDCON2	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	56, 242
ECCP1DEL	P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0	0000 0000	57, 188
TMR4	Timer4 Register								0000 0000	57, 168
PR4	Timer4 Period Register								1111 1111	57, 168
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	57, 167
CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx	57, 170
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx	57, 170
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000	57, 169
CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx	57, 170
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx	57, 170
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	--00 0000	57, 169
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte								0000 0000	57, 243
RCREG2	EUSART2 Receive Register								0000 0000	57, 251, 252
TXREG2	EUSART2 Transmit Register								0000 0000	57, 249, 250
TXSTA2	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	0000 0010	57, 240
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	57, 241
ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	0000 0000	57, 189
ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	0000 0000	57, 188
ECCP2AS	ECCP2ASE	ECCP2AS2	ECCP2AS1	ECCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	57, 189
ECCP2DEL	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	57, 188
SSP2BUF	MSSP2 Receive Buffer/Transmit Register								xxxx xxxx	57, 203, 238
SSP2ADD	MSSP2 Address Register (I ² C™ Slave mode), MSSP2 Baud Rate Reload Register (I ² C Master mode)								0000 0000	57, 203
SSP2STAT	SMP	CKE	D/Ā	P	S	R/Ā	UA	BF	0000 0000	57, 194, 204
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	57, 206, 205
SSP2CON2	GCEN	ACKSTAT	ACKDT/ADMSK5	ACKEN/ADMSK4	RCEN/ADMSK3	PEN/ADMSK2	RSEN/ADMSK1	SEN	0000 0000	57, 206

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

- Note**
- 1: Bit 21 of the PC is only available in Serial Programming modes.
 - 2: These bits and/or registers are only available in 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset values are shown for 80-pin devices.
 - 3: This register and its bits are not implemented in 64-pin devices. In 80-pin devices, the bits are unwritable and read as '0' in Microcontroller mode.
 - 4: The PLLEN bit is available only when either ECPLL or HSPLL Oscillator modes are selected; otherwise, the bit is read as '0'.
 - 5: Reset value is '0' when Two-Speed Start-up is enabled and '1' if disabled.

8.2 Address and Data Width

The PIC18F87J10 family of devices can be independently configured for different address and data widths on the same memory bus. Both address and data width are set by Configuration bits in the CONFIG3L register. As Configuration bits, this means that these options can only be configured by programming the device and are not controllable in software.

The BW bit selects an 8-bit or 16-bit data bus width. Setting this bit (default) selects a data width of 16 bits.

The EMB<1:0> bits determine both the program memory operating mode and the address bus width. The available options are 20-bit, 16-bit and 12-bit, as well as Microcontroller mode (external bus disabled). Selecting a 16-bit or 12-bit width makes a corresponding number of high-order lines available for I/O functions. These pins are no longer affected by the setting of the EBDIS bit. For example, selecting a 16-Bit Addressing mode (EMB<1:0> = 01) disables A<19:16> and allows PORTH<3:0> to function without interruptions from the bus. Using the smaller address widths allows users to tailor the memory bus to the size of the external memory space for a particular design while freeing up pins for dedicated I/O operation.

Because the EMB bits have the effect of disabling pins for memory bus operations, it is important to always select an address width at least equal to the data width. If a 12-bit address width is used with a 16-bit data width, the upper four bits of data will not be available on the bus.

All combinations of address and data widths require multiplexing of address and data information on the same lines. The address and data multiplexing, as well as I/O ports made available by the use of smaller address widths, are summarized in Table 8-2.

8.2.1 ADDRESS SHIFTING ON THE EXTERNAL BUS

By default, the address presented on the external bus is the value of the PC. In practical terms, this means that addresses in the external memory device below the top of on-chip memory are unavailable to the microcontroller. To access these physical locations, the glue logic between the microcontroller and the external memory must somehow translate addresses.

To simplify the interface, the external bus offers an extension of Extended Microcontroller mode that automatically performs address shifting. This feature is controlled by the EASHFT Configuration bit. Setting this bit offsets addresses on the bus by the size of the microcontroller's on-chip program memory and sets the bottom address at 0000h. This allows the device to use the entire range of physical addresses of the external memory.

8.2.2 21-BIT ADDRESSING

As an extension of 20-bit address width operation, the external memory bus can also fully address a 2-Mbyte memory space. This is done by using the Bus Address bit 0 (BA0) control line as the Least Significant bit of the address. The UB and LB control signals may also be used with certain memory devices to select the upper and lower bytes within a 16-bit wide data word.

This addressing mode is available in both 8-Bit and certain 16-Bit Data Width modes. Additional details are provided in **Section 8.6.3 "16-Bit Byte Select Mode"** and **Section 8.7 "8-Bit Mode"**.

TABLE 8-2: ADDRESS AND DATA LINES FOR DIFFERENT ADDRESS AND DATA WIDTHS

Data Width	Address Width	Multiplexed Data and Address Lines (and Corresponding Ports)	Address Only Lines (and Corresponding Ports)	Ports Available for I/O
8-Bit	12-Bit	AD<7:0> (PORTD<7:0>)	AD<11:8> (PORTE<3:0>)	PORTE<7:4>, All of PORTH
	16-Bit		AD<15:8> (PORTE<7:0>)	All of PORTH
	20-Bit		A<19:16>, AD<15:8> (PORTH<3:0>, PORTE<7:0>)	—
16-Bit	16-Bit	AD<15:0> (PORTD<7:0>, PORTE<7:0>)	—	All of PORTH
	20-Bit		A<19:16> (PORTH<3:0>)	—

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TABLE 11-9: PORTD FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RD0/AD0/PSP0	RD0	0	O	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	AD0 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 0 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 0 input. ⁽¹⁾
	PSP0		O	DIG	PSP read output data (LATD<0>); takes priority over port data.
			I	TTL	PSP write data input.
RD1/AD1/PSP1	RD1	0	O	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	AD1 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 1 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 1 input. ⁽¹⁾
	PSP1	x	O	DIG	PSP read output data (LATD<1>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD2/AD2/PSP2	RD2	0	O	DIG	LATD<2> data output.
		1	I	ST	PORTD<2> data input.
	AD2 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 2 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 2 input. ⁽¹⁾
	PSP2	x	O	DIG	PSP read output data (LATD<2>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD3/AD3/PSP3	RD3	0	O	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	AD3 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 3 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 3 input. ⁽¹⁾
	PSP3	x	O	DIG	PSP read output data (LATD<3>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD4/AD4/PSP4/SDO2	RD4	0	O	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	AD4 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 4 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 4 input. ⁽¹⁾
	PSP4	x	O	DIG	PSP read output data (LATD<4>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD5/AD5/PSP5/SDI2/SDA2	RD5	0	O	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input.
	AD5 ⁽²⁾	x	O	DIG	External memory interface, address/data bit 5 output. ⁽¹⁾
		x	I	TTL	External memory interface, data bit 5 input. ⁽¹⁾
	PSP5	x	O	DIG	PSP read output data (LATD<5>); takes priority over port data.
		x	I	TTL	PSP write data input.
	SDI2	1	I	ST	SPI data input (MSSP2 module).
	SDA2	1	O	DIG	I ² C™ data output (MSSP2 module); takes priority over port data.
		1	I	I ² C/SMB	I ² C data input (MSSP2 module); input type depends on module setting.

Legend: PWR = Power Supply, O = Output, I = Input, I²C™/SMB = I²C/SMBus input buffer, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: External memory interface I/O takes priority over all other digital and PSP I/O.

2: Available on 80-pin devices only.

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11.9 PORTH, LATH and TRISH Registers

Note: PORTH is available only on 80-pin devices.

PORTH is an 8-bit wide, bidirectional I/O port. The corresponding Data Direction register is TRISH. Setting a TRISH bit (= 1) will make the corresponding PORTH pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISH bit (= 0) will make the corresponding PORTH pin an output (i.e., put the contents of the output latch on the selected pin). PORTH<3:0> pins are digital only and tolerate voltages up to 5.5V.

The Output Latch register (LATH) is also memory mapped. Read-modify-write operations on the LATH register read and write the latched output value for PORTH.

All pins on PORTH are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

When the external memory interface is enabled, four of the PORTH pins function as the high-order address lines for the interface. The address output from the interface takes priority over other digital I/O. The corresponding TRISH bits are also overridden.

PORTH pins, RH4 through RH7, are multiplexed with analog converter inputs. The operation of these pins as analog inputs is selected by clearing or setting the PCFG<3:0> control bits in the ADCON1 register.

PORTH can also be configured as the alternate Enhanced PWM output Channels B and C for the ECCP1 and ECCP3 modules. This is done by clearing the ECCPMX Configuration bit.

EXAMPLE 11-8: INITIALIZING PORTH

```
CLRF    PORTH        ; Initialize PORTH by
                      ; clearing output
                      ; data latches
CLRF    LATH          ; Alternate method
                      ; to clear output
                      ; data latches
MOVLW   0Fh           ; Configure PORTH as
MOVWF   ADCON1        ; digital I/O
MOVLW   0CFh          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISH         ; Set RH3:RH0 as inputs
                      ; RH5:RH4 as outputs
                      ; RH7:RH6 as inputs
```


12.0 TIMER0 MODULE

The Timer0 module incorporates the following features:

- Software-selectable operation as a timer or counter in both 8-bit or 16-bit modes
- Readable and writable registers
- Dedicated 8-bit, software programmable prescaler
- Selectable clock source (internal or external)
- Edge select for external clock
- Interrupt-on-overflow

The T0CON register (Register 12-1) controls all aspects of the module's operation, including the prescale selection. It is both readable and writable.

A simplified block diagram of the Timer0 module in 8-bit mode is shown in Figure 12-1. Figure 12-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

REGISTER 12-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0
- bit 6 **T08BIT:** Timer0 8-Bit/16-Bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter
- bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)
- bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA:** Timer0 Prescaler Assignment bit
1 = Timer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.
- bit 2-0 **T0PS<2:0>:** Timer0 Prescaler Select bits
111 = 1:256 Prescale value
110 = 1:128 Prescale value
101 = 1:64 Prescale value
100 = 1:32 Prescale value
011 = 1:16 Prescale value
010 = 1:8 Prescale value
001 = 1:4 Prescale value
000 = 1:2 Prescale value

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18.1 ECCP Outputs and Configuration

Each of the Enhanced CCP modules may have up to four PWM outputs, depending on the selected operating mode. These outputs, designated PxA through PxD, are multiplexed with various I/O pins. Some ECCP pin assignments are constant, while others change based on device configuration. For those pins that do change, the controlling bits are:

- CCP2MX Configuration bit
- ECCPMX Configuration bit (80-pin devices only)
- Program Memory Operating mode, set by the EMB Configuration bits (80-pin devices only)

The pin assignments for the Enhanced CCP modules are summarized in Table 18-1, Table 18-2 and Table 18-3. To configure the I/O pins as PWM outputs, the proper PWM mode must be selected by setting the PxMx and CCPxMx bits (CCPxCON<7:6> and <3:0>, respectively). The appropriate TRIS direction bits for the corresponding port pins must also be set as outputs.

18.1.1 ECCP1/ECCP3 OUTPUTS AND PROGRAM MEMORY MODE

In 80-pin devices, the use of Extended Microcontroller mode has an indirect effect on the use of ECCP1 and ECCP3 in Enhanced PWM modes. By default, PWM outputs, P1B/P1C and P3B/P3C, are multiplexed to PORTE pins, along with the high-order byte of the external memory bus. When the bus is active in Extended Microcontroller mode, it overrides the Enhanced CCP outputs and makes them unavailable. Because of this, ECCP1 and ECCP3 can only be used in compatible (single-output) PWM modes when the device is in Extended Microcontroller mode and default pin configuration.

An exception to this configuration is when a 12-bit address width is selected for the external bus (EMB<1:0> Configuration bits = 01). In this case, the upper pins of PORTE continue to operate as digital I/O, even when the external bus is active. P1B/P1C and P3B/P3C remain available for use as Enhanced PWM outputs.

If an application requires the use of additional PWM outputs during Enhanced microcontroller operation, the P1B/P1C and P3B/P3C outputs can be reassigned to the upper bits of PORTH. This is done by clearing the ECCPMX Configuration bit.

18.1.2 ECCP2 OUTPUTS AND PROGRAM MEMORY MODES

For 80-pin devices, the program memory mode of the device (**Section 6.1.3 “PIC18F8XJ10/8XJ15 Program Memory Modes”**) also impacts pin multiplexing for the module.

The ECCP2 input/output (ECCP2/P2A) can be multiplexed to one of three pins. The default assignment (CCP2MX Configuration bit is set) for all devices is RC1. Clearing CCP2MX reassigns ECCP2/P2A to RE7.

An additional option exists for 80-pin devices. When these devices are operating in Microcontroller mode, the multiplexing options described above still apply. In Extended Microcontroller mode, clearing CCP2MX reassigns ECCP2/P2A to RB3.

18.1.3 USE OF CCP4 AND CCP5 WITH ECCP1 AND ECCP3

Only the ECCP2 module has four dedicated output pins that are available for use. Assuming that the I/O ports or other multiplexed functions on those pins are not needed, they may be used whenever needed without interfering with any other CCP module.

ECCP1 and ECCP3, on the other hand, only have three dedicated output pins: ECCPx/PxA, PxB and PxC. Whenever these modules are configured for Quad PWM mode, the pin normally used for CCP4 or CCP5 becomes the PxD output pins for ECCP3 and ECCP1, respectively. The CCP4 and CCP5 modules remain functional but their outputs are overridden.

18.1.4 ECCP MODULES AND TIMER RESOURCES

Like the standard CCP modules, the ECCP modules can utilize Timers 1, 2, 3 or 4, depending on the mode selected. Timer1 and Timer3 are available for modules in Capture or Compare modes, while Timer2 and Timer4 are available for modules in PWM mode. Additional details on timer resources are provided in **Section 17.1.1 “CCP Modules and Timer Resources”**.

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19.3.1 REGISTERS

Each MSSP module has four registers for SPI mode operation. These are:

- MSSP Control Register 1 (SSPxCON1)
- MSSP Status Register (SSPxSTAT)
- Serial Receive/Transmit Buffer Register (SSPxBUF)
- MSSP Shift Register (SSPxSR) – Not directly accessible

SSPxCON1 and SSPxSTAT are the control and status registers in SPI mode operation. The SSPxCON1 register is readable and writable. The lower 6 bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write.

SSPxSR is the shift register used for shifting data in or out. SSPxBUF is the buffer register to which data bytes are written to or read from.

In receive operations, SSPxSR and SSPxBUF together create a double-buffered receiver. When SSPxSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set.

During transmission, the SSPxBUF is not double-buffered. A write to SSPxBUF will write to both SSPxBUF and SSPxSR.

REGISTER 19-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE ⁽¹⁾	D/ \bar{A}	P	S	R/ \bar{W}	UA	BF
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

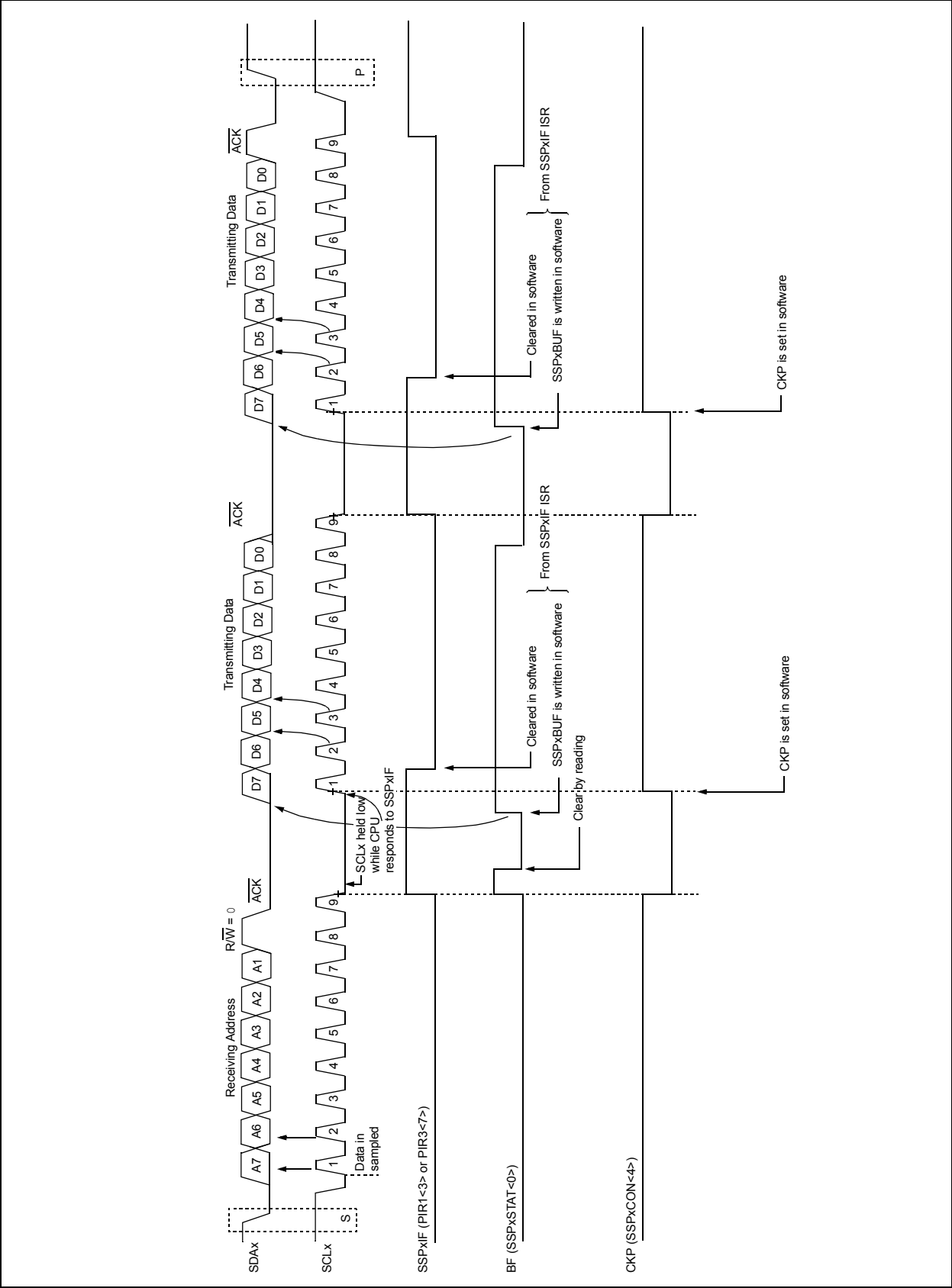
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 7 **SMP:** Sample bit
 SPI Master mode:
 1 = Input data sampled at end of data output time
 0 = Input data sampled at middle of data output time
 SPI Slave mode:
 SMP must be cleared when SPI is used in Slave mode.
- bit 6 **CKE:** SPI Clock Select bit⁽¹⁾
 1 = Transmit occurs on transition from active to Idle clock state
 0 = Transmit occurs on transition from Idle to active clock state
- bit 5 **D/ \bar{A} :** Data/Address bit
 Used in I²C mode only.
- bit 4 **P:** Stop bit
 Used in I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.
- bit 3 **S:** Start bit
 Used in I²C mode only.
- bit 2 **R/ \bar{W} :** Read/Write Information bit
 Used in I²C mode only.
- bit 1 **UA:** Update Address bit
 Used in I²C mode only.
- bit 0 **BF:** Buffer Full Status bit (Receive mode only)
 1 = Receive complete, SSPxBUF is full
 0 = Receive not complete, SSPxBUF is empty

Note 1: The polarity of the clock state is set by the CKP bit (SSPxCON1<4>).

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FIGURE 19-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESSING)



19.4.14 SLEEP OPERATION

While in Sleep mode, the I²C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

19.4.15 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

19.4.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit (SSPxSTAT<4>) is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the MSSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDAx line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

19.4.17 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDAx pin, arbitration takes place when the master outputs a '1' on SDAx, by letting SDAx float high and another master asserts a '0'. When the SCLx pin floats high, data should be stable. If the expected data on SDAx is a '1' and the data sampled on the SDAx pin = 0, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF, and reset the I²C port to its Idle state (Figure 19-27).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDAx and SCLx lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

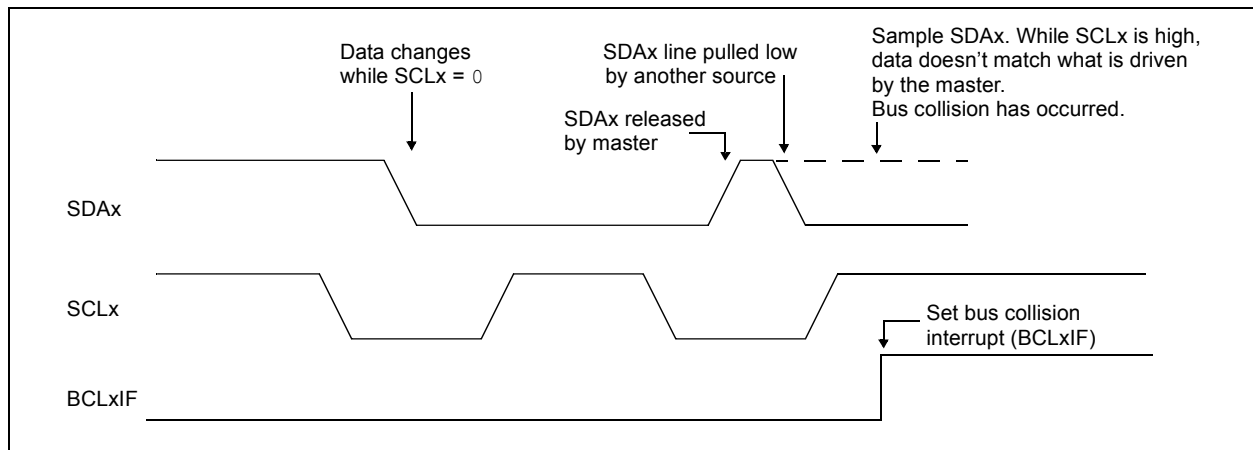
If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDAx and SCLx lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDAx and SCLx pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 19-27: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



20.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTAx<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTAx<4>). In addition, enable bit, SPEN (RCSTAx<7>), is set in order to configure the TXx and RXx pins to CKx (clock) and DTx (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CKx line. Clock polarity is selected with the SCKP bit (BAUDCONx<4>); setting SCKP sets the Idle state on CKx as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

20.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 20-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREGx (if available).

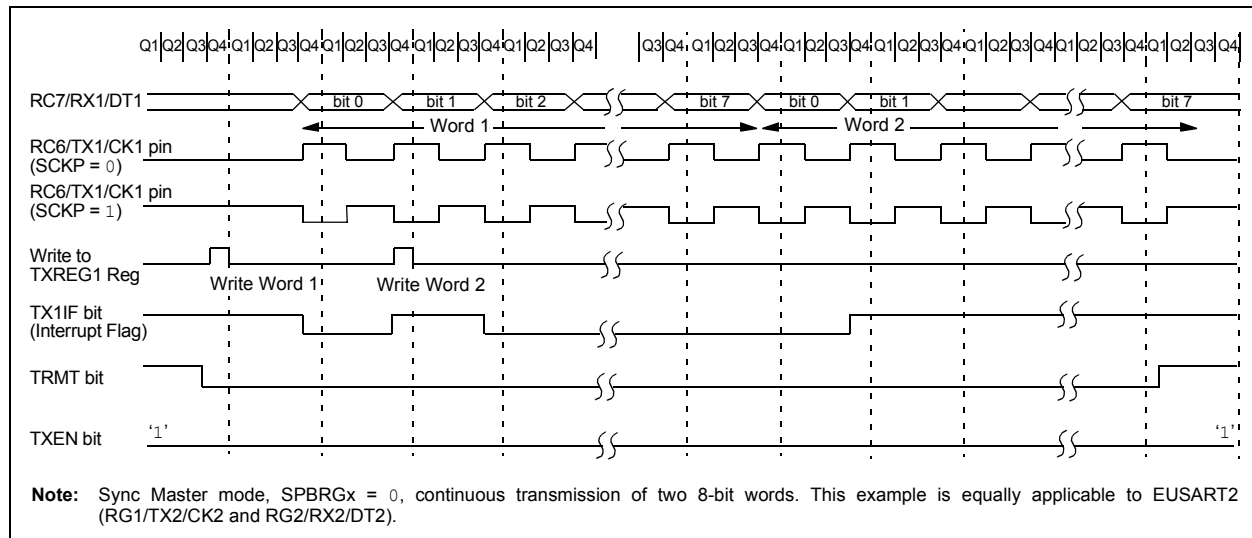
Once the TXREGx register transfers the data to the TSR register (occurs in one Tcy), the TXREGx is empty and the TXxIF flag bit is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXxIE. TXxIF is set regardless of the state of enable bit, TXxIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREGx register.

While flag bit, TXxIF, indicates the status of the TXREGx register, another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user must poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. If interrupts are desired, set enable bit, TXxIE.
4. If 9-bit transmission is desired, set bit, TX9.
5. Enable the transmission by setting bit, TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Start transmission by loading data to the TXREGx register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 20-11: SYNCHRONOUS TRANSMISSION



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TABLE 24-2: CONFIGURATION BITS AND DEVICE IDs

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value ⁽¹⁾
300000h CONFIG1L	DEBUG	XINST	STVREN	—	—	—	—	WDTEN	111- ---1
300001h CONFIG1H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽³⁾	CP0	—	—	---- 01--
300002h CONFIG2L	IESO	FCMEN	—	—	—	FOSC2	FOSC1	FOSC0	11-- -111
300003h CONFIG2H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300004h CONFIG3L	WAIT ⁽⁴⁾	BW ⁽⁴⁾	EMB1 ⁽⁴⁾	EMB0 ⁽⁴⁾	EASHFT ⁽⁴⁾	—	—	—	1111 1---
300005h CONFIG3H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	—	—	ECCPMX ⁽⁴⁾	CCP2MX	---- --11
3FFFFEh DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx ⁽⁵⁾
3FFFFFh DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 10x1 ⁽⁵⁾

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

3: This bit should always be maintained as '0'.

4: Implemented in 80-pin devices only. On 64-pin devices, these bits are reserved and should always be maintained as '1'.

5: See Register 24-7 and Register 24-8 for DEVID values. These registers are read-only and cannot be programmed by the user.

25.2 Extended Instruction Set

In addition to the standard 75 instructions of the PIC18 instruction set, the PIC18F87J10 family of devices also provide an optional extension to the core CPU functionality. The added features include eight additional instructions that augment Indirect and Indexed Addressing operations and the implementation of Indexed Literal Offset Addressing for many of the standard PIC18 instructions.

The additional features of the extended instruction set are disabled by default on unprogrammed devices. Users must properly set or clear the XINST Configuration bit during programming to enable or disable these features.

The instructions in the extended set can all be classified as literal operations, which either manipulate the File Select Registers, or use them for Indexed Addressing. Two of the instructions, `ADDFSR` and `SUBFSR`, each have an additional special instantiation for using FSR2. These versions (`ADDULNK` and `SUBULNK`) allow for automatic return after execution.

The extended instructions are specifically implemented to optimize re-entrant program code (that is, code that is recursive or that uses a software stack) written in high-level languages, particularly C. Among other things, they allow users working in high-level languages to perform certain operations on data structures more efficiently. These include:

- dynamic allocation and deallocation of software stack space when entering and leaving subroutines
- function pointer invocation
- software Stack Pointer manipulation
- manipulation of variables located in a software stack

A summary of the instructions in the extended instruction set is provided in Table 25-3. Detailed descriptions are provided in **Section 25.2.2 “Extended Instruction Set”**. The opcode field descriptions in Table 25-1 (page 294) apply to both the standard and extended PIC18 instruction sets.

Note: The instruction set extension and the Indexed Literal Offset Addressing mode were designed for optimizing applications written in C; the user may likely never use these instructions directly in assembler. The syntax for these commands is provided as a reference for users who may be reviewing code that has been generated by a compiler.

25.2.1 EXTENDED INSTRUCTION SYNTAX

Most of the extended instructions use indexed arguments, using one of the File Select Registers and some offset to specify a source or destination register. When an argument for an instruction serves as part of Indexed Addressing, it is enclosed in square brackets (“[]”). This is done to indicate that the argument is used as an index or offset. The MPASM™ Assembler will flag an error if it determines that an index or offset value is not bracketed.

When the extended instruction set is enabled, brackets are also used to indicate index arguments in byte-oriented and bit-oriented instructions. This is in addition to other changes in their syntax. For more details, see **Section 25.2.3.1 “Extended Instruction Syntax with Standard PIC18 Commands”**.

Note: In the past, square brackets have been used to denote optional arguments in the PIC18 and earlier instruction sets. In this text and going forward, optional arguments are denoted by braces (“{ }”).

TABLE 25-3: EXTENSIONS TO THE PIC18 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected
			MSb		LSb		
ADDFSR f, k	Add Literal to FSR	1	1110	1000	ffkk	kkkk	None
ADDULNK k	Add Literal to FSR2 and Return	2	1110	1000	11kk	kkkk	None
CALLW	Call Subroutine using WREG	2	0000	0000	0001	0100	None
MOVSF z _s , f _d	Move z _s (source) to 1st word f _d (destination) 2nd word	2	1110	1011	0zzz	zzzz	None
MOVSS z _s , z _d	Move z _s (source) to 1st word z _d (destination) 2nd word	2	1110	1011	1zzz	zzzz	None
PUSHL k	Store Literal at FSR2, Decrement FSR2	1	1110	1010	kkkk	kkkk	None
SUBFSR f, k	Subtract Literal from FSR	1	1110	1001	ffkk	kkkk	None
SUBULNK k	Subtract Literal from FSR2 and Return	2	1110	1001	11kk	kkkk	None

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27.2 DC Characteristics: Power-Down and Supply Current PIC18F87J10 Family (Industrial) (Continued)

PIC18F87J10 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ^(2,3)						
	All devices	1.8	3.27	mA	-40°C	VDD = 2.0V ⁽⁵⁾	FOSC = 1 MHz (PRI_IDLE mode, EC oscillator)
		1.8	3.27	mA	+25°C		
		1.9	3.27	mA	+85°C		
	All devices	4.0	5.57	mA	-40°C	VDD = 2.5V ⁽⁵⁾	
		3.7	5.57	mA	+25°C		
		3.5	5.57	mA	+85°C		
	All devices	4.2	5.97	mA	-40°C	VDD = 3.3V ⁽⁶⁾	
		4.0	5.97	mA	+25°C		
		3.8	5.97	mA	+85°C		
	All devices	2.4	4.47	mA	-40°C	VDD = 2.0V ⁽⁵⁾	FOSC = 4 MHz (PRI_IDLE mode, EC oscillator)
		2.4	4.47	mA	+25°C		
		2.5	4.47	mA	+85°C		
	All devices	4.7	6.97	mA	-40°C	VDD = 2.5V ⁽⁵⁾	
		4.4	6.97	mA	+25°C		
		4.8	6.97	mA	+85°C		
	All devices	5.1	7.47	mA	-40°C	VDD = 3.3V ⁽⁶⁾	
		4.9	7.47	mA	+25°C		
		4.8	7.47	mA	+85°C		
	All devices	13.4	18.7	mA	-40°C	VDD = 2.5V ⁽⁵⁾	FOSC = 40 MHz (PRI_IDLE mode, EC oscillator)
		13.0	18.7	mA	+25°C		
		13.0	18.7	mA	+85°C		
	All devices	14.8	19.7	mA	-40°C	VDD = 3.3V ⁽⁶⁾	
		14.4	19.7	mA	+25°C		
14.5		19.7	mA	+85°C			

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} , and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 $OSC1$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
 $MCLR$ = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in k Ω .
- 4:** Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.
- 5:** ENVREG tied to V_{SS} , voltage regulator disabled.
- 6:** ENVREG tied to V_{DD} , voltage regulator enabled.

PIC18F87J10 FAMILY

27.2 DC Characteristics: Power-Down and Supply Current PIC18F87J10 Family (Industrial) (Continued)

PIC18F87J10 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ^(2,3)						
	All devices	1.8	3.27	mA	-10°C	VDD = 2.0V ⁽⁵⁾	FOSC = 32 kHz ⁽⁴⁾ (SEC_RUN mode, Timer1 as clock)
		1.8	3.27	mA	+25°C		
		1.9	3.27	mA	+70°C		
	All devices	4.0	5.57	mA	-10°C	VDD = 2.5V ⁽⁵⁾	
		3.7	5.57	mA	+25°C		
		3.5	5.57	mA	+70°C		
	All devices	4.2	5.97	mA	-10°C	VDD = 3.3V ⁽⁶⁾	
		4.0	5.97	mA	+25°C		
		3.8	5.97	mA	+70°C		
	All devices	1.8	3.27	mA	-10°C	VDD = 2.0V ⁽⁵⁾	FOSC = 32 kHz ⁽⁴⁾ (SEC_IDLE mode, Timer1 as clock)
		1.8	3.27	mA	+25°C		
		1.9	3.27	mA	+70°C		
	All devices	4.0	5.57	mA	-10°C	VDD = 2.5V ⁽⁵⁾	
		3.7	5.57	mA	+25°C		
		3.5	5.57	mA	+70°C		
	All devices	4.2	5.97	mA	-10°C	VDD = 3.3V ⁽⁶⁾	
		4.0	5.97	mA	+25°C		
		3.8	5.97	mA	+70°C		

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} , and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 $\text{OSC1} = \text{external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to } V_{DD}$;
 $\text{MCLR} = V_{DD}$; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2\text{REXT}$ (mA) with REXT in $\text{k}\Omega$.
- 4:** Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.
- 5:** ENVREG tied to V_{SS} , voltage regulator disabled.
- 6:** ENVREG tied to V_{DD} , voltage regulator enabled.

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FIGURE 27-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

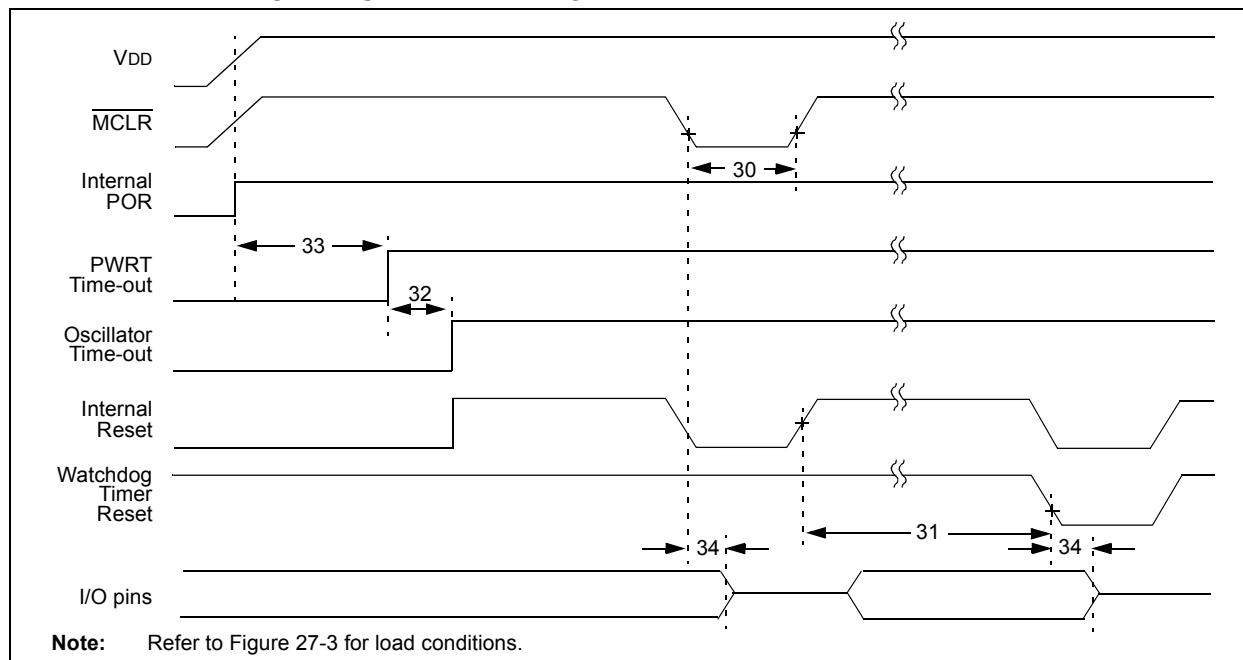


TABLE 27-12: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	μs	
31	TWD	Watchdog Timer Time-out Period (no postscaler)	3.5	4.1	4.9	ms	
32	TOST	Oscillation Start-up Timer Period	1024 TOSC	—	1024 TOSC	—	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	57.4	66	77.7	ms	
34	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μs	
38	TCSD	CPU Start-up Time	—	200	—	μs	

APPENDIX B: REVISION HISTORY

Revision A (December 2004)

Original data sheet for PIC18F87J10 family devices.

Revision B (July 2005)

Packaging diagrams have been updated. Document updated from Advanced to Preliminary. Updated all TBDs in **Section 27.0 “Electrical Characteristics”**. Edits to text throughout document.

Revision C (December 2005)

Packaging diagrams have been updated. Minor edits to text throughout document.

Revision D (June 2006)

Electrical characteristics and packaging diagrams have been updated. Minor edits to text throughout document.

Revision E (June 2009)

Pin diagrams have been edited to indicate 5.5V tolerant input pins. Packaging diagrams have been updated. **Section 2.0 “Guidelines for Getting Started with PIC18FJ Microcontrollers”** has been added. Minor text edits throughout the document.

Revision F (September 2009)

Added **Appendix B: “Revision History”**.