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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f87j10-i-pt

PIC18F87J10 FAMILY

TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF1/AN6/C2OUT	17	I/O	ST	PORTF is a bidirectional I/O port. Digital I/O. Analog input 6. Comparator 2 output.
RF1		I	Analog	
AN6		O	—	
C2OUT	16	O	—	Digital I/O. Analog input 7. Comparator 1 output.
RF2/AN7/C1OUT		I/O	ST	
RF2		I	Analog	
AN7	15	O	—	Digital I/O. Analog input 8.
C1OUT		I/O	ST	
RF3/AN8		I	Analog	
RF3	14	I/O	ST	Digital I/O. Analog input 9.
AN8		I	Analog	
RF4/AN9		I/O	ST	
RF4	13	I	Analog	Digital I/O. Analog input 10. Comparator reference voltage output.
AN9		O	—	
RF5/AN10/CVREF		I/O	ST	
RF5	12	I	Analog	Digital I/O. Analog input 11.
AN10		O	—	
CVREF		I/O	ST	
RF6/AN11	11	I	Analog	Digital I/O. SPI slave select input.
RF6		I/O	ST	
AN11		I	TTL	
RF7/SS1	11	I/O	ST	Digital I/O. SPI slave select input.
RF7		I	TTL	
SS1		I	TTL	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C/SMB = I²C™/SMBus input buffer

Note 1: Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

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TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/AD0/PSP0	72			PORTD is a bidirectional I/O port.
RD0		I/O	ST	Digital I/O.
AD0		I/O	TTL	External memory address/data 0.
PSP0		I/O	TTL	Parallel Slave Port data.
RD1/AD1/PSP1	69			
RD1		I/O	ST	Digital I/O.
AD1		I/O	TTL	External memory address/data 1.
PSP1		I/O	TTL	Parallel Slave Port data.
RD2/AD2/PSP2	68			
RD2		I/O	ST	Digital I/O.
AD2		I/O	TTL	External memory address/data 2.
PSP2		I/O	TTL	Parallel Slave Port data.
RD3/AD3/PSP3	67			
RD3		I/O	ST	Digital I/O.
AD3		I/O	TTL	External memory address/data 3.
PSP3		I/O	TTL	Parallel Slave Port data.
RD4/AD4/PSP4/SDO2	66			
RD4		I/O	ST	Digital I/O.
AD4		I/O	TTL	External memory address/data 4.
PSP4		I/O	TTL	Parallel Slave Port data.
SDO2		O	—	SPI data out.
RD5/AD5/PSP5/SDI2/SDA2	65			
RD5		I/O	ST	Digital I/O.
AD5		I/O	TTL	External memory address/data 5.
PSP5		I/O	TTL	Parallel Slave Port data.
SDI2		I	ST	SPI data in.
SDA2		I/O	I ² C/SMB	I ² C™ data I/O.
RD6/AD6/PSP6/SCK2/SCL2	64			
RD6		I/O	ST	Digital I/O.
AD6		I/O	TTL	External memory address/data 6.
PSP6		I/O	TTL	Parallel Slave Port data.
SCK2		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL2		I/O	I ² C/SMB	Synchronous serial clock input/output for I ² C mode.
RD7/AD7/PSP7/SS2	63			
RD7		I/O	ST	Digital I/O.
AD7		I/O	TTL	External memory address/data 7.
PSP7		I/O	TTL	Parallel Slave Port data.
SS2		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C/SMB = I²C™/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).
Note 2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).
Note 3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).
Note 4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).
Note 5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

PIC18F87J10 FAMILY

TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/ECCP3/P3A	5			PORTG is a bidirectional I/O port.
RG0		I/O	ST	Digital I/O.
ECCP3		I/O	ST	Capture 3 input/Compare 3 output/PWM 3 output.
P3A		O	—	ECCP3 PWM output A.
RG1/TX2/CK2	6			
RG1		I/O	ST	Digital I/O.
TX2		O	—	EUSART2 asynchronous transmit.
CK2		I/O	ST	EUSART2 synchronous clock (see related RX2/DT2).
RG2/RX2/DT2	7			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	EUSART2 asynchronous receive.
DT2		I/O	ST	EUSART2 synchronous data (see related TX2/CK2).
RG3/CCP4/P3D	8			
RG3		I/O	ST	Digital I/O.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM 4 output.
P3D		O	—	ECCP3 PWM output D.
RG4/CCP5/P1D	10			
RG4		I/O	ST	Digital I/O.
CCP5		I/O	ST	Capture 5 input/Compare 5 output/PWM 5 output.
P1D		O	—	ECCP1 PWM output D.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C/SMB = I²C™/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).
2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).
3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).
4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).
5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

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3.5 Internal Oscillator Block

The PIC18F87J10 family of devices includes an internal oscillator source (INTRC) which provides a nominal 31 kHz output. The INTRC is enabled on device power-up and clocks the device during its configuration cycle until it enters operating mode. INTRC is also enabled if it is selected as the device clock source or if any of the following are enabled:

- Fail-Safe Clock Monitor
- Watchdog Timer
- Two-Speed Start-up

These features are discussed in greater detail in **Section 24.0 “Special Features of the CPU”**.

The INTRC can also be optionally configured as the default clock source on device start-up by setting the FOSC2 Configuration bit. This is discussed in **Section 3.6.1 “Oscillator Control Register”**.

3.6 Clock Sources and Oscillator Switching

The PIC18F87J10 family includes a feature that allows the device clock source to be switched from the main oscillator to an alternate clock source. PIC18F87J10 family devices offer two alternate clock sources. When an alternate clock source is enabled, the various power-managed operating modes are available.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- Secondary oscillators
- Internal oscillator

The **primary oscillators** include the External Crystal and Resonator modes and the External Clock modes. The particular mode is defined by the FOSC<2:0> Configuration bits. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC18F87J10 family devices offer the Timer1 oscillator as a secondary oscillator. This oscillator, in all power-managed modes, is often the time base for functions such as a real-time clock.

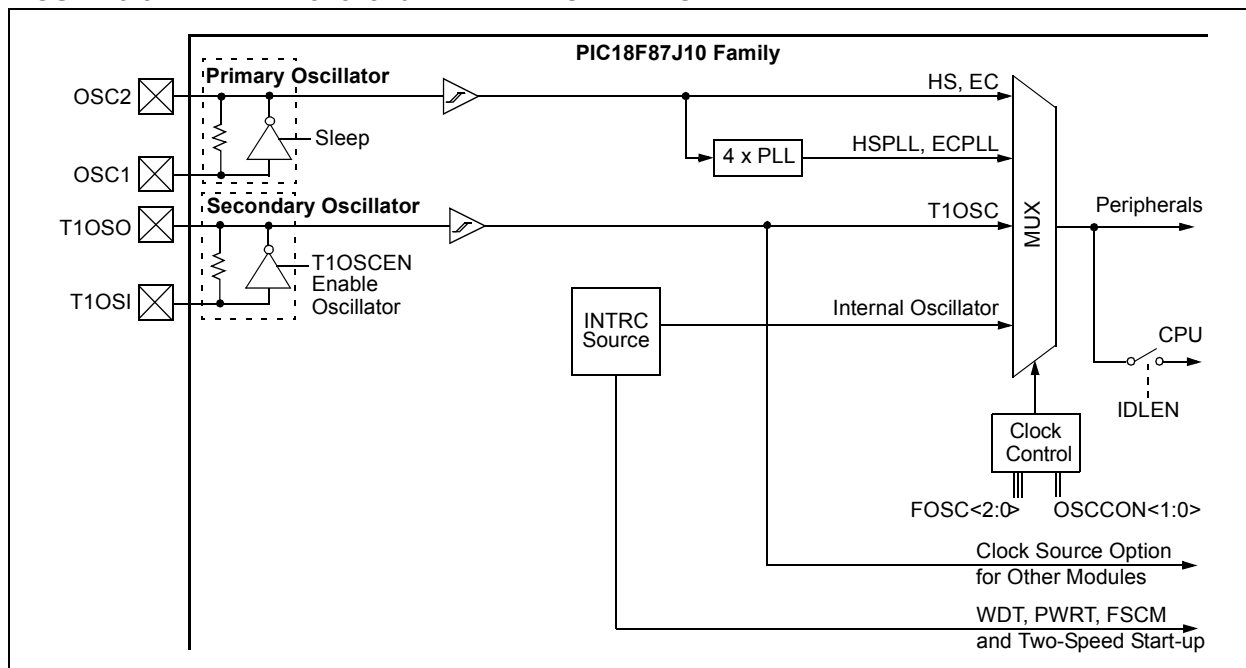
Most often, a 32.768 kHz watch crystal is connected between the RC0/T1OSO/T13CKI and RC1/T1OSI pins. Loading capacitors are also connected from each pin to ground.

The Timer1 oscillator is discussed in greater detail in **Section 13.3 “Timer1 Oscillator”**.

In addition to being a primary clock source, the **internal oscillator** is available as a power-managed mode clock source. The INTRC source is also used as the clock source for several special features, such as the WDT and Fail-Safe Clock Monitor.

The clock sources for the PIC18F87J10 family devices are shown in Figure 3-5. See **Section 24.0 “Special Features of the CPU”** for Configuration register details.

FIGURE 3-5: PIC18F87J10 FAMILY CLOCK DIAGRAM



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TABLE 6-4: REGISTER FILE SUMMARY (PIC18F87J10 FAMILY) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte								0000 0000	56, 243
BAUDCON1	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	56, 242
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte								0000 0000	56, 243
BAUDCON2	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	56, 242
ECCP1DEL	P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0	0000 0000	57, 188
TMR4	Timer4 Register								0000 0000	57, 168
PR4	Timer4 Period Register								1111 1111	57, 168
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	57, 167
CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx	57, 170
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx	57, 170
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000	57, 169
CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx	57, 170
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx	57, 170
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	--00 0000	57, 169
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte								0000 0000	57, 243
RCREG2	EUSART2 Receive Register								0000 0000	57, 251, 252
TXREG2	EUSART2 Transmit Register								0000 0000	57, 249, 250
TXSTA2	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	0000 0010	57, 240
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	57, 241
ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	0000 0000	57, 189
ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	0000 0000	57, 188
ECCP2AS	ECCP2ASE	ECCP2AS2	ECCP2AS1	ECCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	57, 189
ECCP2DEL	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	57, 188
SSP2BUF	MSSP2 Receive Buffer/Transmit Register								xxxx xxxx	57, 203, 238
SSP2ADD	MSSP2 Address Register (I ² C™ Slave mode), MSSP2 Baud Rate Reload Register (I ² C Master mode)								0000 0000	57, 203
SSP2STAT	SMP	CKE	D/Ā	P	S	R/Ā	UA	BF	0000 0000	57, 194, 204
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	57, 206, 205
SSP2CON2	GCEN	ACKSTAT	ACKDT/ADMSK5	ACKEN/ADMSK4	RCEN/ADMSK3	PEN/ADMSK2	RSEN/ADMSK1	SEN	0000 0000	57, 206

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

- Note**
- 1: Bit 21 of the PC is only available in Serial Programming modes.
 - 2: These bits and/or registers are only available in 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset values are shown for 80-pin devices.
 - 3: This register and its bits are not implemented in 64-pin devices. In 80-pin devices, the bits are unwritable and read as '0' in Microcontroller mode.
 - 4: The PLLEN bit is available only when either ECPLL or HSPLL Oscillator modes are selected; otherwise, the bit is read as '0'.
 - 5: Reset value is '0' when Two-Speed Start-up is enabled and '1' if disabled.

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6.4.3.2 FSR Registers and POSTINC, POSTDEC, PREINC and PLUSW

In addition to the INDF operand, each FSR register pair also has four additional indirect operands. Like INDF, these are “virtual” registers that cannot be indirectly read or written to. Accessing these registers actually accesses the associated FSR register pair, but also performs a specific action on its stored value. They are:

- POSTDEC: accesses the FSR value, then automatically decrements it by ‘1’ afterwards
- POSTINC: accesses the FSR value, then automatically increments it by ‘1’ afterwards
- PREINC: increments the FSR value by ‘1’, then uses it in the operation
- PLUSW: adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the new value in the operation

In this context, accessing an INDF register uses the value in the FSR registers without changing them. Similarly, accessing a PLUSW register gives the FSR value offset by the value in the W register; neither value is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR registers.

Operations on the FSRs with POSTDEC, POSTINC and PREINC affect the entire register pair; that is, roll-overs of the FSRnL register from FFh to 00h carry over to the FSRnH register. On the other hand, results of these operations do not change the value of any flags in the STATUS register (e.g., Z, N, OV, etc.).

The PLUSW register can be used to implement a form of Indexed Addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

6.4.3.3 Operations by FSRs on FSRs

Indirect Addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a specific case, assume that FSR0H:FSR0L contains FE7h, the address of INDF1. Attempts to read the value of the INDF1, using INDF0 as an operand, will return 00h. Attempts to write to INDF1, using INDF0 as the operand, will result in a NOP.

On the other hand, using the virtual registers to write to an FSR pair may not occur as planned. In these cases, the value will be written to the FSR pair but without any incrementing or decrementing. Thus, writing to INDF2 or POSTDEC2 will write the same value to the FSR2H:FSR2L.

Since the FSRs are physical registers mapped in the SFR space, they can be manipulated through all direct operations. Users should proceed cautiously when working on these registers, particularly if their code uses Indirect Addressing.

Similarly, operations by Indirect Addressing are generally permitted on all other SFRs. Users should exercise the appropriate caution that they do not inadvertently change settings that might affect the operation of the device.

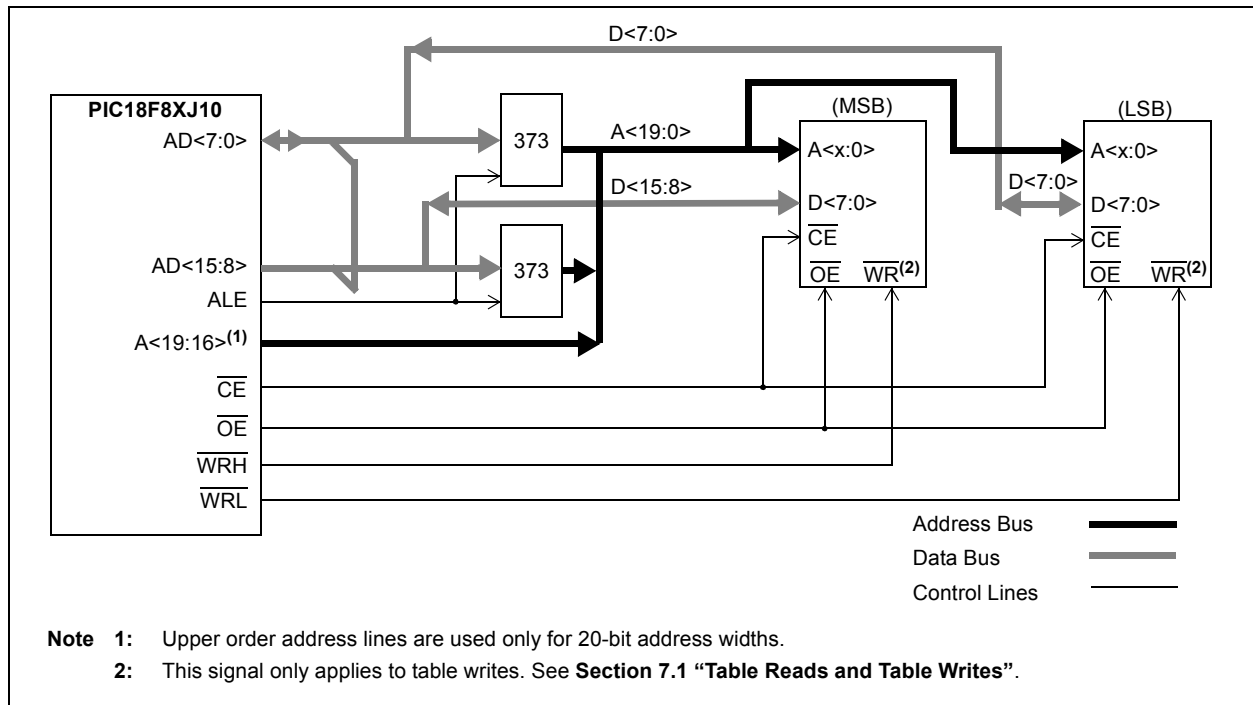
PIC18F87J10 FAMILY

8.6.1 16-BIT BYTE WRITE MODE

Figure 8-1 shows an example of 16-Bit Byte Write mode for PIC18F87J10 family devices. This mode is used for two separate 8-bit memories connected for 16-bit operation. This generally includes basic EPROM and Flash devices. It allows table writes to byte-wide external memories.

During a `TBLWT` instruction cycle, the `TABLAT` data is presented on the upper and lower bytes of the `AD<15:0>` bus. The appropriate `WRH` or `WRL` control line is strobed on the LSb of the `TBLPTR`.

FIGURE 8-1: 16-BIT BYTE WRITE MODE EXAMPLE



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FIGURE 19-8: I²C™ SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 7-BIT ADDRESSING)

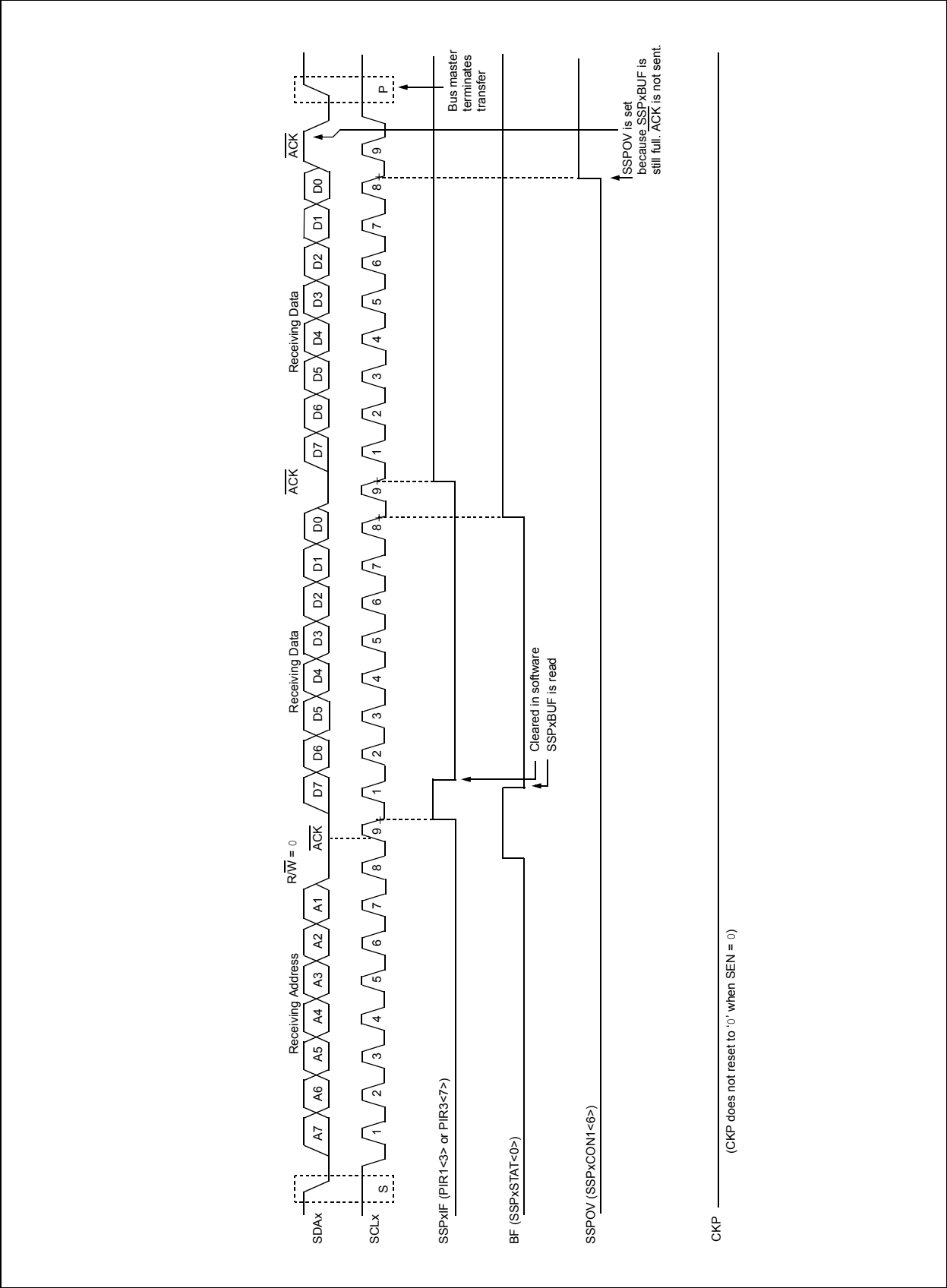


FIGURE 19-13: I²C™ SLAVE MODE TIMING (TRANSMISSION, 10-BIT ADDRESSING)

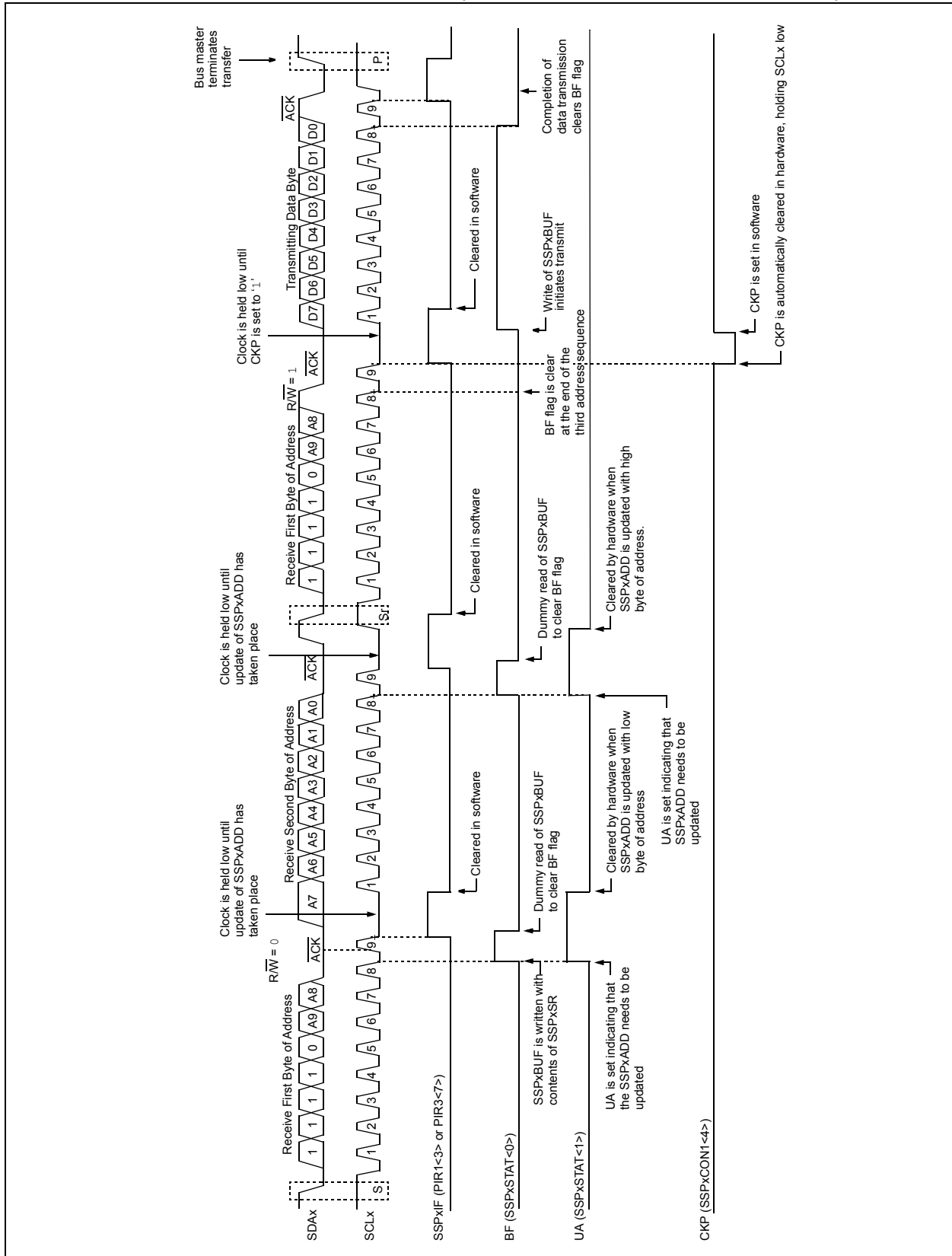
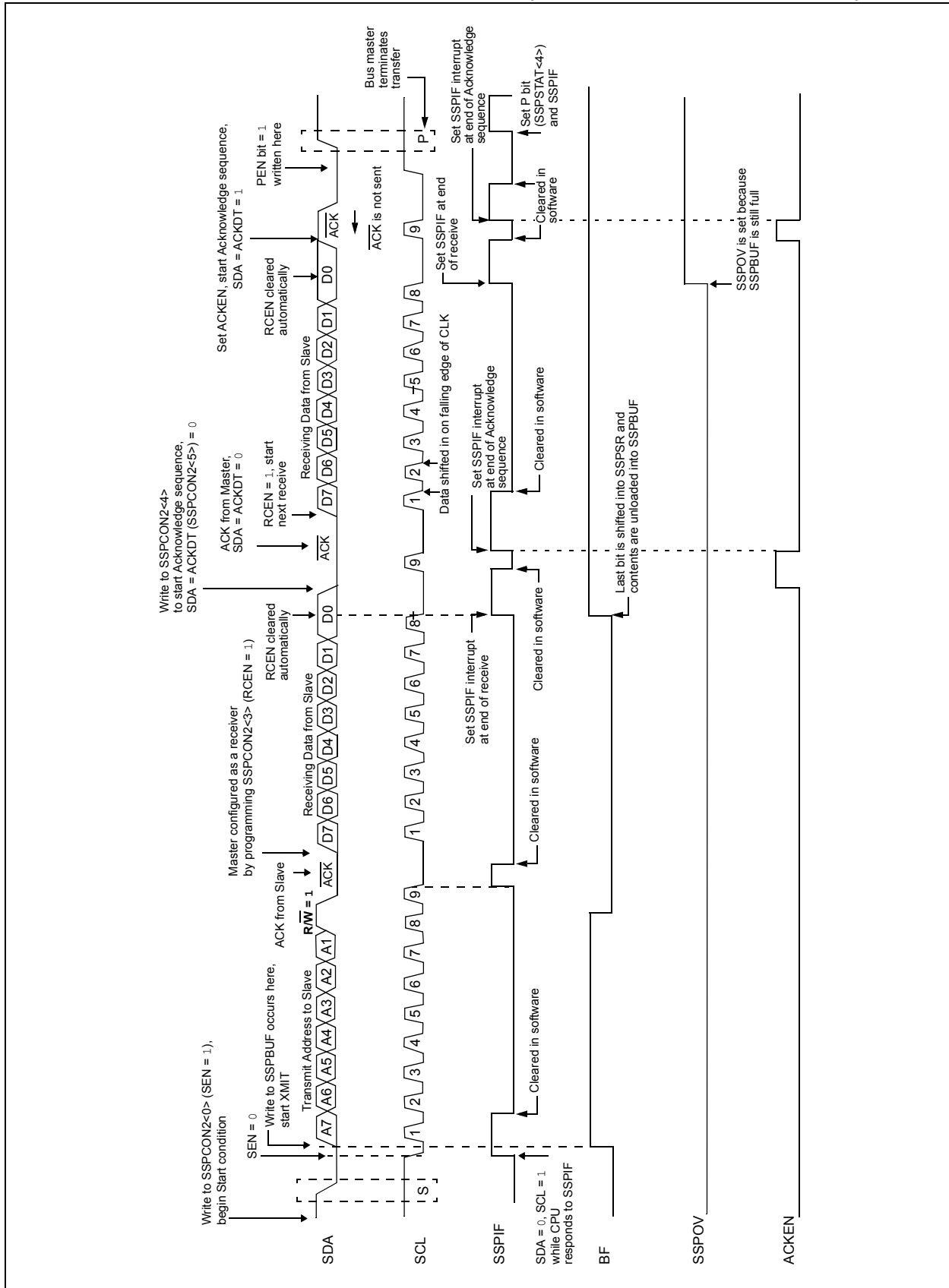


FIGURE 19-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESSING)



PIC18F87J10 FAMILY

19.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

- A low level is sampled on SDAx when SCLx goes from low level to high level.
- SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD<6:0> and counts down to 0. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 19-31). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 19-32).

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 19-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

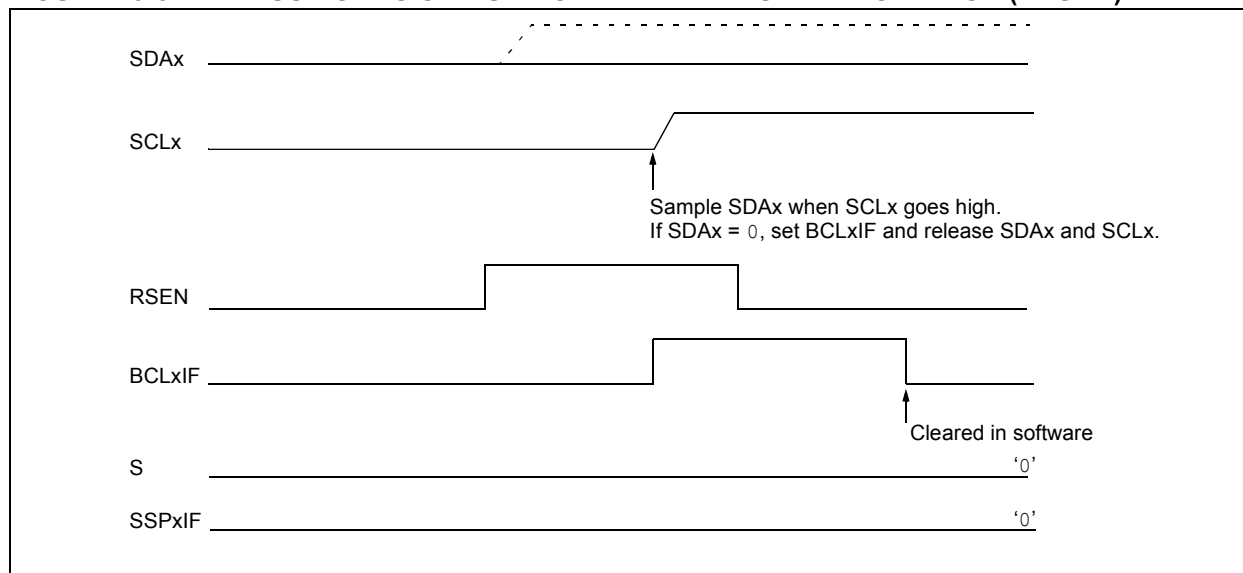


FIGURE 19-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

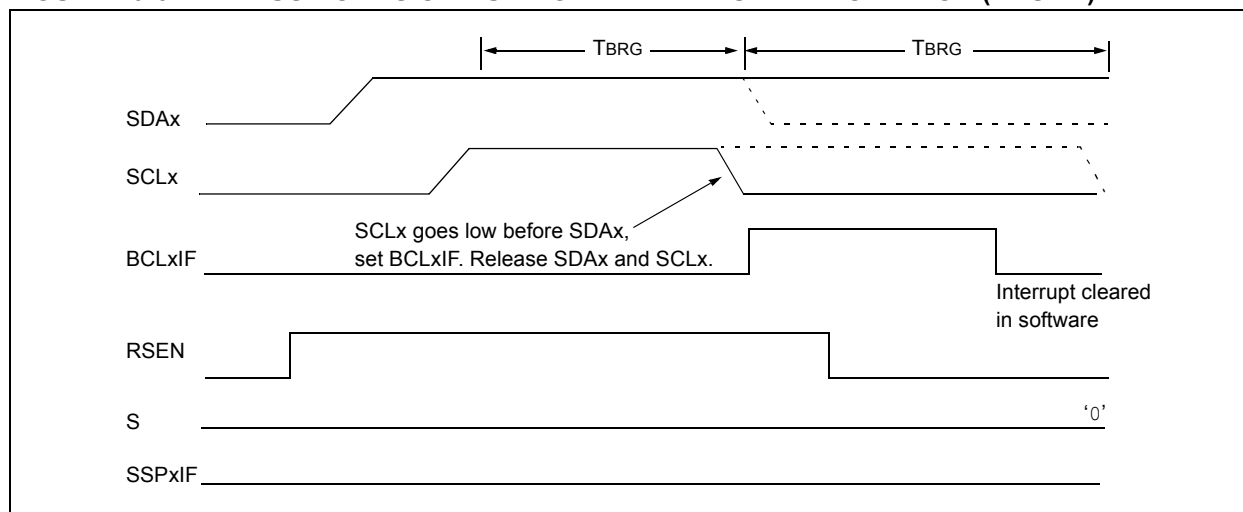
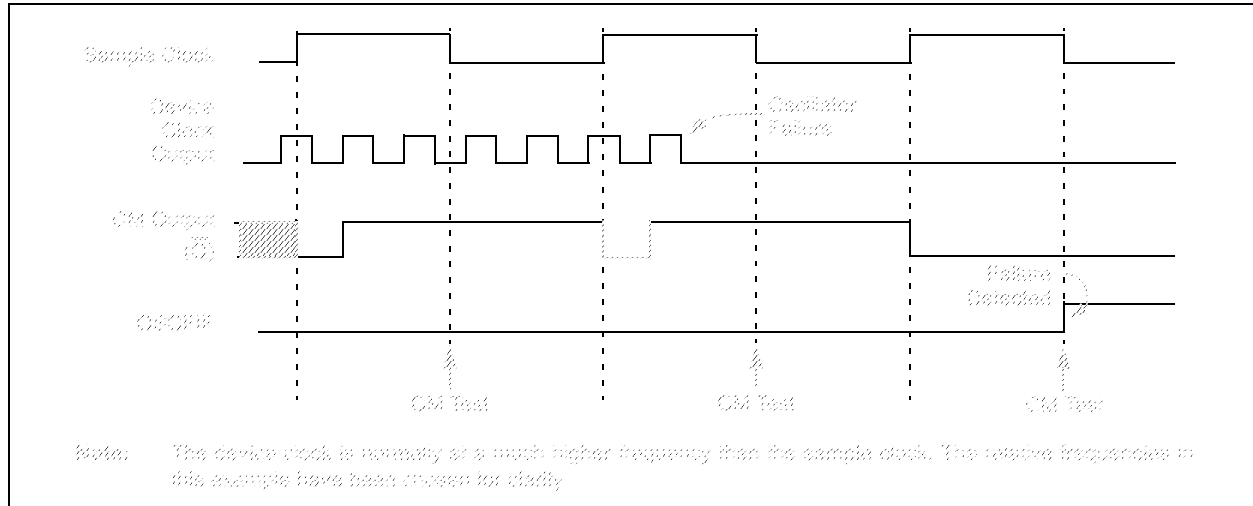


FIGURE 24-5: FSCM TIMING DIAGRAM



24.5.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexor selects the clock source selected by the OSCCON register. Fail-Safe Monitoring of the power-managed clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTRC multiplexor. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTRC source.

24.5.4 POR OR WAKE-UP FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is either EC or INTRC modes, monitoring can begin immediately following these events.

For HS or HSPLL modes, the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 24.4.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new power-managed mode is selected, the primary clock is disabled.

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TABLE 25-2: PIC18F87J10 FAMILY INSTRUCTION SET (CONTINUED)

Mnemonic, Operands	Description	Cycles	16-bit Instruction Word				Status Affected	Notes
			MSb		LSb			
LITERAL OPERATIONS								
ADDLW k	Add Literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW k	AND Literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW k	Inclusive OR Literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR f, k	Move Literal (12-bit) 2nd word to FSR(f) 1st word	2	1110	1110	00ff	kkkk	None	
			1111	0000	kkkk	kkkk		
MOVLB k	Move Literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW k	Move Literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW k	Multiply Literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW k	Subtract WREG from Literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW k	Exclusive OR Literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS								
TBLRD*	Table Read	2	0000	0000	0000	1000	None	
TBLRD*+	Table Read with Post-Increment	2	0000	0000	0000	1001	None	
TBLRD*-	Table Read with Post-Decrement		0000	0000	0000	1010	None	
TBLRD*+	Table Read with Pre-Increment		0000	0000	0000	1011	None	
TBLWT*	Table Write		0000	0000	0000	1100	None	
TBLWT*+	Table Write with Post-Increment		0000	0000	0000	1101	None	
TBLWT*-	Table Write with Post-Decrement		0000	0000	0000	1110	None	
TBLWT*+	Table Write with Pre-Increment	0000	0000	0000	1111	None		

- Note 1:** When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and, where applicable, $d = 1$), the prescaler will be cleared if assigned.
- 3:** If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
- 4:** Some instructions are two-word instructions. The second word of these instructions will be executed as a `NOP` unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

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25.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set for the PIC18F87J10 family. This includes the MPLAB C18 C Compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option or dialog box within the environment that allows the user to configure the language tool and its settings for the project
- A command line option
- A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

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FIGURE 27-8: PROGRAM MEMORY READ TIMING DIAGRAM

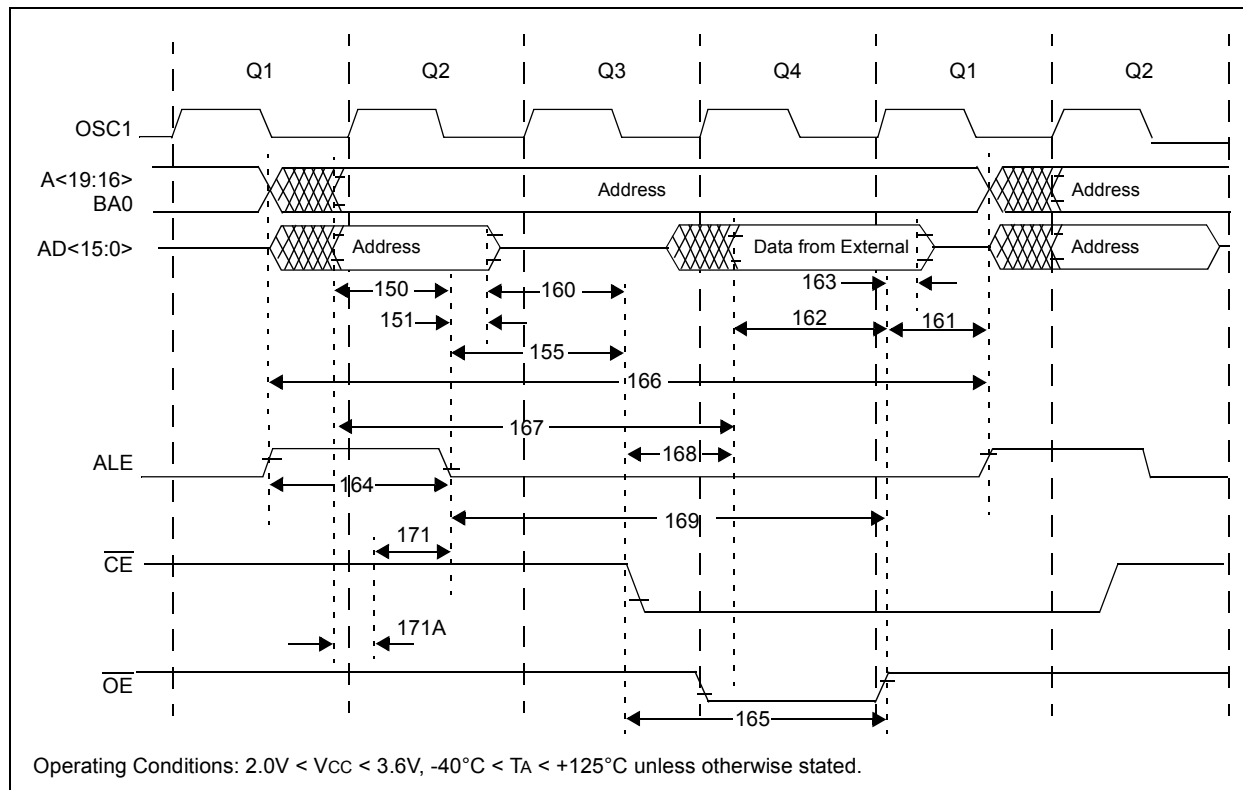


TABLE 27-10: CLK0 AND I/O TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2alL	Address Out Valid to ALE ↓ (address setup time)	$0.25 T_{CY} - 10$	—	—	ns
151	TalL2adI	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
155	TalL2oeL	ALE ↓ to \overline{OE} ↓	10	$0.125 T_{CY}$	—	ns
160	TadZ2oeL	AD High-Z to \overline{OE} ↓ (bus release to \overline{OE})	0	—	—	ns
161	ToeH2adD	\overline{OE} ↑ to AD Driven	$0.125 T_{CY} - 5$	—	—	ns
162	TadV2oeH	LS Data Valid before \overline{OE} ↑ (data setup time)	20	—	—	ns
163	ToeH2adI	\overline{OE} ↑ to Data In Invalid (data hold time)	0	—	—	ns
164	TalH2alL	ALE Pulse Width	—	$0.25 T_{CY}$	—	ns
165	ToeL2oeH	\overline{OE} Pulse Width	$0.5 T_{CY} - 5$	$0.5 T_{CY}$	—	ns
166	TalH2alH	ALE ↑ to ALE ↑ (cycle time)	—	T_{CY}	—	ns
167	Tacc	Address Valid to Data Valid	$0.75 T_{CY} - 25$	—	—	ns
168	Toe	\overline{OE} ↓ to Data Valid	—	—	$0.5 T_{CY} - 25$	ns
169	TalL2oeH	ALE ↓ to \overline{OE} ↑	$0.625 T_{CY} - 10$	—	$0.625 T_{CY} + 10$	ns
171	TalH2csL	Chip Enable Active to ALE ↓	$0.25 T_{CY} - 20$	—	—	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	—	—	10	ns

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FIGURE 27-9: PROGRAM MEMORY WRITE TIMING DIAGRAM

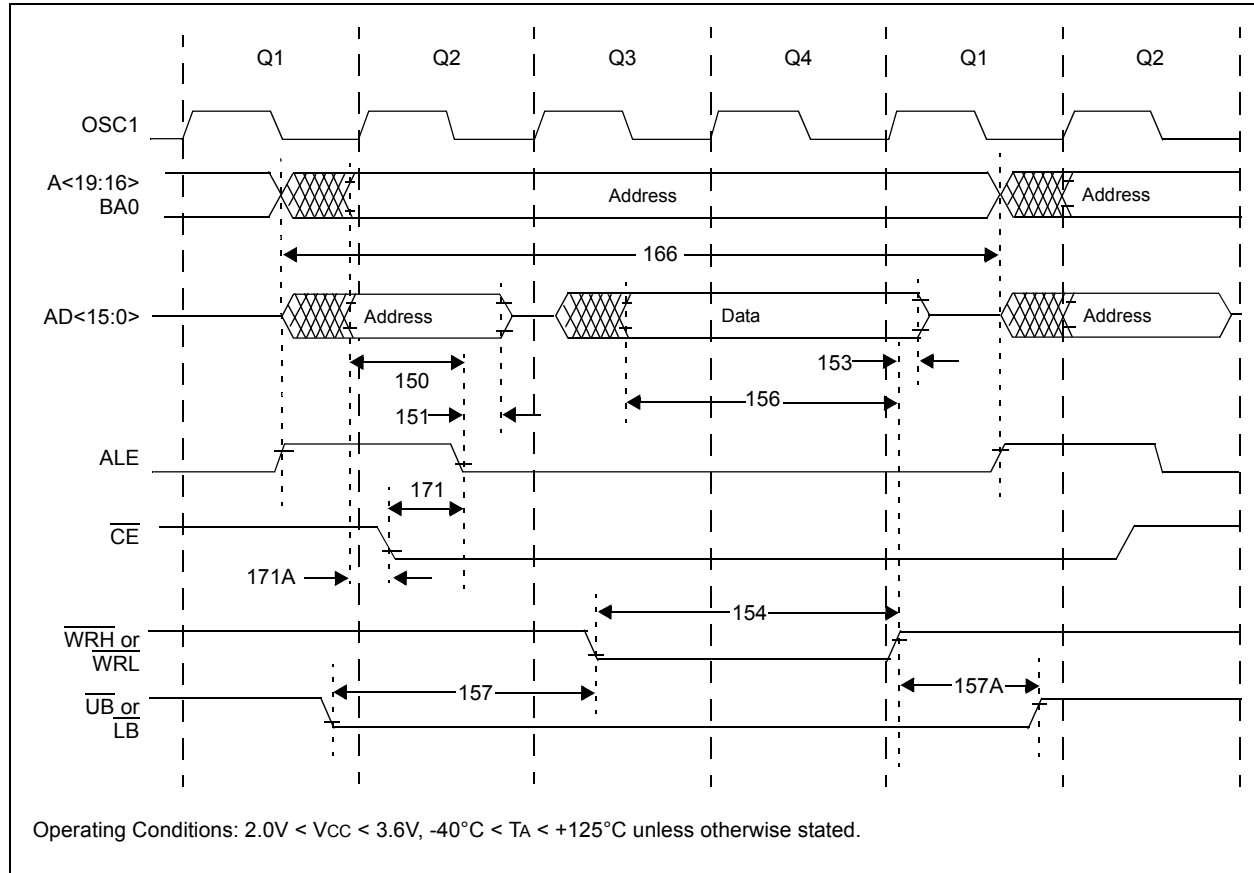


TABLE 27-11: PROGRAM MEMORY WRITE TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2aL	Address Out Valid to ALE ↓ (address setup time)	0.25 T _{CY} – 10	—	—	ns
151	TaIL2adI	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
153	TwrH2adI	WRN ↑ to Data Out Invalid (data hold time)	5	—	—	ns
154	TwrL	WRN Pulse Width	0.5 T _{CY} – 5	0.5 T _{CY}	—	ns
156	TadV2wrH	Data Valid before WRN ↑ (data setup time)	0.5 T _{CY} – 10	—	—	ns
157	TbsV2wrL	Byte Select Valid before WRN ↓ (byte select setup time)	0.25 T _{CY}	—	—	ns
157A	TwrH2bsI	WRN ↑ to Byte Select Invalid (byte select hold time)	0.125 T _{CY} – 5	—	—	ns
166	TaIH2aIH	ALE ↑ to ALE ↑ (cycle time)	—	T _{CY}	—	ns
171	TaIH2csL	Chip Enable Active to ALE ↓	0.25 T _{CY} – 20	—	—	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	—	—	10	ns

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FIGURE 27-15: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)

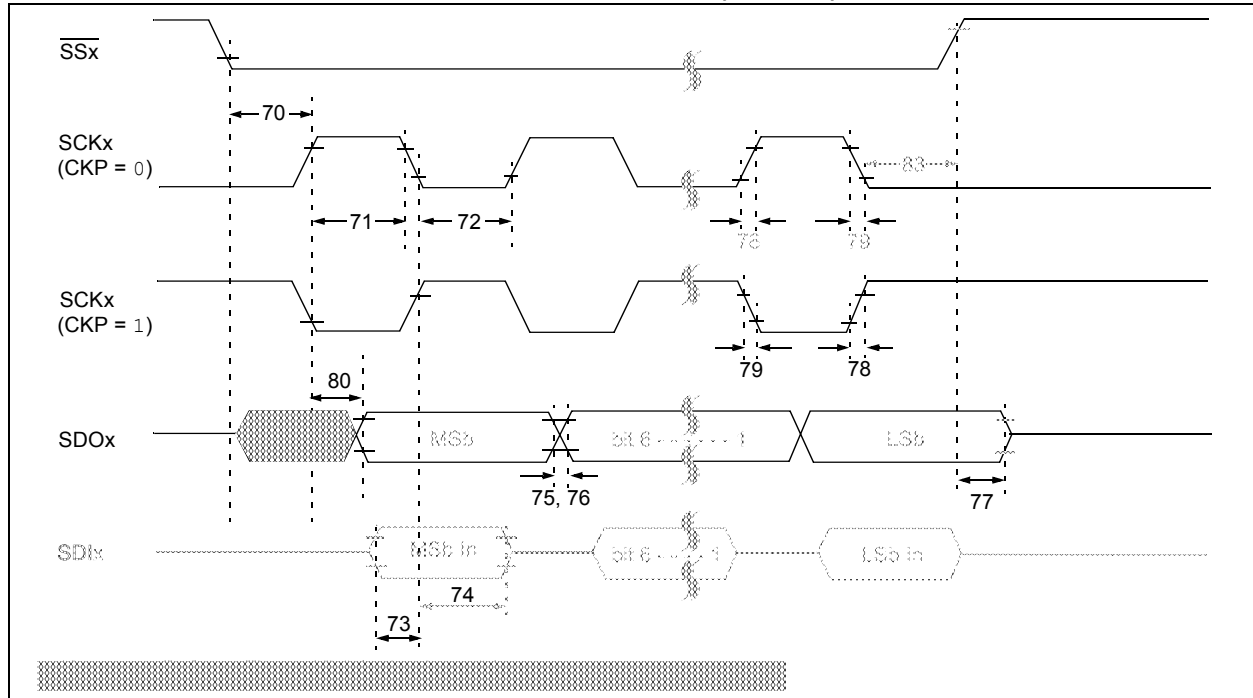


TABLE 27-18: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2sch, TssL2scl	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input		Tcy	—	ns	
71	Tsch	SCKx Input High Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
71A			Single Byte	40	—	ns	(Note 1)
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	—	ns	(Note 1)
73	TdIV2sch, TdIV2scl	Setup Time of SDIx Data Input to SCKx Edge		20	—	ns	
73A	Tb2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 Tcy + 40	—	ns	(Note 2)
74	Tsch2dIL, TscL2dIL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time		—	25	ns	
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance		10	50	ns	
80	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge		—	50	ns	
83	Tsch2ssH, TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge		1.5 Tcy + 40	—	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

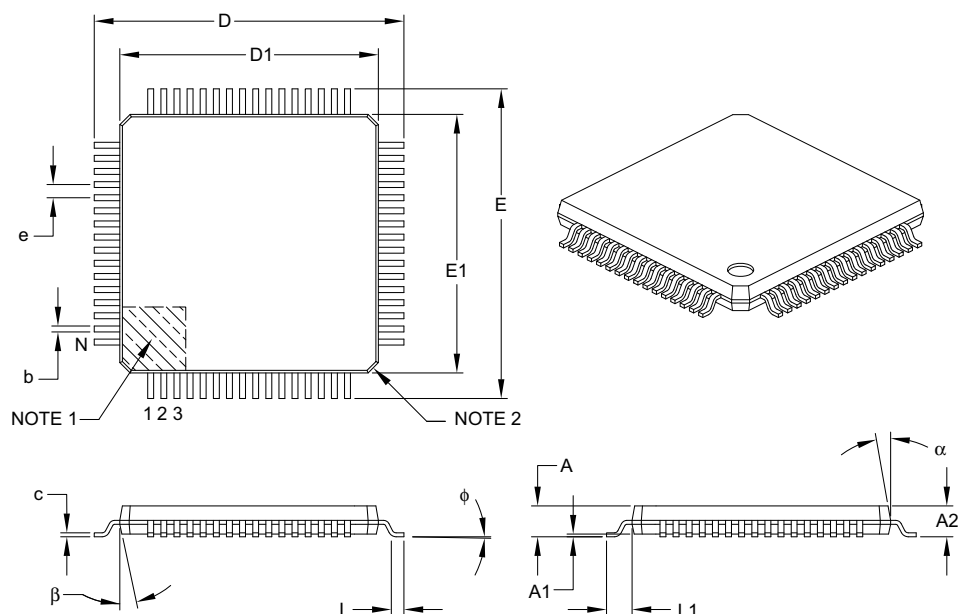
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28.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		64		
Lead Pitch	e		0.50 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

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