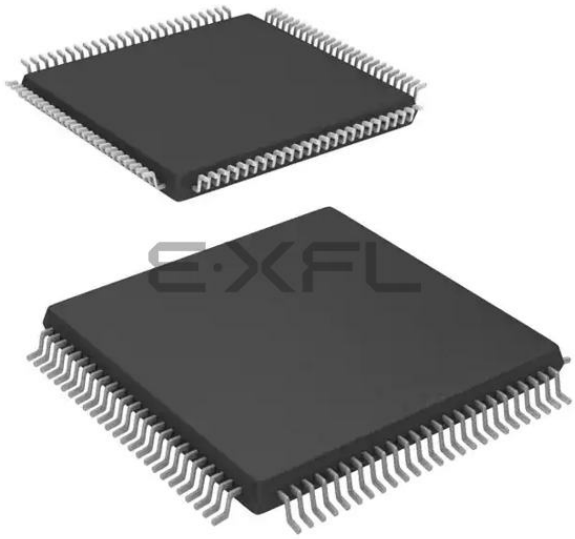

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Applications of "Embedded - Microcontrollers"

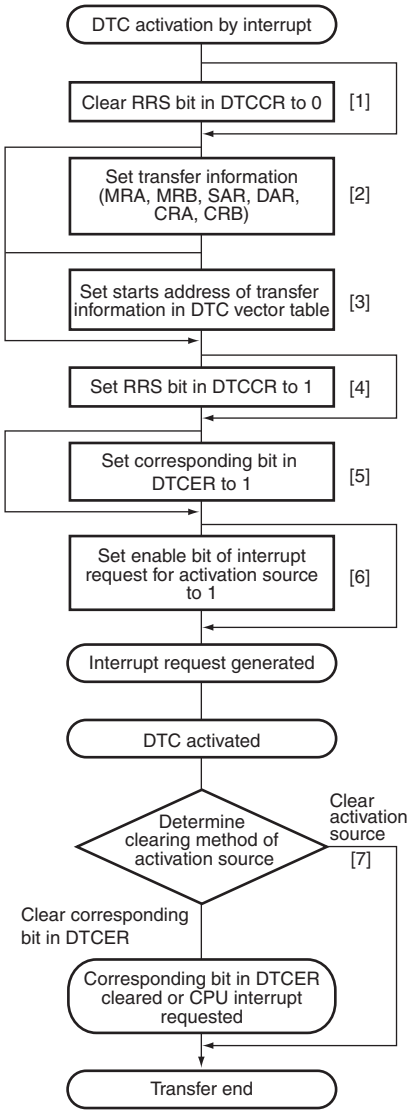
Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/de70835rn80ftv

Bit	Bit Name	Initial Value	R/W	Description
2, 1	—	All 0	R	Reserved These are read-only bits and cannot be modified.
0	ERR	0	R/(W)*	Transfer Stop Flag Indicates that the DTC address error or NMI interrupt request has occurred. If a DTC address error or NMI interrupt occurs while the DTC is active, address error handling or NMI interrupt handling processing is executed after the DTC has released the bus mastership. The DTC stops in the transfer information writing state after transferring data. 0: No interrupt occurs 1: An interrupt occurs [Clearing condition] • When writing 0 after reading 1

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

8.6 DTC Activation by Interrupt

The procedure for using the DTC with interrupt activation is shown in figure 8.18.



[1] Clearing the RRS bit in DTCCR to 0 clears the read skip flag of transfer information. Read skip is not performed when the DTC is activated after clearing the RRS bit. When updating transfer information, the RRS bit must be cleared.

[2] Set the MRA, MRB, SAR, DAR, CRA, and CRB transfer information in the data area. For details on setting transfer information, see section 8.2, Register Descriptions. For details on location of transfer information, see section 8.4, Location of Transfer Information and DTC Vector Table.

[3] Set the start address of the transfer information in the DTC vector table. For details on setting DTC vector table, see section 8.4, Location of Transfer Information and DTC Vector Table.

[4] Setting the RRS bit to 1 performs a read skip of second time or later transfer information when the DTC is activated consecutively by the same interrupt source. Setting the RRS bit to 1 is always allowed. However, the value set during transfer will be valid from the next transfer.

[5] Set the bit in DTCER corresponding to the DTC activation interrupt source to 1. For the correspondence of interrupts and DTCER, refer to table 8.2. The bit in DTCER may be set to 1 on the second or later transfer. In this case, setting the bit is not needed.

[6] Set the enable bits for the interrupt sources to be used as the activation sources to 1. The DTC is activated when an interrupt used as an activation source is generated. For details on the settings of the interrupt enable bits, see the corresponding descriptions of the corresponding module.

[7] After the end of one data transfer, the DTC clears the activation source flag or clears the corresponding bit in DTCER and requests an interrupt to the CPU. The operation after transfer depends on the transfer information. For details, see section 8.2, Register Descriptions and figure 8.4.

Figure 8.18 Activation of DTC by Interrupt

Address	Area	Memory Type	Capacity	Bus Width
H'18000000 to H'1BFFFFFF	CS6 space	Normal space SRAM with byte selection PCMCIA Burst MPX-I/O	64 Mbytes	8, 16, or 32 bits*[2]
H'1C000000 to H'1FFFFFFF	CS7 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*[2]
H'20000000 to H'FFF7FFFF	Reserved			
H'FFF80000 to H'FFF9FFFF	SDRAM mode setting space			
H'FFFA0000 to H'FFFF3FFF	Reserved			
H'FFFF4000 to H'FFFFBFFF	On-chip RAM		32 Kbytes	32 bits
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral modules		16 Kbytes	8 or 16 bits

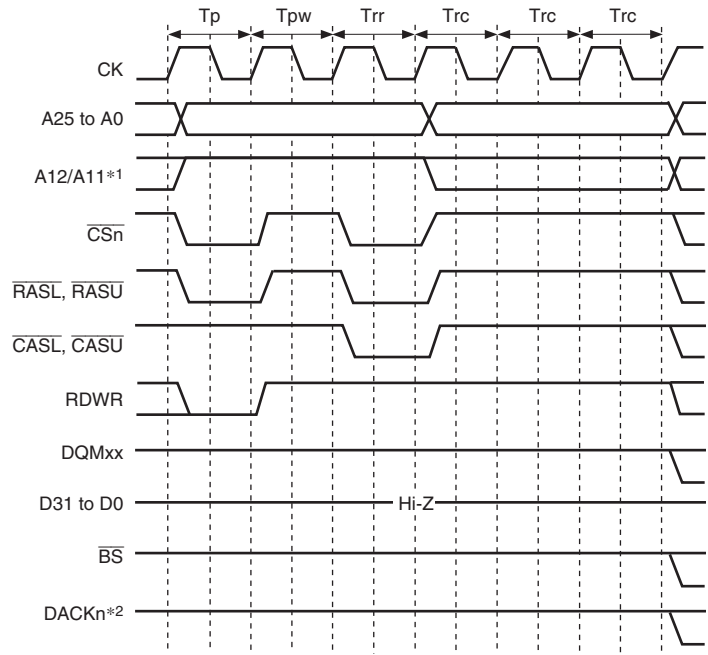
Notes: Do not access the reserved area. If the reserved area is accessed, the correct operation cannot be guaranteed.

1. The bus width is selected by the mode pins.
2. The bus width is selected by the register setting.

Table 9.14 Address Map: SH7086 in On-Chip ROM-Enabled Mode

Address	Area	Memory Type	Capacity	Bus Width
H'00000000 to H'0007FFFF	On-chip ROM		512 Kbytes	32 bits
H'00080000 to H'01FFFFFF	Reserved			
H'02000000 to H'03FFFFFF	CS0 space	Normal space SRAM with byte selection Burst ROM (asynchronous) Burst ROM (synchronous)	32 Mbytes	8, 16, or 32 bits*
H'04000000 to H'07FFFFFF	CS1 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*

Address	Area	Memory Type	Capacity	Bus Width
H'08000000 to H'0BFFFFFF	CS2 space	Normal space SRAM with byte selection SDRAM	64 Mbytes	8, 16, or 32 bits*
H'0C000000 to H'0FFFFFFF	CS3 space	Normal space SRAM with byte selection SDRAM	64 Mbytes	8, 16, or 32 bits*
H'10000000 to H'13FFFFFF	CS4 space	Normal space SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes	8, 16, or 32 bits*
H'14000000 to H'17FFFFFF	CS5 space	Normal space SRAM with byte selection PCMCIA MPX-I/O	64 Mbytes	8, 16, or 32 bits*
H'18000000 to H'1BFFFFFF	CS6 space	Normal space SRAM with byte selection PCMCIA Burst MPX-I/O	64 Mbytes	8, 16, or 32 bits*
H'1C000000 to H'1FFFFFFF	CS7 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*
H'20000000 to H'3FFFFFFF	Reserved			
H'40000000 to H'7FFFFFFF	CS8 space	Normal space SRAM with byte selection	1 Gbyte	8, 16, or 32 bits*
H'80000000 to H'FFF7FFFF	Reserved			
H'FFF80000 to H'FFF9FFFF	SDRAM mode setting space			
H'FFFA0000 to H'FFFF3FFF	Reserved			



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.29 Auto-Refresh Timing

2. Self-refreshing

Self-refresh mode is a kind of standby mode in which the refresh timing and refresh addresses are generated within SDRAM. Self-refreshing is activated by setting both the RMODE bit and the RFSH bit in SDCR to 1. After starting the self-refreshing, PALL command is issued in the Tp cycle after the completion of the precharging bank. A SELF command is then issued after inserting idle cycles of which number is specified by the WTRP[1:0] bits in CS3WCR. SDRAM cannot be accessed while in the self-refresh state. Self-refresh mode is cleared by clearing the RMODE bit to 0. After self-refresh mode has been cleared, command issuance is disabled for the number of cycles specified by the WTRC[1:0] bits in CS3WCR.

Self-refresh timing is shown in figure 9.30. After self-refreshing is cleared, settings must be made so that auto-refreshing is performed at the correct intervals. When self-refreshing is activated from the state in which auto-refreshing is set, auto-refreshing is restarted if the RFSH bit is set to 1 and the RMODE bit is cleared to 0 when self-refresh mode is cleared. If the transition from clearing of self-refresh mode to the start of auto-refreshing takes time, making the RTCNT value 1 less than the RTCOR value will enable auto-refreshing to be started immediately.

Bus Mode and Channel Priority: When the priority is set in fixed mode (CH0 > CH1) and channel 1 is transferring in burst mode, if there is a transfer request to channel 0 with a higher priority, the transfer of channel 0 will begin immediately.

At this time, if channel 0 is also operating in burst mode, the channel 1 transfer will continue after the channel 0 transfer has completely finished.

When channel 0 is in cycle steal mode, channel 0 with a higher priority performs the transfer of one transfer unit and the channel 1 transfer is continuously performed without releasing the bus mastership. The bus mastership will then switch between the two in the order channel 0, channel 1, channel 0, and channel 1. Therefore, the bus state is such that the CPU cycle after the completion of cycle steal mode transfer has been replaced with the channel 1 burst mode transfer. (Hereinafter referred to as burst mode priority execution.)

This example is shown in figure 10.13. When multiple channels are operating in burst modes, the channel with the highest priority is executed first.

When DMA transfer is executed in the multiple channels, the bus mastership will not be given to the bus master until all competing burst transfers are complete.

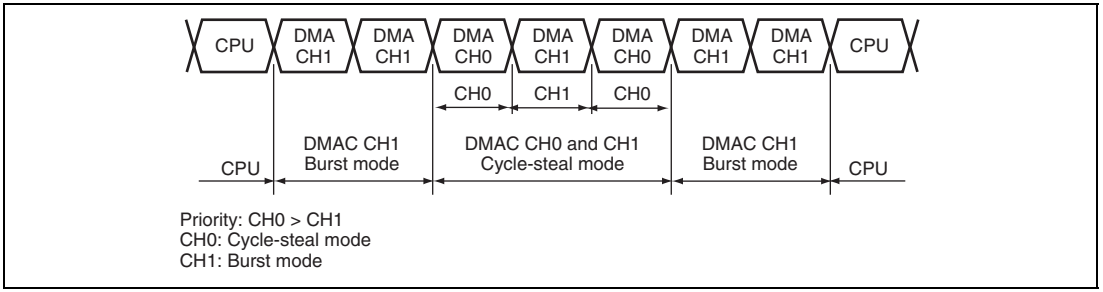


Figure 10.13 Bus State when Multiple Channels Are Operating

In round-robin mode, the priority changes according to the specification shown in figure 10.3. However, the channel in cycle steal mode cannot be mixed with the channel in burst mode.

10.4.5 Number of Bus Cycle States and DREQ Pin Sampling Timing

Number of Bus Cycle States: When the DMAC is the bus master, the number of bus cycle states is controlled by the bus state controller (BSC) in the same way as when the CPU is the bus master. For details, see section 9, Bus State Controller (BSC).

DREQ Pin Sampling Timing: Figures 10.14 to 10.17 show the sample timing of the DREQ input in each bus mode, respectively.
Determination of DMAC activation by DREQ takes 3 × Bcyc (Bcyc is the external clock (Bϕ = CK) cycle). Timing of the DACK output for the first DREQ acceptance differs depending on the internal bus state, the AM bit setting in CHCR, and the configuration of the BSC regarding the transfer source/destination areas, but the fastest case is 6 × Bcyc.

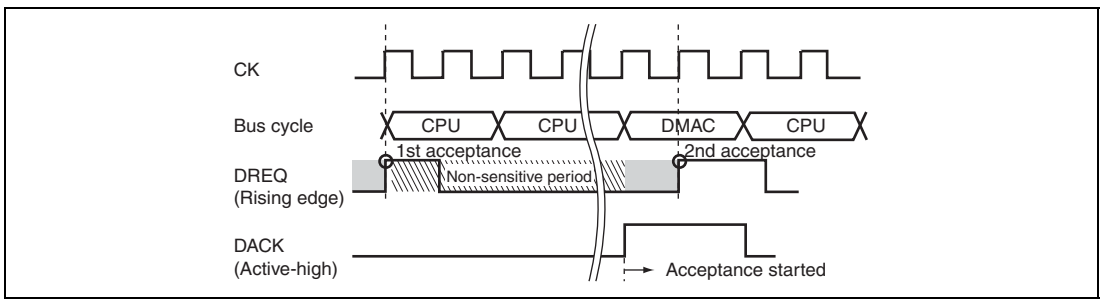


Figure 10.14 Example of DREQ Input Detection in Cycle Steal Mode Edge Detection

Bit	Bit Name	Initial Value	R/W	Description
1	CMFV5	0	R/(W)*[1]	Compare Match/Input Capture Flag V5 Status flag that indicates the occurrence of TGRV_5 input capture or compare match. [Setting conditions] • When TCNTV_5 = TGRV_5 and TGRV_5 is functioning as output compare register • When TCNTV_5 value is transferred to TGRV_5 by input capture signal and TGRV_5 is functioning as input capture register • When TCNTV_5 value is transferred to TGRV_5 and TGRV_5 is functioning as a register for measuring the pulse width of the external input signal. The transfer timing is specified by the IOC bits in timer I/O control register V_5 (TIORV_5).*[2] [Clearing conditions] • When DTC is activated by a TGIV_5 interrupt and the DISEL bit of MRB in DTC is 0 • When 0 is written to CMFV5 after reading CMFV5 = 1

Table 11.57 MTU2 Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	DMAC Activation	DTC Activation	Priority
0	TGIA_0	TGRA_0 input capture/compare match	TGFA_0	Possible	Possible	High
	TGIB_0	TGRB_0 input capture/compare match	TGFB_0	Not possible	Possible	
	TGIC_0	TGRC_0 input capture/compare match	TGFC_0	Not possible	Possible	
	TGID_0	TGRD_0 input capture/compare match	TGFD_0	Not possible	Possible	
	TCIV_0	TCNT_0 overflow	TCFV_0	Not possible	Not possible	
	TGIE_0	TGRE_0 compare match	TGFE_0	Not possible	Not possible	
	TGIF_0	TGRF_0 compare match	TGFF_0	Not possible	Not possible	
1	TGIA_1	TGRA_1 input capture/compare match	TGFA_1	Possible	Possible	
	TGIB_1	TGRB_1 input capture/compare match	TGFB_1	Not possible	Possible	
	TCIV_1	TCNT_1 overflow	TCFV_1	Not possible	Not possible	
	TCIU_1	TCNT_1 underflow	TCFU_1	Not possible	Not possible	
2	TGIA_2	TGRA_2 input capture/compare match	TGFA_2	Possible	Possible	
	TGIB_2	TGRB_2 input capture/compare match	TGFB_2	Not possible	Possible	
	TCIV_2	TCNT_2 overflow	TCFV_2	Not possible	Not possible	
	TCIU_2	TCNT_2 underflow	TCFU_2	Not possible	Not possible	
3	TGIA_3	TGRA_3 input capture/compare match	TGFA_3	Possible	Possible	
	TGIB_3	TGRB_3 input capture/compare match	TGFB_3	Not possible	Possible	
	TGIC_3	TGRC_3 input capture/compare match	TGFC_3	Not possible	Possible	
	TGID_3	TGRD_3 input capture/compare match	TGFD_3	Not possible	Possible	
	TCIV_3	TCNT_3 overflow	TCFV_3	Not possible	Not possible	
4	TGIA_4	TGRA_4 input capture/compare match	TGFA_4	Possible	Possible	
	TGIB_4	TGRB_4 input capture/compare match	TGFB_4	Not possible	Possible	
	TGIC_4	TGRC_4 input capture/compare match	TGFC_4	Not possible	Possible	
	TGID_4	TGRD_4 input capture/compare match	TGFD_4	Not possible	Possible	
	TCIV_4	TCNT_4 overflow/underflow	TCFV_4	Not possible	Possible	
5	TGIU_5	TGRU_5 input capture/compare match	TGFU_5	Not possible	Possible	
	TGIV_5	TGRV_5 input capture/compare match	TGFV_5	Not possible	Possible	
	TGIW_5	TGRW_5 input capture/compare match	TGFW_5	Not possible	Possible	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

Bit	Bit Name	Initial Value	R/W	Description
4	SOL	0	R/W	Serial Data Output Value Select The serial data output retains its level of the last bit after completion of transmission. The output level before or after transmission can be specified by setting this bit. When specifying the output level, use the MOV instruction after clearing the SOLP bit to 0. Since writing to this bit during data transmission causes malfunctions, this bit should not be changed. 0: Serial data output is changed to low. 1: Serial data output is changed to high.
3	SOLP	1	R/W	SOL Bit Write Protect When changing the output level of serial data, set the SOL bit to 1 or clear the SOL bit to 0 after clearing the SOLP bit to 0 using the MOV instruction. 0: Output level can be changed by the SOL bit 1: Output level cannot be changed by the SOL bit. This bit is always read as 1.
2	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
1, 0	CSS[1:0]	01	R/W	$\overline{\text{SCS}}$ Pin Select Select that the $\overline{\text{SCS}}$ pin functions as $\overline{\text{SCS}}$ input or output. 00: Setting prohibited 01: Setting prohibited 10: Function as $\overline{\text{SCS}}$ automatic input/output (function as $\overline{\text{SCS}}$ input before and after transfer and output a low level during transfer) 11: Function as $\overline{\text{SCS}}$ automatic output (outputs a high level before and after transfer and outputs a low level during transfer)

- Writing 1 to IICRST does not clear the BBSY bit in ICCR2 to 0. However, if the states of the SCL and SDA pins lead to the generation of a stop condition, (rising edge on SDA while SCL is at the high level), the BBSY bit may be cleared to 0 as a result. This can also affect other bits in the same way.
- Data transfer stops while a reset is being applied by writing 1 to IICRST. However, functions for detecting start conditions, stop conditions, and failure in bus contention continue to operate. Signals input to the SCL and SDA pins may alter the states of ICCR1, ICCR2, and ICSR.

18.3.3 I²C Bus Mode Register (ICMR)

ICMR is an 8-bit readable/writable register that selects whether the MSB or LSB is transferred first and selects the transfer bit count.

ICMR is initialized to H'38 by a power-on reset. Bits BC[2:0] are initialized to B'000 by the IICRST bit in ICCR2.

Bit:	7	6	5	4	3	2	1	0
	MLS	-	-	-	BCWP	BC[2:0]		
Initial value:	0	0	1	1	1	0	0	0
R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I²C bus format is used.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Table 21.14 SH7086 Multiplexed Pins (Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)
E	PE0 I/O (port)	DREQ0 input (DMAC)	TIOC0A I/O (MTU2)	AUDCK output (AUD)*1	—	—
	PE1 I/O (port)	TEND0 output (DMAC)	TIOC0B I/O (MTU2)	—	—	—
	PE2 I/O (port)	DREQ1 input (DMAC)	TIOC0C I/O (MTU2)	—	—	—
	PE3 I/O (port)	TEND1 output (DMAC)	TIOC0D I/O (MTU2)	AUDATA3 output (AUD)*1	—	—
	PE4 I/O (port)	$\overline{\text{IOIS16}}$ input (BSC)	TIOC1A I/O (MTU2)	RXD3 input (SCIF)	AUDATA2 output (AUD)*1	—
	PE5 I/O (port)	$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$ output (BSC)	TIOC1B I/O (MTU2)	TXD3 output (SCIF)	AUDATA1 output (AUD)*1	—
	PE6 I/O (port)	$\overline{\text{CS7}}$ output (BSC)	TIOC2A I/O (MTU2)	SCK3 I/O (SCIF)	AUDATA0 output (AUD)*1	—
	PE7 I/O (port)	$\overline{\text{BS}}$ output (BSC)	TIOC2B I/O (MTU2)	$\overline{\text{UBCTRG}}$ output (UBC)	RXD2 input (SCI)	SSI I/O (SSU)
	PE8 I/O (port)	TIOC3A I/O (MTU2)	SCK2 I/O (SCI)	SSCK I/O (SSU)	TMS input (H-UDI)*2	—
	PE9 I/O (port)	TIOC3B I/O (MTU2)	SCK3 I/O (SCIF)	$\overline{\text{RTS3}}$ output (SCIF)	$\overline{\text{TRST}}$ input (H-UDI)*2	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	TXD2 output (SCI)	SSO I/O (SSU)	TDI input (H-UDI)*2	—
	PE11 I/O (port)	TIOC3D I/O (MTU2)	RXD3 input (SCIF)	$\overline{\text{CTS3}}$ input (SCIF)	TDO output (H-UDI)*2	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	TXD3 output (SCIF)	$\overline{\text{SCS}}$ I/O (SSU)	TCK input (H-UDI)*2	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	$\overline{\text{ASEBRKAK}}$ output (E10A)*2	$\overline{\text{ASEBRK}}$ input (E10A)*2	—
	PE14 I/O (port)	$\overline{\text{WRHH}}$/$\overline{\text{ICIOWR}}$/$\overline{\text{AH}}$ /DQMUU output (BSC)	DACK0 output (DMAC)	TIOC4C I/O (MTU2)	—	—
	PE15 I/O (port)	CKE output (BSC)	DACK1 output (DMAC)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—
	PE16 I/O (port)	$\overline{\text{CS8}}$ output (BSC)	TIOC3BS I/O (MTU2S)	—	—	—
	PE17 I/O (port)	TIOC3DS I/O (MTU2S)	—	—	—	—

22.2.3 Port B Port Register L (PBPRL)

The port B port register L (PBPRL) is a 16-bit read-only register that always returns the states of the pins regardless of the PFC setting. Bits PB9PR to PB4PR and PB2PR to PB0PR correspond to pins PB9 to PB4 and PB2 to PB0, respectively (multiplexed functions omitted here) in the SH7083. Bits PB9PR to PB0PR correspond to pins PB9 to PB0 (multiplexed functions omitted here) in the SH7084, SH7085, and SH7086

- PBPRL (SH7083)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PB9PR	PB8PR	PB7PR	PB6PR	PB5PR	PB4PR	-	PB2PR	PB1PR	PB0PR
Initial value:	0	0	0	0	0	0	*	*	*	*	*	*	0	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PB9PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
8	PB8PR	Pin state	R	
7	PB7PR	Pin state	R	
6	PB6PR	Pin state	R	
5	PB5PR	Pin state	R	
4	PB4PR	Pin state	R	
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PB2PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
1	PB1PR	Pin state	R	
0	PB0PR	Pin state	R	

23.4.4 RAM Emulation Register (RAMER)

When the realtime programming of the user MAT is emulated, RAMER sets the area of the user MAT which is overlapped with a part of the on-chip RAM. The RAM emulation must be executed in user mode or in user program mode.

For the division method of the user-MAT area, see table 23.7. In order to operate the emulation function certainly, the target MAT of the RAM emulation must not be accessed immediately after RAMER is programmed. If it is accessed, the normal access is not guaranteed.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	RAMS	RAM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RAMS	0	R/W	RAM Select Sets whether the user MAT is emulated or not. When RAMS = 1, all blocks of the user MAT are in the programming/erasing protection state. 0: Emulation is not selected Programming/erasing protection of all user-MAT blocks is invalid 1: Emulation is selected Programming/erasing protection of all user-MAT blocks is valid
2 to 0	RAM[2:0]	000	R/W	User MAT Area Select These bits are used with bit 3 to select the user-MAT area to be overlapped with the on-chip RAM. (See table 23.7.)

- Command Error

Command errors are generated by undefined commands, commands sent in an incorrect order, and the inability to accept a command. For example, sending the clock-mode selection command before device selection or an inquiry command after the transition-to-programming/erasure state command generates a command error.

Error response	H'80	H'xx

— Error response H'80 (1 byte): Command error
— Command H'xx (1 byte): Received command

- Order of Commands

In the inquiry-and-selection state, commands should be sent in the following order.

1. Send the inquiry on supported devices command (H'20) to get the list of supported devices.
2. Select a device from the returned device information, and send the device selection command (H'10) to select that device.
3. Send the inquiry on clock mode command (H'21) to get the available clock modes.
4. Select a clock mode from among the returned clock modes, and send the clock-mode selection command (H'11).
5. After selection of the device and clock mode, send the commands to inquire about frequency multipliers (H'22) and operating frequencies (H'23) to get the information required to select a new bit rate.
6. Taking into account the returned information on the frequency multipliers and operating frequencies, send a new-bit-rate selection command (H'3F).
7. After the device and clock mode have been selected, get the information required for programming and erasure of the user boot MAT and user MAT by sending the commands to inquire about the user boot MAT (H'24), user MAT (H'25), erasure block (H'26), and programming size (H'27).
8. After making all necessary inquiries and the new bit rate selection, send the transition-to-programming/erasure state command (H'40) to place the boot program in the programming/erasure state.

28.3.8 Watchdog Timer (WDT) Timing

Table 28.13 Watchdog Timer (WDT) Timing

Conditions: V_{CC} = 3.0 V to 3.6 V or 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +85°C (consumer applications), T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	50	ns	Figure 28.50

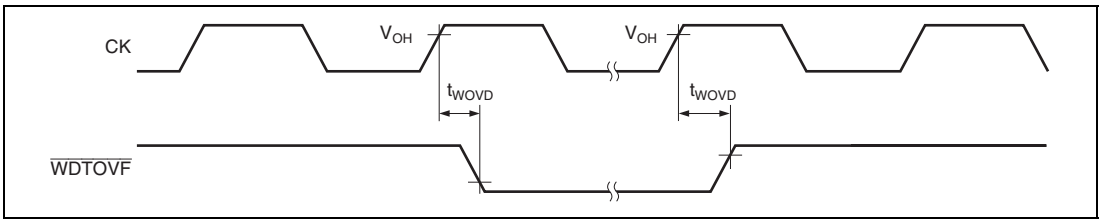


Figure 28.50 WDT Timing

[Legend]

I: Input

O: Output

H: High-level output

L: Low-level output

Z: High-impedance

K: Input pins become high-impedance, and output pins retain their state.

Notes:
1. Output pins become high-impedance when the HIZ bit in standby control register 6 (STBCR6) is set to 1.
2. Becomes output when the HIZCNT bit in the common control register (CMNCR) is set to 1.
3. Becomes output when the HIZMEM bit in the common control register (CMNCR) is set to 1.
4. Becomes high-impedance when the MZIZDL bit in the high-current port control register (HCPCR) is cleared to 0.
5. Becomes high-impedance when the MZIZEL bit in the high-current port control register (HCPCR) is cleared to 0.
6. Becomes input during a power-on reset. Pull-up to prevent erroneous operation. Pull-down with a resistance of at least 1 MΩ as required.
7. Pulled-up inside the LSI when there is no input.

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
Overall	—	"I²C2" changed to "IIC2"
3.1 Selection of Operating Modes Table 3.1 Selection of Operating Modes*1	55	Table amended

	Pin Setting					Bus Width of CS0 Space			
Mode No.	FWE	MD1	MD0	Mode Name	On-Chip ROM	SH7083	SH7084	SH7085	SH7086
Mode 0	0	0	0	MCU extension mode 0	Not active	8	8	16	16
Mode 1	0	0	1	MCU extension mode 1	Not active	16	16	32	32
Mode 2	0	1	0	MCU extension mode 2	Active	Set by CS0BCR in BSC			
Mode 3	0	1	1	Single chip mode	Active	—			
Mode 4*2	1	0	0	Boot mode	Active	—			
Mode 5*2	1	0	1	User boot mode	Active	Set by CS0BCR in BSC			
Mode 6*2	1	1	0	User programming mode	Active	Set by CS0BCR in BSC			
Mode 7*2	1	1	1			—			

Notes: 1. Do not input a low-level signal to $\overline{\text{ASEMD0}}$ when the MCU is not connected to the E10A. Operation cannot be guaranteed if a low-level signal is input to $\overline{\text{ASEMD0}}$ when the E10A is not connected. For information on connecting the E10A, see SuperH™ Family E10A-USB Emulator, Additional Document for User's Manual: Supplementary Information on Using the SH7083, SH7084, SH7085, and SH7086.

2. These are flash memory programming modes.

5.8.4 Notes on Slot Illegal Instruction Exception Handling	103	Description deleted 3. Others The slot illegal instruction exception handling may be generated in this LSI in a case where the instruction is described in assembler or when the middleware of the object is introduced.
8.2.2 DTC Mode Register B (MRB)	176	Table amended

Bit	Bit Name	Initial Value	R/W	Description
5	DISEL	Undefined	—	DTC Interrupt Select When this bit is set to 1, an interrupt request is generated to the CPU every time a data transfer or a block transfer ends. When this bit is set to 0, a CPU interrupt request is only generated when the specified number of data transfers end. Note: This bit should be cleared to 0 when the IIC2 is selected as the activation source.

Item	Page	Revision (See Manual for Details)
15.5 Interrupt Sources and DMAC/DTC Table 15.14 SCI Interrupt Sources	801	Table amended

Interrupt Source	Description	Interrupt Enable Bit	DMAC/DTC Activation	Priority
ERI	Interrupt caused by receive error (ORER, FER, or PER)	RIE = 1	Not possible	High
RXI	Interrupt caused by receive data full (RDRF)	RIE = 1 and EIO = 0	Possible	
TXI	Interrupt caused by transmit data empty (TDRE)	TIE = 1	Possible	
TEI	Interrupt caused by transmit end (TEND)	TEIE = 1	Not possible	Low

15.6 Serial Port Register (SCSPTR) and SCI Pins Figure 15.19 SPB1IO Bit, SPB1DT bit, and SCK Pin	801	Figure and title amended

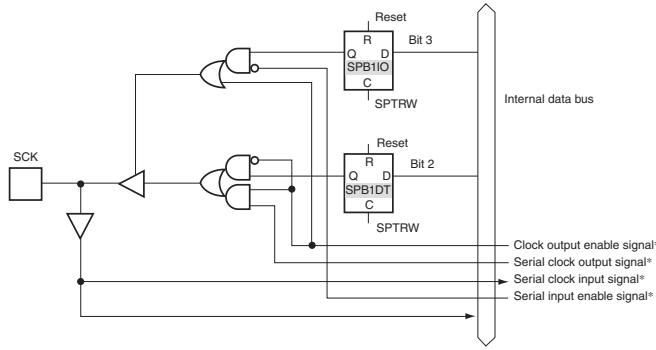
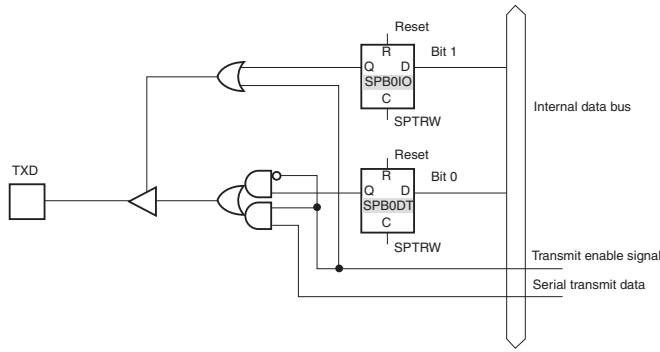
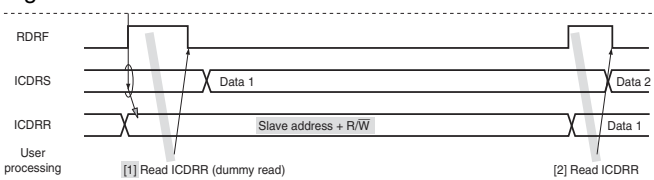


Figure 15.20 SPB0IO Bit, SPB0DT bit, and TXD Pin	802	Figure and title amended



Item	Page	Revision (See Manual for Details)
18.4.5 Slave Receive Operation	950	Description amended The reception procedure and operations in slave receive mode are described below. For operation up to reception of the 1st frame (slave address + R/$\overline{W}$), see 18.4.4, Slave Transmit Operation. 1. Perform a dummy read of ICDRR. (The read data indicates slave address + R/$\overline{W}$, and is therefore unnecessary.) The slave device outputs to SDA the level indicated by the setting of ACKBT in ICIER at the 9th clock pulse of the receive clock. 2. After reception of one frame of data finishes, RDRF in ICSR is set to 1 at the rising edge of the 9th receive clock pulse. At this time, the received data can be read by reading ICDRR, and RDRF is cleared to 0 simultaneously. Continuous receive operation can be accomplished by reading ICDRR each time RDRF is set to 1. If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read. 3. If the next receive operation is the final frame, set ACKBT in ICIER to 1 before reading ICDRR. 4. When RDRF in ICSR is set to 1, read the final receive data from ICDRR.
Figure 18.12 Slave Receive Mode Operation Timing (1)		Figure amended 
Figure 18.13 Slave Receive Mode Operation Timing (2)	951	Figure amended