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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/de70855rn80fpv

4.2 Input/Output Pins

Table 4.2 shows the CPG pin configuration.

Table 4.2 Pin Configuration

Pin Name	Abbr.	I/O	Description
Crystal input/output pins (clock input pins)	XTAL	Output	Connects a crystal resonator.
	EXTAL	Input	Connects a crystal resonator or an external clock.
Clock output pin	CK	Output	Outputs an external clock.

Note: To use the clock output (CK) pin, appropriate settings may be needed for the pin in the pin function controller (PFC) in some cases. For details, refer to section 21, Pin Function Controller (PFC).

Address	Area	Memory Type	Capacity	Bus Width
H'FFF80000 to H'FFF9FFFF	SDRAM mode setting space			
H'FFFA0000 to H'FFFF7FFF	Reserved			
H'FFFF8000 to H'FFFFBFFF	On-chip RAM		16 Kbytes	32 bits
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral modules		16 Kbytes	8 or 16 bits

Notes: Do not access the reserved area. If the reserved area is accessed, the correct operation cannot be guaranteed. In single-chip mode, only the on-chip ROM, on-chip RAM, and on-chip peripheral modules can be accessed; the other areas cannot be accessed.

* The bus width is selected by the register setting.

Table 9.11 Address Map: SH7085 (256-Kbyte Flash Memory Version) in On-Chip ROM-Disabled Mode

Address	Area	Memory Type	Capacity	Bus Width
H'00000000 to H'03FFFFFF	CS0 space	Normal space SRAM with byte selection Burst ROM (asynchronous) Burst ROM (synchronous)	64 Mbytes	16 or 32 bits*[1]
H'04000000 to H'07FFFFFF	CS1 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*[2]
H'08000000 to H'0BFFFFFF	CS2 space	Normal space SRAM with byte selection SDRAM	64 Mbytes	8, 16, or 32 bits*[2]
H'0C000000 to H'0FFFFFFF	CS3 space	Normal space SRAM with byte selection SDRAM	64 Mbytes	8, 16, or 32 bits*[2]
H'10000000 to H'13FFFFFF	CS4 space	Normal space SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes	8, 16, or 32 bits*[2]

Bit	Bit Name	Initial Value	R/W	Description
5	DMAIWA	0	R/W	Specification for Method of Inserting Wait States between Access Cycles during DMA Single Address Transfer Specifies the method of inserting the idle cycles specified by the DMAIW1 and DMAIW0 bits. Clearing this bit will make this LSI insert the idle cycles when another device, which includes this LSI, drives the data bus after an external device with DACK drove it. When the external device with DACK drives the data bus continuously, idle cycles are not inserted. Setting this bit will make this LSI insert the idle cycles after one access is completed even when the continuous accesses to an external device with DACK are performed. 0: Idle cycles are inserted when another device drives data bus after external device with DACK drives data bus 1: Idle cycles are always inserted after external device with DACK is accessed.
4	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	HIZMEM	0	R/W	Hi-Z Memory Control Specifies the pin state in software standby mode for A29 to A0, $\overline{BS}$, $\overline{CSn}$, RDWR, $\overline{WRxx}$, $\overline{RD}$, $\overline{AH}$, $\overline{FRAME}$, $\overline{ICIORD}$, $\overline{ICIOWR}$, $\overline{WE}$, $\overline{CE1A}$, $\overline{CE1B}$, $\overline{CE2A}$, and $\overline{CE2B}$. While the bus is released, these pins are in high-impedance state regardless of this bit setting. 0: High impedance in software standby mode 1: Driven in software standby mode

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	WR[3:0]	1010	R/W	Number of Read Access Wait Cycles Specify the number of wait cycles required for read access. 0000: 0 cycles 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	WR[3:0]	1010	R/W	Number of Wait Cycles in Read Access Specify the number of wait cycles required for read access. 0000: 0 cycles 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait is valid 1: External wait is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	HW[1:0]	00	R/W	Delay Cycles from $\overline{RD}$ and $\overline{WRxx}$ Negation to Address and $\overline{CSn}$ Negation Specify the number of delay cycles from $\overline{RD}$ and $\overline{WRxx}$ negation to address and $\overline{CSn}$ negation. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

(4) SDRAM

When SDRAM is selected in areas 2 and 3, the WTRP1/0, WTRCD0/1, TRWL1/0, and WTRC1/0 bit settings are effective in both areas in common. When SDRAM should be connected to only one area, select area 3 for SDRAM connection. In this case, the normal space or SRAM with byte selection must be selected for area 2.

- CS2WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	A2CL[1:0]		-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
8, 7	A3CL[1:0]	10	R/W	CAS Latency for Area 3 Specify the CAS latency for area 3. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4, 3	TRWL[1:0]	00	R/W	Number of Wait Cycles for Precharge Activation Specify the minimum number of wait cycles to be inserted for activation of precharge. • From issuance of WRITA command by this LSI until auto precharge is activated in SDRAM: ACTV command is issued for the same bank in non-bank active mode. See the datasheet of the SDRAM to find the number of cycles taken from the acceptance of WRITA command by SDRAM until auto-precharge is activated. These bits should be set so that the above number of cycles will not exceed the number of cycles specified by these bits. • From issuance of WRIT command by this LSI until issuance of PRE command: Different row addresses in the same bank are accessed in bank active mode. The setting for areas 2 and 3 is common. 00: 0 cycle (No wait cycles) 01: 1 cycle 10: 2 cycles 11: 3 cycles
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	PCW[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of wait cycles to be inserted. 0000: 3 cycles 0001: 6 cycles 0010: 9 cycles 0011: 12 cycles 0100: 15 cycles 0101: 18 cycles 0110: 22 cycles 0111: 26 cycles 1000: 30 cycles 1001: 33 cycles 1010: 36 cycles 1011: 38 cycles 1100: 52 cycles 1101: 60 cycles 1110: 64 cycles 1111: 80 cycles
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait input is valid 1: External wait input is ignored
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Table 11.26 TIORH_4 (Channel 4)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function**	**TIOC4A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

2. Free-Running Count Operation and Periodic Count Operation:

   Immediately after a reset, the MTU2's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the MTU2 requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

   Figure 11.5 illustrates free-running counter operation.

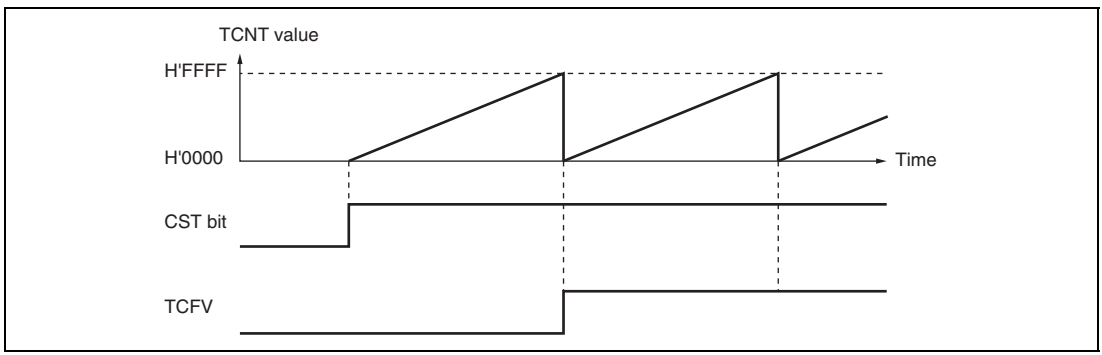


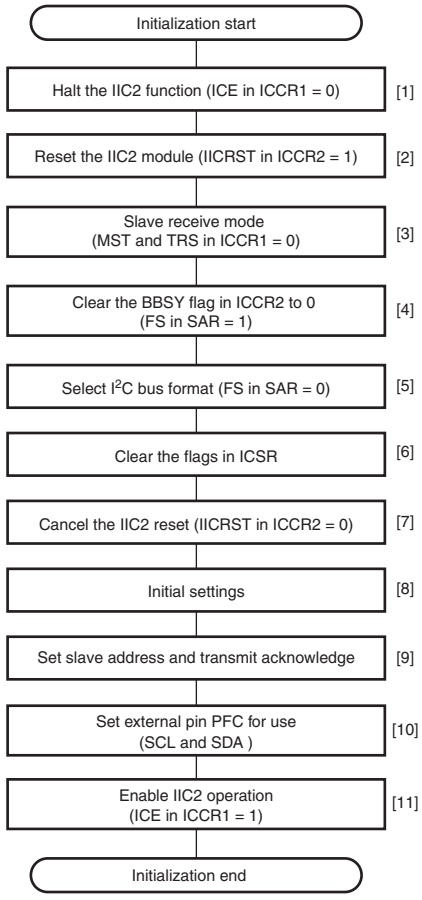
Figure 11.5 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR[2:0] in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the MTU2 requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

Bit	Bit Name	Initial value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode Selects whether the SCIF operates in asynchronous or clock synchronous mode. 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length Selects 7-bit or 8-bit data in asynchronous mode. In the clock synchronous mode, the data length is always eight bits, regardless of the CHR setting. 0: 8-bit data 1: 7-bit data* Note: * When 7-bit data is selected, the MSB (bit 7) of the transmit FIFO data register is not transmitted.
5	PE	0	R/W	Parity Enable Selects whether to add a parity bit to transmit data and to check the parity of receive data, in asynchronous mode. In clock synchronous mode, a parity bit is neither added nor checked, regardless of the PE setting. 0: Parity bit not added or checked 1: Parity bit added and checked* Note: * When PE is set to 1, an even or odd parity bit is added to transmit data, depending on the parity mode (O/$\overline{E}$) setting. Receive data parity is checked according to the even/odd (O/$\overline{E}$) mode setting.

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/(W)*[1]	Stop Condition Detection Flag [Clearing condition] • When 0 is written to STOP after reading STOP = 1 [Setting conditions] • In master mode, when a stop condition is detected after frame transfer • In slave mode, when a stop condition is detected after the slave address in the first byte that came following the detection of a start condition have matched the address set in SAR.
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag This flag indicates that arbitration was lost in master mode with the I²C bus format and that the final bit has been received while RDRF = 1 with the clock synchronous format. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface 2 detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been occupied by another master. [Clearing condition] • When 0 is written to AL/OVE after reading AL/OVE = 1 [Setting conditions] • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • When the SDA pin outputs high in master mode while a start condition is detected • When the final bit is received with the clock synchronous format while RDRF = 1



[1] Write 0 to the ICE bit in ICCR1 to halt functioning of the IIC2.

[2] Write 1 to the IICRST bit in ICCR2 to reset some registers and the contol part of the IIC2 module.

[3] Write 0 to the MST and TRS bits in ICCR1 to switch the operating mode to slave receiver mode.

[4] Write 1 to the FS bit in SAR to clear the BBSY flag in ICCR2 to 0.

[5] Write 0 to the FS bit in the SAR to select I²C bus format.

[6] Clear the flags in ICSR to 0.

[7] Write 0 to the IICRST bit to release the IIC2 module from the reset state.

[8] Initialize IIC2 registers (ICCR1, ICCR2, ICMR, ICIER, and NF2CYC). Clear the ICE, MST, and TRS bits in the ICCR1 to 0.

[9] Specify the slave address in the SVA[6:0] bit field in the SAR. Clear ACKBT in the ICIER to 0.

[10] Set external pin PFC for use. Set PFC while SCL and SDA are high-level.

[11] Write 1 to the ICE bit in the ICCR1 to enable transfer operation.

Note: For the procedure for initializing IIC2 when communication is in progress, see 18.4.8, Using the IICRST Bit to Reset I²C Bus Interface 2.

Figure 18.7 Flowchart of Initialization of I²C Bus Interface 2

Section 21 Pin Function Controller (PFC)

The pin function controller (PFC) is composed of registers that are used to select the functions of multiplexed pins and assign pins to be inputs or outputs. Tables 21.1 to 21.16 list the multiplexed pins of this LSI.

Tables 21.17 to 21.20 list the pin functions in each operating mode.

Table 21.1 SH7083 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA7 I/O (port)	$\overline{\text{CS3}}$ output (BSC)	TCLKB input (MTU2)	—	—
	PA8 I/O (port)	RDWR output (BSC)	IRQ2 input (INTC)	TCLKC input (MTU2)	—
	PA9 I/O (port)	CKE output (BSC)	IRQ3 input (INTC)	TCLKD input (MTU2)	—
	PA10 I/O (port)	$\overline{\text{CS0}}$ output (BSC)	$\overline{\text{POE4}}$ input (POE)	—	—
	PA12 I/O (port)	$\overline{\text{WRL}}$/DQMLL output (BSC)	$\overline{\text{POE6}}$ input (POE)	—	—
	PA13 I/O (port)	$\overline{\text{WRH}}$/DQMLU output (BSC)	$\overline{\text{POE7}}$ input (POE)	—	—
	PA14 I/O (port)	$\overline{\text{RD}}$ output (BSC)	—	—	—
	PA15 I/O (port)	CK output (CPG)	—	—	—

Table 21.2 SH7084 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA0 I/O (port)	$\overline{\text{CS4}}$ output (BSC)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	$\overline{\text{CS5}}$ output (BSC)	TXD0 output (SCI)	—	—
	PA2 I/O (port)	A25 output (BSC)	DREQ0 input (DMAC)	IRQ0 input (INTC)	SCK0 I/O (SCI)
	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA6 I/O (port)	$\overline{\text{CS2}}$ output (BSC)	TCLKA input (MTU2)	—	—
	PA7 I/O (port)	$\overline{\text{CS3}}$ output (BSC)	TCLKB input (MTU2)	—	—

Bit	Bit Name	Initial Value	R/W	Description
14	PA3MD2	0	R/W	PA3 Mode
13	PA3MD1	0	R/W	Select the function of the PA3/A24/RXD1 pin.
12	PA3MD0	0	R/W	000: PA3 I/O (port) 001: RXD1 input (SCI) 101: A24 output (BSC)* Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PA2MD2	0	R/W	PA2 Mode
9	PA2MD1	0	R/W	Select the function of the PA2/A25/DREQ0/IRQ0/SCK0 pin.
8	PA2MD0	0	R/W	000: PA2 I/O (port) 001: SCK0 I/O (SCI) 010: DREQ0 input (DMAC) 011: IRQ0 input (INTC) 101: A25 output (BSC)* Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PA1MD2	0	R/W	PA1 Mode
5	PA1MD1	0	R/W	Select the function of the PA1/$\overline{\text{CS5}}$/$\overline{\text{CE1A}}$/TXD0 pin.
4	PA1MD0	0	R/W	000: PA1 I/O (port) 001: TXD0 output (SCI) 101: $\overline{\text{CS5}}$/$\overline{\text{CE1A}}$ output (BSC)* Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

(6) Inquiry on operating frequency

In response to the inquiry on operating frequency, the boot program returns the number of operating frequencies and the maximum and minimum values.

Command	H'23

— Command H'23 (1 byte): Inquiry on operating frequency

Response	H'33	Size	No. of operating clocks
	Operating freq. (min)		Operating freq. (max)
	…		
	SUM		

— Response H'33 (1 byte): Response to the inquiry on operating frequency

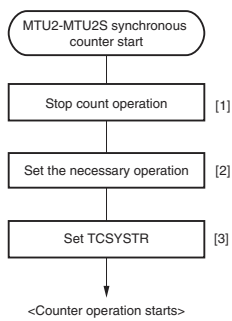
— Size (1 byte): The total length of the number of operating clocks, and maximum and minimum values of operating frequency fields.

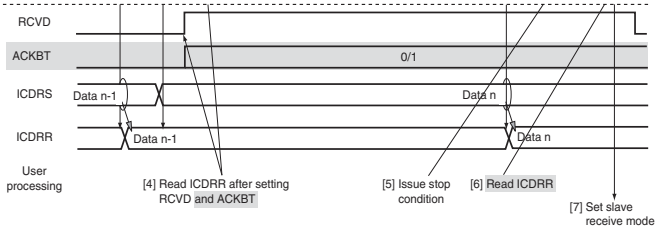
— Number of operating clocks (1 byte): The number of operating clock frequencies required within the device.
For example, the value two indicates main and peripheral operating clock frequencies.

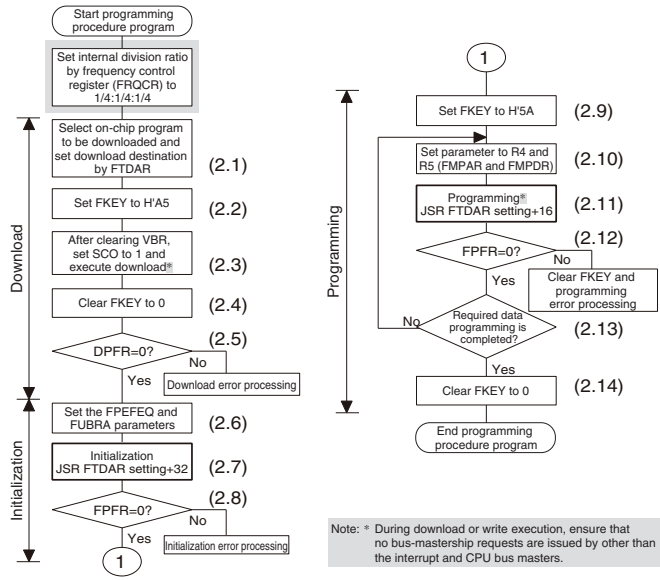
— Minimum value of operating frequency (2 bytes): The minimum frequency of a frequency-multiplied or -divided clock signal.
The value in this field and in the maximum value field is the frequency in MHz to two decimal places, multiplied by 100 (for example, if the frequency is 20.00 MHz, the value multiplied by 100 is 2000, so H'07D0 is returned here).

— Maximum value of operating frequency (2 bytes): The maximum frequency of a frequency-multiplied or -divided clock signal.
As many pairs of minimum/maximum values are included as there are operating clocks.

— SUM (1 byte): Checksum

Item	Page	Revision (See Manual for Details)
11.4.9 A/D Converter Start Request Delaying Function (e) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping	604	Description and note added In complementary PWM mode, A/D converter start requests (TRG4AN and TRG4BN) can be issued in coordination with interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR). ... The A/D converter start request delaying function linked to the interrupt skipping function cannot be used when not in complementary PWM mode. In this case, clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in TADCR to 0. Note: This function must be used in combination with interrupt skipping. ... Furthermore, when this function is to be used, set TADCORA_4 and TADCORB_4 to a value between H'0002 and the TCDR setting minus two.
11.4.10 MTU2–MTU2S Synchronous Operation (1) MTU2–MTU2S Synchronous Counter Start (a) Example of MTU2–MTU2S Synchronous Counter Start Setting Procedure Figure 11.83 Example of Synchronous Counter Start Setting Procedure	607	Figure amended  [1] Use TSTR registers in the MTU2 and MTU2S and halt the counters used for synchronous start operation. [2] Specify necessary operation with appropriate registers such as TCR and TMDR. [3] In TCSYSTR in the MTU2, set the bits corresponding to the counters to be started synchronously to 1. The TSTRs are automatically set appropriately and the counters start synchronously. Notes: 1. Even if a bit in TCSYSTR corresponding to an operating counter is cleared to 0, the counter will not stop. To stop the counter, clear the corresponding bits in TSTR and TSTRS to 0 directly. 2. To start channels 3 and 4 in reset-synchronized PWM mode or complementary PWM mode, make appropriate settings in TCYSTR according to the TSTR setting for the respective mode. For details, refer to section 11.4.7, Reset-Synchronized PWM Mode, and section 11.4.8, Complementary PWM Mode.
(b) Examples of Synchronous Counter Start Operation	608	Description amended In these examples, the count clock settings are MPϕ/1 (MTU2) and MIϕ/1 (MTU2S).

Item	Page	Revision (See Manual for Details)
18.4.3 Master Receive Operation Figure 18.9 Master Receive Mode Operation Timing (2)	946	Figure amended 
18.4.4 Slave Transmit Operation	947	Description amended 1. Initialize IIC2 (figure 18.7). After initialization, set the ICE bit in ICCR1 to 1. Set the MST and TRS bits in ICCR1 to select slave receive mode, and wait until the slave address matches. 2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise of the 9th clock pulse. At this time, if the 8th bit data (R/$\overline{W}$) is high, the TRS bit in ICCR1 and the TDRE bit in ICSR are set to 1, and the mode changes to slave transmit mode automatically. If the 8th bit of data is low-level, operation continues in slave receive mode. 3. Write the transmit data to ICDRT. At this time, TDRE is automatically cleared to 0, the data is transferred from ICDRT to ICDRS, and TDRE is set to 1 once again. Write the subsequent transmit data to ICDRT each time TDRE is set to 1. 4. Write the last transmit data to ICDRT, wait until TEND is set to 1 (final frame transmit-end). Alternately, wait for a NACK from the receive device (NACKF in ICSR = 1) with ACKE in ICIER set to 1. 5. Clear TRS for the end processing, and read ICDRR (dummy read). SCL is free. 6. Clear TDRE, TEND, and NACKF.

Item	Page	Revision (See Manual for Details)
23.2.6 Programming/ Erasing Interface (4) Programming/Erasing Execution	1250	Description amended The area to be programmed must be erased in advance when programming flash memory. Ensure that no interrupts, including NMI and IRQ, are generated during programming or erasure.
23.5.2 User Program Mode (2) Programming Procedure in User Program Mode Figure 23.11 Programming Procedure	1284	Figure amended 
	1286	Description amended In the download processing, the values of the general registers of the CPU are retained. During download processing, ensure that no bus-mastership requests are issued by other than the interrupt and CPU bus masters. For details, see section 23.8.2, Interrupts during Programming/Erasing. Since a stack area of maximum 128 bytes is used, an area of at least 128 bytes must be saved before setting the SCO bit to 1. (2.4) FKEY is cleared to H'00 for protection.