Renesas Electronics America Inc - DE70865RN80FPV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/de70865rn80fpv

4.4 Register Descriptions

The CPG has the following registers.

For details on the addresses of these registers and the states of these registers in each processing state, see section 27, List of Registers.

Table 4.5 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Frequency control register	FRQCR	R/W	H'36DB	H'FFFFE800	16
Oscillation stop detection control register	OSCCR	R/W	H'00	H'FFFFE814	8

4.4.1 Frequency Control Register (FRQCR)

FRQCR is a 16-bit readable/writable register that specifies the frequency division ratios for the internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), MTU2S clock (MIϕ), and MTU2 clock (MPϕ). FRQCR can be accessed only in words.

FRQCR is initialized to H'36DB only by a power-on reset (except a power-on reset due to a WDT overflow).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	IFC[2:0]			BFC[2:0]			PFC[2:0]			MIFC[2:0]			MPFC[2:0]		
Initial value:	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4.6.2 External Clock Input Method

Figure 4.4 shows an example of an external clock input connection. In this case, make the external clock high level to stop it when in software standby mode. During operation, make the external input clock frequency 5 to 12.5 MHz.

When leaving the XTAL pin open, make sure the parasitic capacitance is less than 10 pF.

Even when inputting an external clock, be sure to wait at least the oscillation stabilization time in power-on sequence or in releasing software standby mode, in order to ensure the PLL stabilization time.

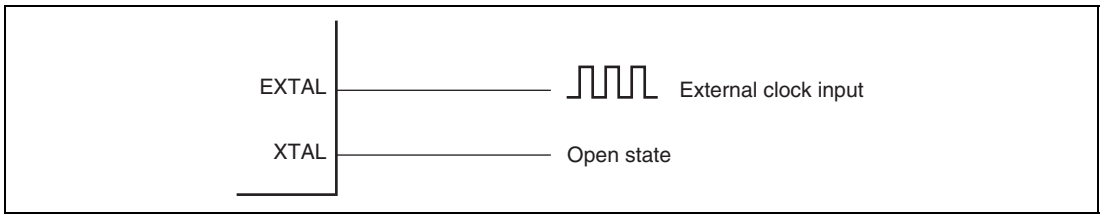


Figure 4.4 Example of External Clock Connection

Bit	Bit Name	Initial Value	R/W	Description
10	PCBA	0	R/W	PC Break Select A Selects the break timing of the instruction fetch cycle for channel A as before or after instruction execution. 0: PC break of channel A is set before instruction execution 1: PC break of channel A is set after instruction execution
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	DBEA	0	R/W	Data Break Enable A Selects whether or not the data bus condition is included in the break condition of channel A. 0: No data bus condition is included in the condition of channel A 1: The data bus condition is included in the condition of channel A
6	PCBB	0	R/W	PC Break Select B Selects the break timing of the instruction fetch cycle for channel B as before or after instruction execution. 0: PC break of channel B is set before instruction execution 1: PC break of channel B is set after instruction execution
5	DBEB	0	R/W	Data Break Enable B Selects whether or not the data bus condition is included in the break condition of channel B. 0: No data bus condition is included in the condition of channel B 1: The data bus condition is included in the condition of channel B
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

8.2.5 DTC Transfer Count Register A (CRA)

CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC.

In normal transfer mode, CRA functions as a 16-bit transfer counter (1 to 65,536). It is decremented by 1 every time data is transferred, and bit DTCEn (n = 15 to 0) corresponding to the activation source is cleared and then an interrupt is requested to the CPU when the count reaches H'0000. The transfer count is 1 when CRA = H'0001, 65,535 when CRA = H'FFFF, and 65,536 when CRA = H'0000.

In repeat transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent to CRAL when the count reaches H'00. The transfer count is 1 when CRAH = CRAL = H'01, 255 when CRAH = CRAL = H'FF, and 256 when CRAH = CRAL = H'00.

In block transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the block size while CRAL functions as an 8-bit block-size counter (1 to 256 for byte, word, or longword). CRAL is decremented by 1 every time a byte (word or longword) data is transferred, and the contents of CRAH are sent to CRAL when the count reaches H'00. The block size is 1 byte (word or longword) when CRAH = CRAL =H'01, 255 bytes (words or longwords) when CRAH = CRAL = H'FF, and 256 bytes (words or longwords) when CRAH = CRAL =H'00.

CRA cannot be accessed directly from the CPU.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

*: Undefined

3. For the second transfer, set repeat transfer mode (with the source side as the repeat area) for re-setting the transfer destination address for the first data transfer. Use the upper eight bits of DAR in the first transfer information area as the transfer destination. Set CHNE = DISEL = 0. If the above input buffer is specified as H'200000 to H'21FFFF, set the transfer counter to 2.
4. Execute the first data transfer 65536 times by means of interrupts. When the transfer counter for the first data transfer reaches 0, the second data transfer is started. Set the upper eight bits of the transfer destination address for the first data transfer to H'21. The lower 16 bits of the transfer destination address of the first data transfer and the transfer counter are H'0000.
5. Next, execute the first data transfer the 65536 times specified for the first data transfer by means of interrupts. When the transfer counter for the first data transfer reaches 0, the second data transfer is started. Set the upper eight bits of the transfer destination address for the first data transfer to H'20. The lower 16 bits of the transfer destination address of the first data transfer and the transfer counter are H'0000.
6. Steps 4 and 5 are repeated endlessly. As repeat mode is specified for the second data transfer, no interrupt request is sent to the CPU.

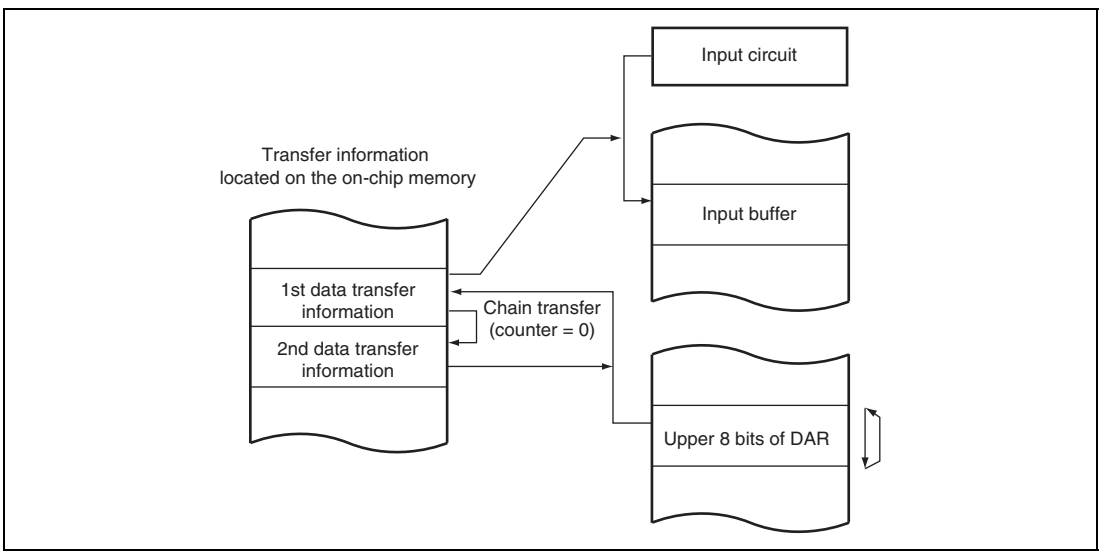


Figure 8.19 Chain Transfer when Counter = 0

9.4.8 Bus Function Extending Register (BSCEHR)

BSCEHR is a 16-bit register that specifies the timing of bus release by the DTC and DMAC. It also specifies the application of priority in transfer operations and enables or disables the functions that have the effect of decreasing numbers of cycles over which the DTC is active. The differences in DTC operation made by the combinations of the DTLOCK, CSSTP1, and DTBST bits settings are described in section 8.5.9, DTC Bus Releasing Timing.

Setting the CSSTP2 bit can improve the transfer performance of the DMAC in burst-mode transfer and of the DTC when the DTLOCK bit is 0.

Furthermore, setting the CSSTP3 bit selects whether or not access to the external space by the CPU takes priority over DTC or DMAC transfer in cycle-steal mode. The DTC short address mode is implemented by setting the DTSA bit. For details of the short address mode, see section 8.4, Location of Transfer Information and DTC Vector Table.

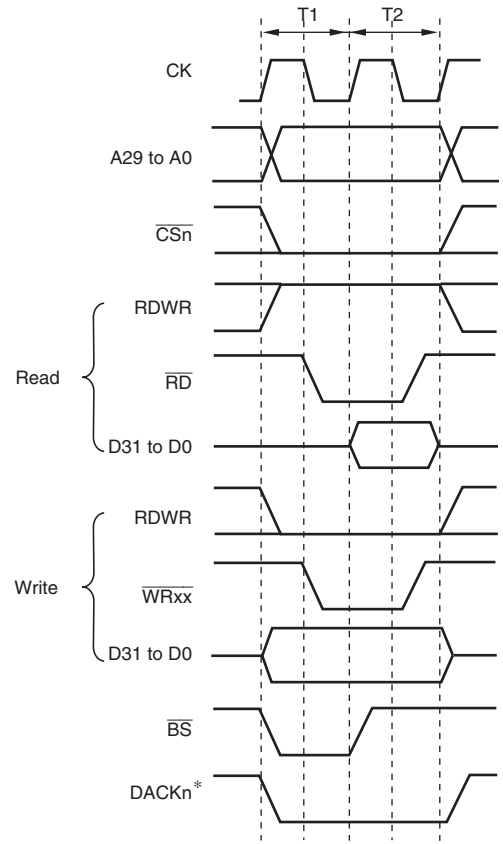
A DTC activation priority order can be set up for the DTC activation sources. The DTPR bit selects whether or not this priority order is valid or invalid when multiple sources issue activation requests before DTC activation. The corresponding bit from among DMMTU4 to DMMTU0 must be set for MTU2-triggered transfer by the DMAC in the burst mode. Do not modify this register while the DMAC or DTC is active.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTLOCK	CSSTP1	-	CSSTP2	DTBST	DTSA	CSSTP3	DTPR	-	-	-	DMMTU4	DMMTU3	DMMTU2	DMMTU1	DMMTU0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	DTLOCK	0	R/W	DTC Lock Enable Specifies the timing of bus release by the DTC. 0: The DTC releases the bus on generation of the NOP cycle that follows vector read or write-back of transfer information. 1: The DTC releases the bus after vector read, on generation of the NOP cycle that follows vector read, after transfer information read, after a round of data transfer, or after write-back of transfer information.

9.5.2 Normal Space Interface

Basic Timing: For access to a normal space, this LSI uses strobe signal output in consideration of the fact that mainly SRAM without a byte selection will be directly connected. When using SRAM with a byte-selection pin, see section 9.5.8, SRAM Interface with Byte Selection. Figure 9.2 shows the basic timings of normal space access. A no-wait normal access is completed in two cycles. The $\overline{BS}$ signal is asserted for one cycle to indicate the start of a bus cycle.

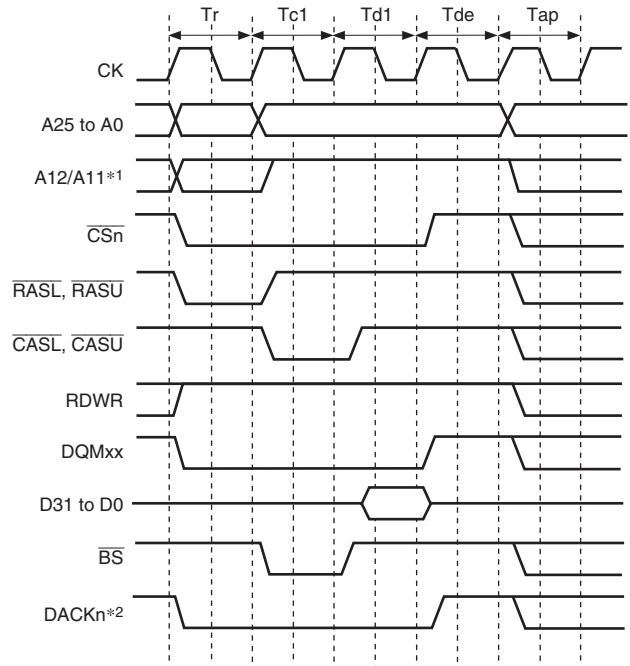


Note: * The waveform for DACKn is when active low is specified.

Figure 9.2 Normal Space Basic Access Timing (Access Wait 0)

Single Read: A read access ends in one cycle when the data bus width is larger than or equal to access size. This is called single read. As the burst length is set to 1 in SDRAM burst read/single write mode, only the required data is output. Consequently, no unnecessary bus cycles are generated.

Figure 9.20 shows the single read basic timing.



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.20 Single Read Basic Timing (Auto-Precharge)

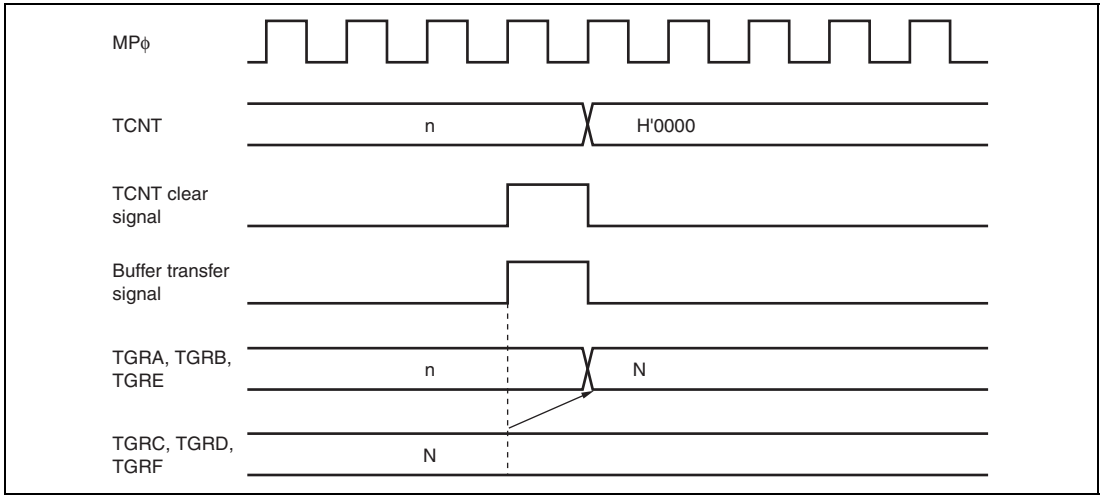


Figure 11.105 Buffer Transfer Timing (when TCNT Cleared)

(6) Buffer Transfer Timing (Complementary PWM Mode)

Figures 11.106 to 11.108 show the buffer transfer timing in complementary PWM mode.

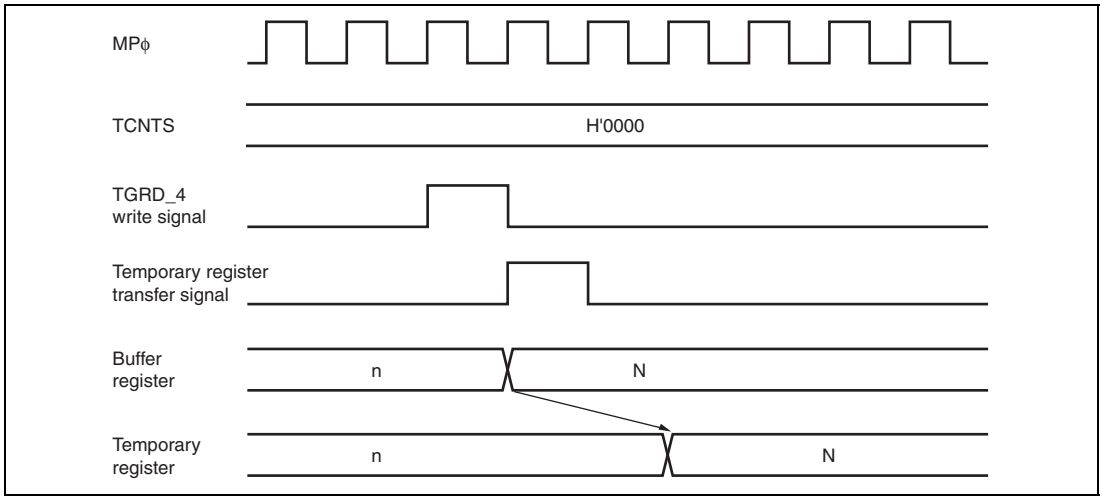


Figure 11.106 Transfer Timing from Buffer Register to Temporary Register (TCNTS Stop)

16.2 Input/Output Pins

The SCIF has the serial pins summarized in table 16.1.

Table 16.1 Pin Configuration

Channel	Pin Name	Abbreviation	I/O	Function
3	Serial clock pin	SCK3	I/O	Clock I/O
	Receive data pin	RXD3	Input	Receive data input
	Transmit data pin	TXD3	Output	Transmit data output
	Request to send pin	$\overline{\text{RTS3}}$	Output	Request to send
	Clear to send pin	$\overline{\text{CTS3}}$	Input	Clear to send

Note: In the following descriptions in this section, the channel number in the abbreviated pin names is omitted as in SCK, RXD, TXD, $\overline{\text{RTS}}$, and $\overline{\text{CTS}}$.

16.3.7 Serial Status Register (SCFSR)

SCFSR is a 16-bit register. The upper 8 bits indicate the number of receives errors in the SCFRDR data, and the lower 8 bits indicate the status flag indicating SCIF operating state.

The CPU can always read and write to SCFSR, but cannot write 1 to the status flags (ER, TEND, TDFE, BRK, RDF, and DR). These flags can be cleared to 0 only if they have first been read (after being set to 1). Bits 3 (FER) and 2 (PER) are read-only bits that cannot be written.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PER[3:0]				FER[3:0]				ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Note: * To clear the flag, only 0 can be written after reading 1.

Bit	Bit Name	Initial value	R/W	Description
15 to 12	PER[3:0]	0000	R	Number of Parity Errors Indicate the number of data including a parity error in the receive data stored in the receive FIFO data register (SCFRDR). After the ER bit in SCFSR is set to 1, the value indicated by bits 15 to 12 indicates the number of parity errors in SCFRDR. When parity errors have occurred in all 16-byte receive data in SCFRDR, PER3 to PER0 show 0.
11 to 8	FER[3:0]	0000	R	Number of Framing Errors Indicate the number of data including a framing error in the receive data stored in SCFRDR. After the ER bit in SCFSR is set to 1, the value indicated by bits 11 to 8 indicates the number of framing errors in SCFRDR. When framing errors have occurred in all 16-byte receive data in SCFRDR, FER3 to FER0 show 0.

(3) Transmitting and Receiving Data

SCIF Initialization (Asynchronous Mode):

Before transmitting or receiving, clear the TE and RE bits to 0 in the serial control register (SCSCR), then initialize the SCIF as follows.

When changing the operation mode or the communication format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 initializes the transmit shift register (SCTSR). Clearing TE and RE to 0, however, does not initialize the serial status register (SCFSR), transmit FIFO data register (SCFTDR), or receive FIFO data register (SCFRDR), which retain their previous contents. Clear TE to 0 after all transmit data has been transmitted and the TEND flag in the SCFSR is set. The TE bit can be cleared to 0 during transmission, but the transmit data goes to the Mark state after the bit is cleared to 0. Set the TFRST bit in SCFCR to 1 and reset SCFTDR before TE is set again to start transmission.

When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCIF operation becomes unreliable if the clock is stopped.

18.3.5 I²C Bus Status Register (ICSR)

ICSR is an 8-bit readable/writable register that confirms interrupt request flags and their status.

ICSR is initialized to H'00 by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	TDRE	TEND	RDRF	NACKF	STOP	AL/OVE	AAS	ADZ
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * These flags can be cleared only by writing 0 after reading the flag's value as 1.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	0	R/(W)*[1]	Transmit Data Register Empty [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When data is written to ICDRT • DTC is activated by IITXI interrupt and the DISEL bit in MRB of DTC is 0. [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When TRS is set • When the start condition (including retransmission) is issued • When slave mode is changed from receive mode to transmit mode

18.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. For slave receive mode operation timing, refer to figures 18.12 and 18.13.

The reception procedure and operations in slave receive mode are described below. For operation up to reception of the 1st frame (slave address + R/$\overline{W}$), see 18.4.4, Slave Transmit Operation.

1. Perform a dummy read of ICDRR. (The read data indicates slave address + R/$\overline{W}$, and is therefore unnecessary.) The slave device outputs to SDA the level indicated by the setting of ACKBT in ICIER at the 9th clock pulse of the receive clock.
2. After reception of one frame of data finishes, RDRF in ICSR is set to 1 at the rising edge of the 9th receive clock pulse. At this time, the received data can be read by reading ICDRR, and RDRF is cleared to 0 simultaneously. Continuous receive operation can be accomplished by reading ICDRR each time RDRF is set to 1.
   If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read.
3. If the next receive operation is the final frame, set ACKBT in ICIER to 1 before reading ICDRR.
4. When RDRF in ICSR is set to 1, read the final receive data from ICDRR.

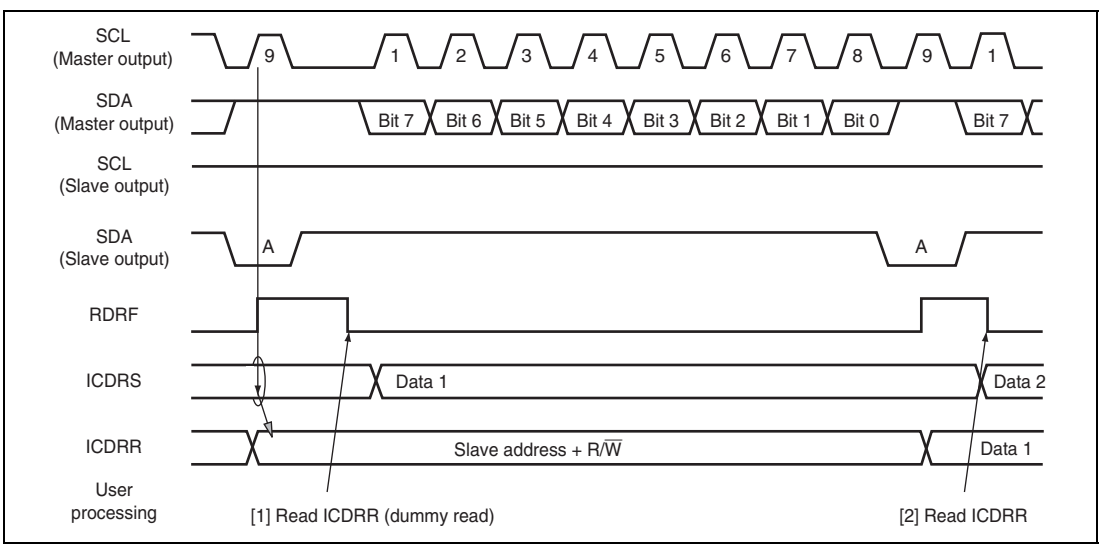


Figure 18.12 Slave Receive Mode Operation Timing (1)

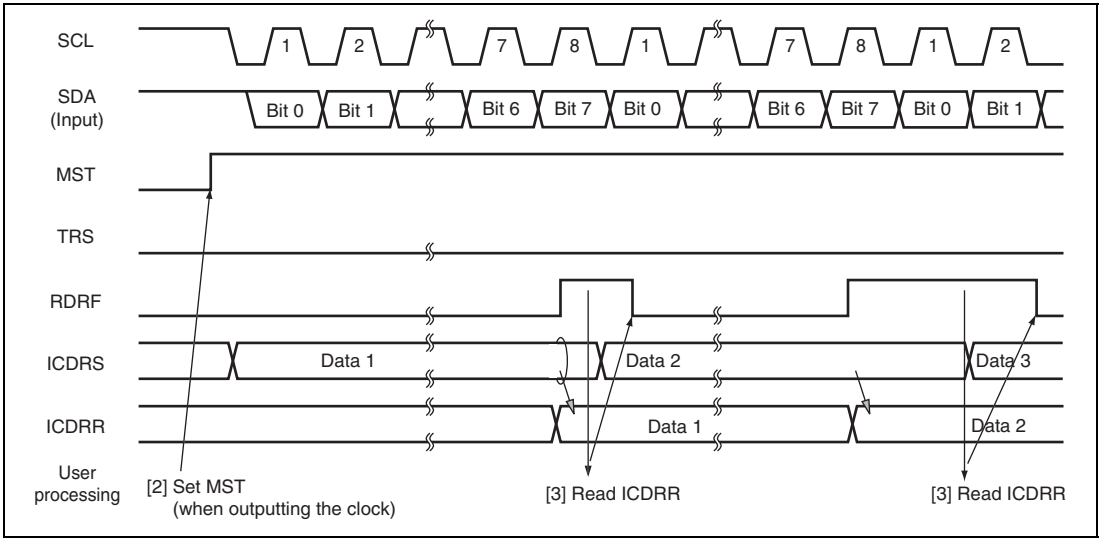


Figure 18.16 Receive Mode Operation Timing (LSB-First Operation)

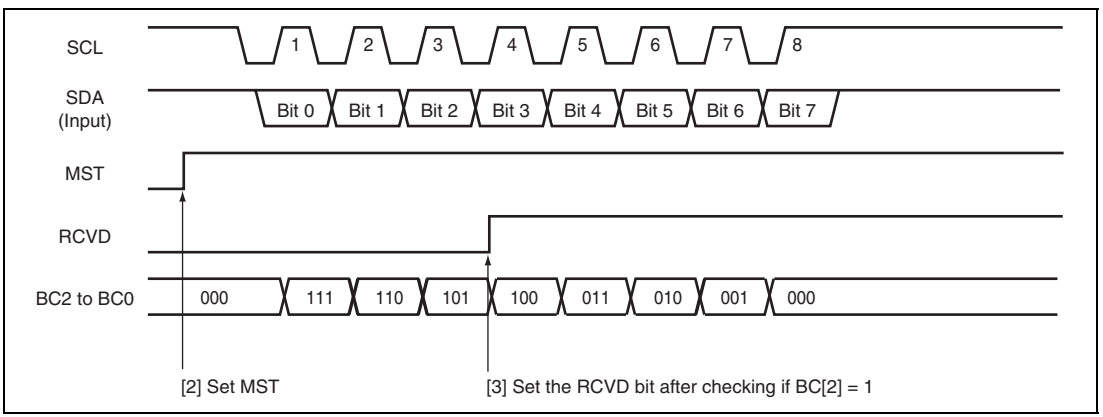


Figure 18.17 Operation Timing For Receiving One Byte (LSB-First Operation)

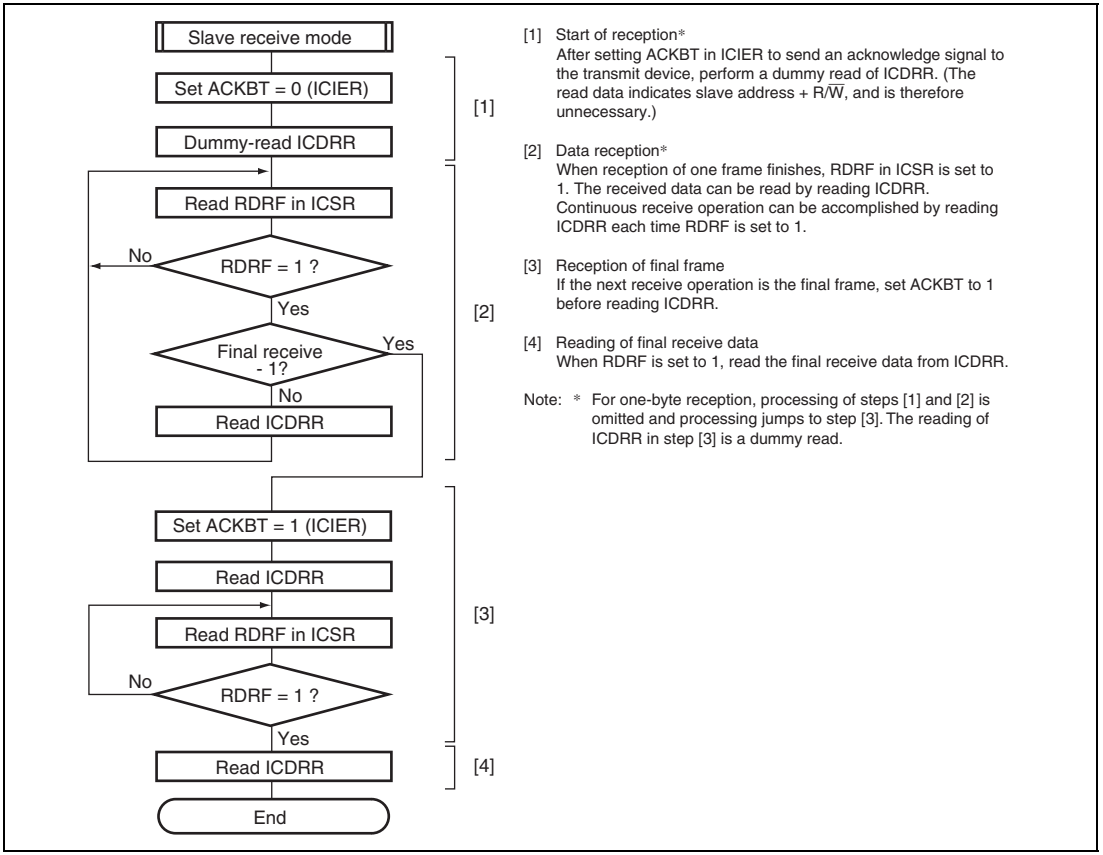


Figure 18.23 Sample Flowchart for Slave Receive Mode

- PEPRH (SH7086)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PE21PR	PE20PR	PE19PR	PE18PR	PE17PR	PE16PR
Initial value:	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PE21PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
4	PE20PR	Pin state	R	
3	PE19PR	Pin state	R	
2	PE18PR	Pin state	R	
1	PE17PR	Pin state	R	
0	PE16PR	Pin state	R	

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
I²C bus control register 1	ICCR1	8	H'FFFFCD80	IIC2	8	Pϕ reference	8 bits
I²C bus control register 2	ICCR2	8	H'FFFFCD81		8	B:2	
I²C bus mode register	ICMR	8	H'FFFFCD82		8		
I²C bus interrupt enable register	ICIER	8	H'FFFFCD83		8		
I²C bus status register	ICSR	8	H'FFFFCD84		8		
Slave address register	SAR	8	H'FFFFCD85		8		
I²C bus transmit data register	ICDRT	8	H'FFFFCD86		8		
I²C bus receive data register	ICDRR	8	H'FFFFCD87		8		
NF2CYC register	NF2CYC	8	H'FFFFCD88		8		
SS control register H	SSCRH	8	H'FFFFCD00	SSU	8, 16	Pϕ reference	16 bits
SS control register L	SSCRL	8	H'FFFFCD01		8	B:2	
SS mode register	SSMR	8	H'FFFFCD02		8, 16	W:2	
SS enable register	SSER	8	H'FFFFCD03		8		
SS status register	SSSR	8	H'FFFFCD04		8, 16		
SS control register 2	SSCR2	8	H'FFFFCD05		8		
SS transmit data register 0	SSTDR0	8	H'FFFFCD06		8, 16		
SS transmit data register 1	SSTDR1	8	H'FFFFCD07		8		
SS transmit data register 2	SSTDR2	8	H'FFFFCD08		8, 16		
SS transmit data register 3	SSTDR3	8	H'FFFFCD09		8		
SS receive data register 0	SSRDR0	8	H'FFFFCD0A		8, 16		
SS receive data register 1	SSRDR1	8	H'FFFFCD0B		8		
SS receive data register 2	SSRDR2	8	H'FFFFCD0C		8, 16		
SS receive data register 3	SSRDR3	8	H'FFFFCD0D		8		
Compare match timer start register	CMSTR	16	H'FFFFCE00	CMT	8, 16, 32	Pϕ reference	16 bits
Compare match timer control/status register_0	CMCSR_0	16	H'FFFFCE02		8, 16	B:2 W:2	
Compare match counter_0	CMCNT_0	16	H'FFFFCE04		8, 16, 32	L:4	
Compare match constant register_0	CMCOR_0	16	H'FFFFCE06		8, 16		
Compare match timer control/status register_1	CMCSR_1	16	H'FFFFCE08		8, 16, 32		
Compare match counter_1	CMCNT_1	16	H'FFFFCE0A		8, 16		
Compare match constant register_1	CMCOR_1	16	H'FFFFCE0C		8, 16, 32		

27.2 Register Bit List

Addresses and bit names of each on-chip peripheral module are shown below.

As for 16-bit or 32-bit registers, they are shown in two or four rows.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
SCSMR_0	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS[1:0]		SCI
SCBRR_0									(Channel 0)
SCSCR_0	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_0									
SCSSR_0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_0									
SCSDCR_0	—	—	—	—	DIR	—	—	—	
SCSPTR_0	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	
SCSMR_1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS[1:0]		SCI
SCBRR_1									(Channel 1)
SCSCR_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_1									
SCSSR_1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_1									
SCSDCR_1	—	—	—	—	DIR	—	—	—	
SCSPTR_1	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	
SCSMR_2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS[1:0]		SCI
SCBRR_2									(Channel 2)
SCSCR_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_2									
SCSSR_2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_2									
SCSDCR_2	—	—	—	—	DIR	—	—	—	
SCSPTR_2	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	

Table A.3 Pin States (SH7085)

Pin Function		Pin State										
		Reset State					Power-Down State					
		Power-On										
Type	Pin Name	Expansion without ROM 16 bits	Expansion without ROM 32 bits	Expansion with ROM	Single-chip	Manual	Deep Software Standby	Software Standby	Sleep	Bus Mastership Release	Oscillation Stop Detected	POE Function Used
Clock	CK	O			Z	O	Z	H*1	O	O	O	O
	XTAL	O				O	L	L	O	O	O	O
	EXTAL	I				I	Z	I	I	I	I	I
System control	$\overline{\text{RES}}$	I				I	I	I	I	I	I	I
	$\overline{\text{MRES}}$	Z				I	Z	I*6	I	I	I*6	I
	$\overline{\text{WDTOVF}}$	O*7				O	O	O	O	O	O	O
	$\overline{\text{BREQ}}$	Z				I	Z	Z	I	I	I	I
	$\overline{\text{BACK}}$	Z				O	Z	Z	O	L	O	O
Operating mode control	MD0, MD1	I				I	I	I	I	I	I	I
	$\overline{\text{ASEMD0}}$	I*8				I*8	I*8	I*8	I*8	I*8	I*8	I*8
	FWE	I				I	I	I	I	I	I	I
Interrupt	NMI	I				I	I	I	I	I	I	I
	IRQ0 to IRQ7	Z				I	Z	I	I	I	I	I
	$\overline{\text{IRQOUT}}$ (PE15)	Z				O	Z	Z (MZIZEL in HCPCR = 0) H*1 (MZIZEL in HCPCR = 1)	O	O	O*6	O
	$\overline{\text{IRQOUT}}$ (PD30)	Z				O	Z	H*1	O	O	O	O
Address bus	A0 to A17	O		Z		O	Z	Z*3	O	Z	O	O
	A18 to A25	Z				O	Z	Z*3	O	Z	O	O
Data bus	D0 to D8, D10, D16 to D23, D30, D31	Z				I/O	Z	Z	I/O	Z	I/O	I/O
	D9, D11 to D15	Z				I/O	Z	Z	I/O	Z	I/O*5	I/O
	D24 to D29	Z				I/O	Z	Z	I/O	Z	I/O*4	I/O