Renesas Electronics America Inc - DF70834AD80BGV Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70834ad80bgv

1.4 Pin Functions

Table 1.2 summarizes the pin functions.

Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pins. Connect all Vcc pins to the system. There will be no operation if any pins are open.
	Vss	I	Ground	Ground pin. Connect all Vss pins to the system power supply (0V). There will be no operation if any pins are open.
	VCL	O	Power supply for internal power-down	External capacitance pins for internal power-down power supply. Connect these pins to Vss via a 0.47 μF capacitor (placed close to the pins).
Clock	PLLVss	I	PLL ground	Ground pin for the on-chip PLL oscillator
	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
	CK	O	System clock	Supplies the system clock to external devices.
Operating mode control	MD1, MD0	I	Mode set	Sets the operating mode. Do not change values on these pins during operation.
	FWE	I	Flash memory write enable	Pin for flash memory. Flash memory can be protected against programming or erasure through this pin.

PLL Multiplication Ratio	FRQCR Division Ratio Setting					Clock Ratio					Clock Frequency (MHz)*					
	Iφ	Bφ	Pφ	MIφ	MPφ	Iφ	Bφ	Pφ	MIφ	MPφ	Input Clock	Iφ	Bφ	Pφ	MIφ	MPφ
×8	1/1	1/2	1/4	1/2	1/2	8	4	2	4	4	10	80	40	20	40	40
	1/1	1/2	1/4	1/1	1/4	8	4	2	8	2		80	40	20	80	20
	1/1	1/2	1/4	1/1	1/2	8	4	2	8	4		80	40	20	80	40
	1/1	1/2	1/2	1/2	1/2	8	4	4	4	4		80	40	40	40	40
	1/1	1/2	1/2	1/1	1/2	8	4	4	8	4		80	40	40	80	40
	1/1	1/1	1/4	1/4	1/4	8	8	2	2	2	5	40	40	10	10	10
	1/1	1/1	1/4	1/2	1/4	8	8	2	4	2		40	40	10	20	10
	1/1	1/1	1/4	1/2	1/2	8	8	2	4	4		40	40	10	20	20
	1/1	1/1	1/4	1/1	1/4	8	8	2	8	2		40	40	10	40	10
	1/1	1/1	1/4	1/1	1/2	8	8	2	8	4		40	40	10	40	20
	1/1	1/1	1/4	1/1	1/1	8	8	2	8	8		40	40	10	40	40
	1/1	1/1	1/3	1/3	1/3	8	8	8/3	8/3	8/3		40	40	13	13	13
	1/1	1/1	1/3	1/1	1/3	8	8	8/3	8	8/3		40	40	13	40	13
	1/1	1/1	1/3	1/1	1/1	8	8	8/3	8	8		40	40	13	40	40
	1/1	1/1	1/2	1/2	1/2	8	8	4	4	4		40	40	20	20	20
	1/1	1/1	1/2	1/1	1/2	8	8	4	8	4		40	40	20	40	20
	1/1	1/1	1/2	1/1	1/1	8	8	4	8	8		40	40	20	40	40
	1/1	1/1	1/1	1/1	1/1	8	8	8	8	8		40	40	40	40	40

5.5.3 Illegal Slot Instructions

An instruction placed immediately after a delayed branch instruction is called "instruction placed in a delay slot". When the instruction placed in the delay slot is an undefined code, illegal slot exception handling starts after the undefined code is decoded. Illegal slot exception handling also starts when an instruction that changes the program counter (PC) value is placed in a delay slot and the instruction is decoded. The CPU handles an illegal slot instruction as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the target address of the delayed branch instruction immediately before the undefined code or the instruction that rewrites the PC.
3. The start address of the exception handling routine is fetched from the exception handling vector table that corresponds to the exception that occurred. Program execution branches to that address and the program starts. This branch is not a delayed branch.

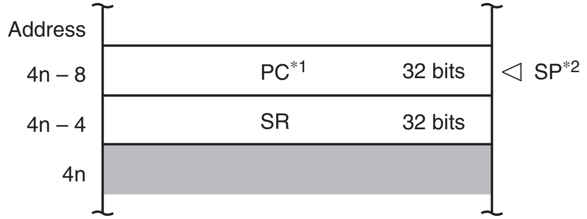
5.5.4 General Illegal Instructions

When an undefined code placed anywhere other than immediately after a delayed branch instruction (i.e., in a delay slot) is decoded, general illegal instruction exception handling starts. The CPU handles the general illegal instructions in the same procedures as in the illegal slot instructions. Unlike processing of illegal slot instructions, however, the program counter value that is stacked is the start address of the undefined code.

		Initial		
Bit	**Bit Name**	**Value**	**R/W**	**Description**
4	IRQ4F	0	R/W	Indicates the status of an IRQ4 interrupt request. • When level detection mode is selected 0: An IRQ4 interrupt has not been detected [Clearing condition] Driving pin IRQ4 high 1: An IRQ4 interrupt has been detected [Setting condition] Driving pin IRQ4 low • When edge detection mode is selected 0: An IRQ4 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ4F = 1 — Accepting an IRQ4 interrupt 1: An IRQ4 interrupt request has been detected [Setting condition] Detecting the specified edge of pin IRQ4
3	IRQ3F	0	R/W	Indicates the status of an IRQ3 interrupt request. • When level detection mode is selected 0: An IRQ3 interrupt has not been detected [Clearing condition] Driving pin IRQ3 high 1: An IRQ3 interrupt has been detected [Setting condition] Driving pin IRQ3 low • When edge detection mode is selected 0: An IRQ3 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ3F = 1 — Accepting an IRQ3 interrupt 1: An IRQ3 interrupt request has been detected [Setting condition] Detecting the specified edge of pin IRQ3

6.6.2 Stack after Interrupt Exception Handling

Figure 6.4 shows the stack after interrupt exception handling.



Notes: 1. PC is the start address of the next instruction (instruction at the return address) after the executed instruction.
2. Always make sure that SP is a multiple of 4

Figure 6.4 Stack after Interrupt Exception Handling

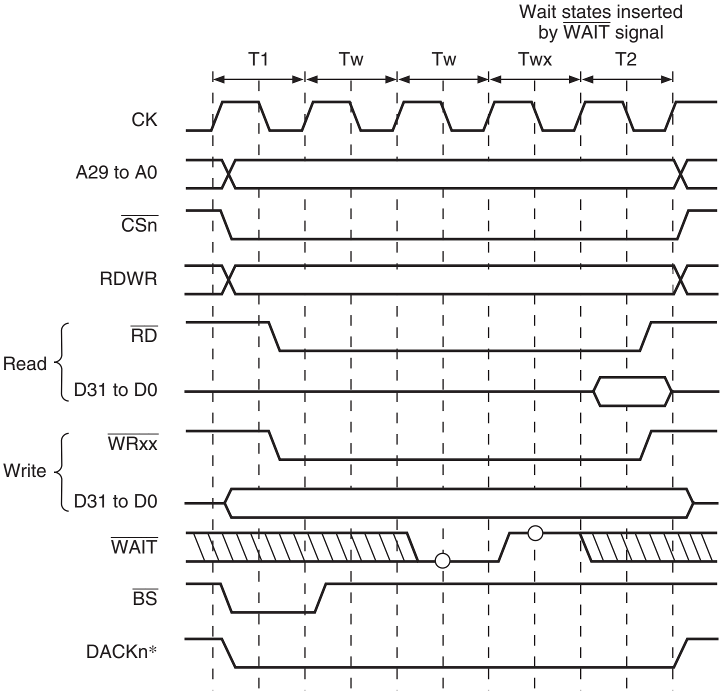
6.7 Interrupt Response Time

Table 6.4 lists the interrupt response time, which is the time from the occurrence of an interrupt request until the interrupt exception handling starts and fetching of the first instruction of the interrupt handling routine begins.

Bit	Bit Name	Initial Value	R/W	Description
2, 1	—	All 0	R	Reserved These are read-only bits and cannot be modified.
0	ERR	0	R/(W)*	Transfer Stop Flag Indicates that the DTC address error or NMI interrupt request has occurred. If a DTC address error or NMI interrupt occurs while the DTC is active, address error handling or NMI interrupt handling processing is executed after the DTC has released the bus mastership. The DTC stops in the transfer information writing state after transferring data. 0: No interrupt occurs 1: An interrupt occurs [Clearing condition] • When writing 0 after reading 1

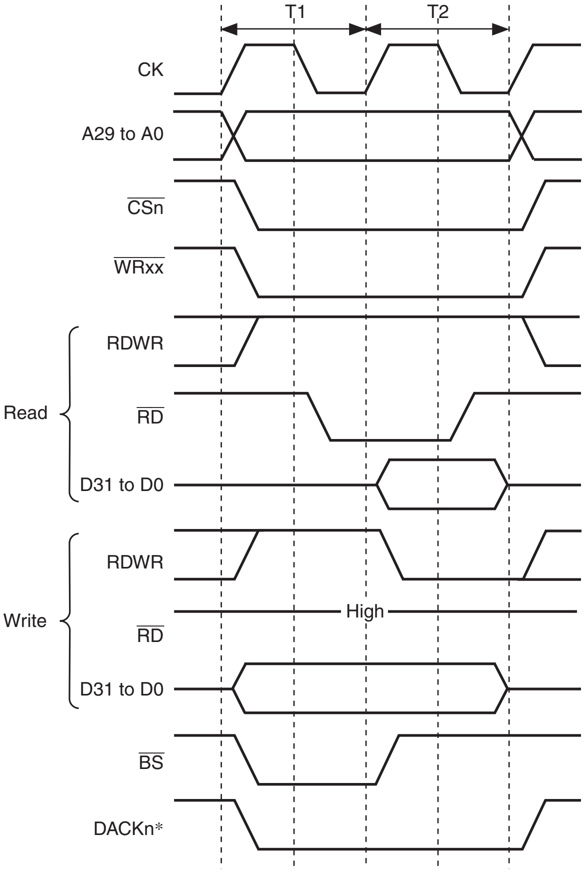
Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

When the WM bit in CSnWCR is cleared to 0, the external wait input $\overline{\text{WAIT}}$ signal is also sampled. $\overline{\text{WAIT}}$ pin sampling is shown in figure 9.9. A 2-cycle wait is specified as a software wait. The $\overline{\text{WAIT}}$ signal is sampled at the falling edge of CK at the transition from the T1 or Tw cycle to the T2 cycle.



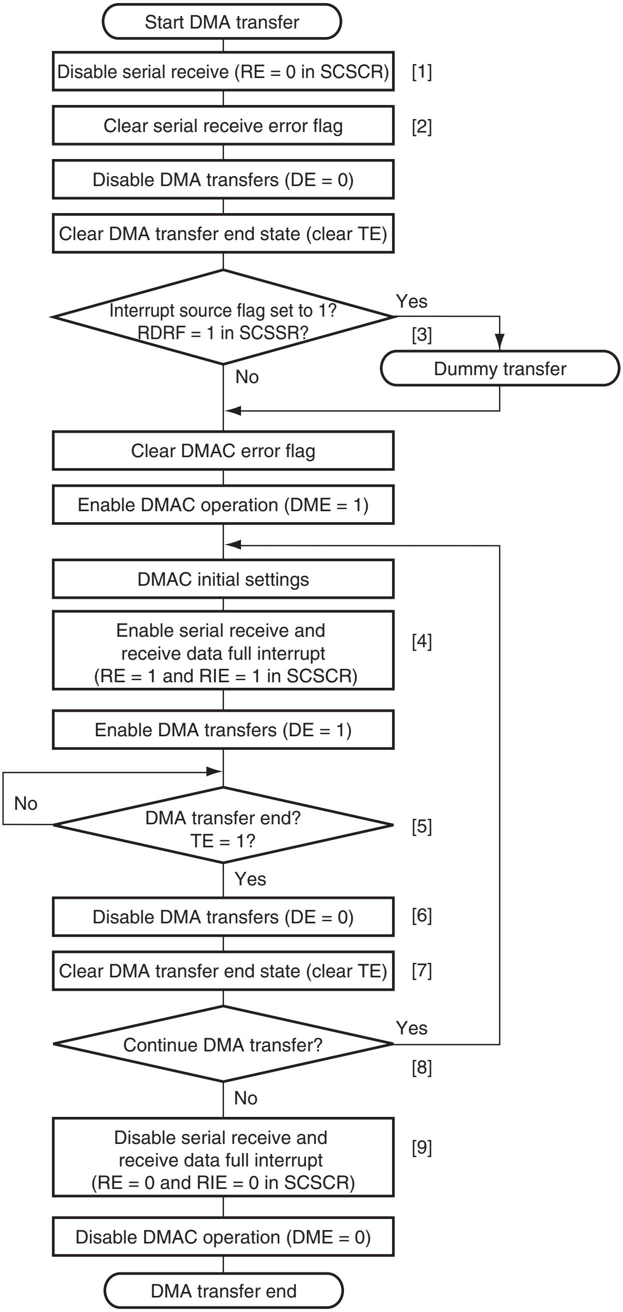
Note: * The waveform for DACKn is when active low is specified.

Figure 9.9 Wait State Timing for Normal Space Access (Wait State Insertion Using $\overline{\text{WAIT}}$ Signal)



Note: * The waveform for DACKn is when active low is specified.

Figure 9.34 Basic Access Timing for SRAM with Byte Selection (BAS = 1)


Start DMA transfer
Disable serial receive (RE = 0 in SCSCR)
[1]
Clear serial receive error flag
[2]
Disable DMA transfers (DE = 0)
Clear DMA transfer end state (clear TE)
Interrupt source flag set to 1?
RDRF = 1 in SCSSR?
Yes
[3]
Dummy transfer
No
Clear DMAC error flag
Enable DMAC operation (DME = 1)
DMAC initial settings
Enable serial receive and
receive data full interrupt
(RE = 1 and RIE = 1 in SCSCR)
[4]
Enable DMA transfers (DE = 1)
No
DMA transfer end?
TE = 1?
[5]
Yes
Disable DMA transfers (DE = 0)
[6]
Clear DMA transfer end state (clear TE)
[7]
Continue DMA transfer?
Yes
[8]
No
Disable serial receive and
receive data full interrupt
(RE = 0 and RIE = 0 in SCSCR)
[9]
Disable DMAC operation (DME = 0)
DMA transfer end

[1] [1] Disable serial receive so no interrupt (RXI) occurs during the transfer sequence.

[2] Clear the serial receive error flag. At this point, do not clear the interrupt source flag (RDRF in SCSSR).

[3] If the interrupt source flag has been set to 1, perform a dummy transfer to clear it.

[4] After enabling serial receive and the receive data full interrupt (RE = 1 and RIE = 1 in SCSCR), enable DMA transfers (DE = 1).

[5] Wait for the DMA transfer to end. If the DEI interrupt is enabled (IE = 1), a DEI interrupt will be generated when the DMA transfer ends.

[6] Disable DMA transfers (DE = 0).

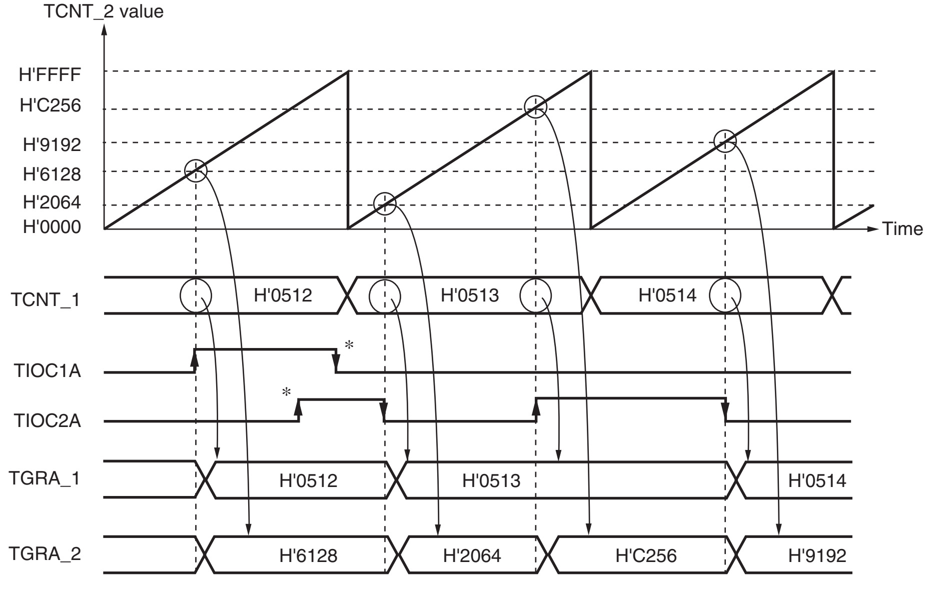
[7] Clear the DMA transfer end state (clear TE).

[8] To continue DMA transfer operation, reset the DMAC. No dummy transfer is needed in this case.

[9] Disable the receive data full interrupt (RIE = 0 in SCSCR) to disable interrupt requests.

Figure 10.22 Example DMA Transfer Sequence in Peripheral Module Request Mode (RXI)

Cascaded Operation Example (c): Figure 11.23 illustrates the operation when TCNT_1 and TCNT_2 have been cascaded and the I2AE and I1AE bits in TICCR have been set to 1 to include the TIOC2A and TIOC1A pins in the TGRA_1 and TGRA_2 input capture conditions, respectively. In this example, the IOA[3:0] bits in both TIOR_1 and TIOR_2 have selected both the rising and falling edges for the input capture timing. Under these conditions, the ORed result of TIOC1A and TIOC2A input is used for the TGRA_1 and TGRA_2 input capture conditions.



Note: * When either of the input pins is at the high level, an edge on the other input pin does not act as an input capture condition.

Figure 11.23 Cascaded Operation Example (c)

Cascaded Operation Example (d): Figure 11.24 illustrates the operation when TCNT_1 and TCNT_2 have been cascaded and the I2AE bit in TICCR has been set to 1 to include the TIOC2A pin in the TGRA_1 input capture conditions. In this example, the IOA[3:0] bits in TIOR_1 have selected TGRA_0 compare match or input capture occurrence for the input capture timing while the IOA[3:0] bits in TIOR_2 have selected the TIOC2A rising edge for the input capture timing.

Under these conditions, as TIOR_1 has selected TGRA_0 compare match or input capture occurrence for the input capture timing, the TIOC2A edge is not used for TGRA_1 input capture condition although the I2AE bit in TICCR has been set to 1.

Pin initialization procedures are described below for the numbered combinations in table 11.59. The active level is assumed to be low.

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Normal Mode: Figure 11.141 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in normal mode after re-setting.

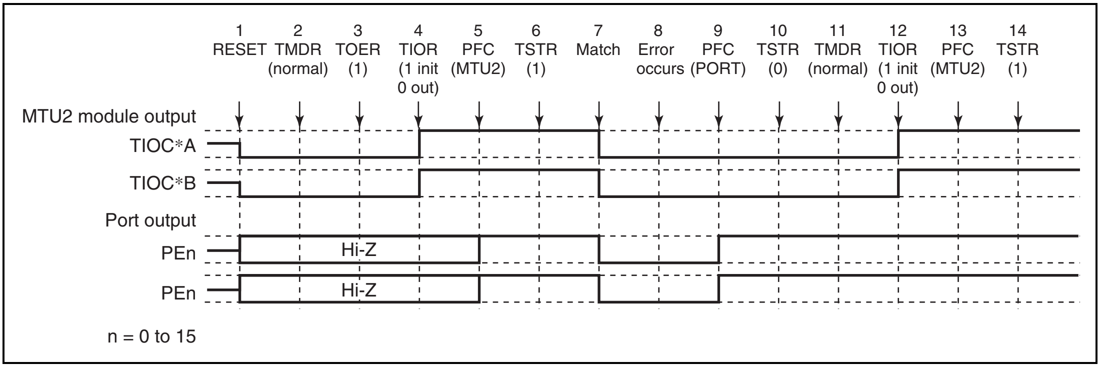


Figure 11.141 Error Occurrence in Normal Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. After a reset, the TMDR setting is for normal mode.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Not necessary when restarting in normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Table 16.3 SCSMR Settings

		SCSMR Settings	
n	Clock Source	CKS1	CKS0
0	Pϕ	0	0
1	Pϕ/4	0	1
2	Pϕ/16	1	0
3	Pϕ/64	1	1

Note: The bit rate error in asynchronous is given by the following formula:

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

18.4.7 Noise Filter

The logic levels at the SCL and SDA pins are routed through noise filters before being latched internally. Figure 18.18 shows a block diagram of the noise filter circuit.

The noise filter consists of three cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on the peripheral clock. When NF2CYC is set to 0, this signal is not passed forward to the next circuit unless the outputs of both latches agree. When NF2CYC is set to 1, this signal is not passed forward to the next circuit unless the outputs of three latches agree. If they do not agree, the previous value is held.

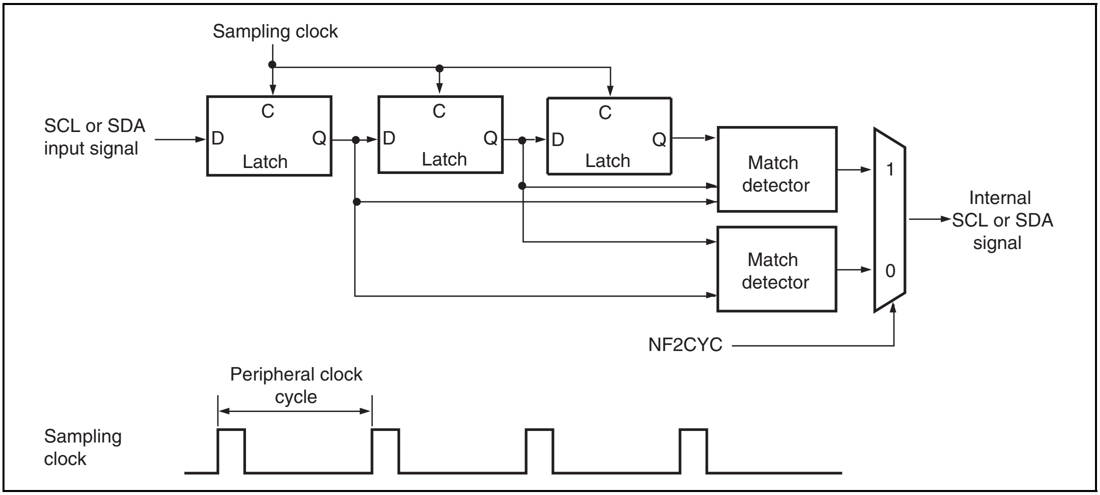


Figure 18.18 Block Diagram of Noise Filter

20.2 Register Descriptions

The CMT has the following registers. For the states of these registers in each processing status, refer to section 27, List of Registers.

Table 20.1 Register Configuration

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Common	Compare match timer start register	CMSTR	R/W	H'0000	H'FFFFCE00	8, 16, 32
0	Compare match timer control/ status register_0	CMCSR_0	R/W	H'0000	H'FFFFCE02	8, 16
	Compare match counter_0	CMCNT_0	R/W	H'0000	H'FFFFCE04	8, 16, 32
	Compare match constant register_0	CMCOR_0	R/W	H'FFFF	H'FFFFCE06	8, 16
1	Compare match timer control/ status register_1	CMCSR_1	R/W	H'0000	H'FFFFCE08	8, 16, 32
	Compare match counter_1	CMCNT_1	R/W	H'0000	H'FFFFCE0A	8, 16
	Compare match constant register_1	CMCOR_1	R/W	H'FFFF	H'FFFFCE0C	8, 16, 32

Table 21.18 SH7084 Pin Functions in Each Operating Mode (2)

	Pin Name			
	On-Chip ROM Enabled (MCU Mode 2)		Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
21, 37, 65, 80, 103	Vcc	Vcc	Vcc	Vcc
3, 27, 39, 55, 61, 71, 90, 101	Vss	Vss	Vss	Vss
23, 81, 109	VCL	VCL	VCL	VCL
100	AVcc	AVcc	AVcc	AVcc
97	AVss	AVss	AVss	AVss
82	PLLVss	PLLVss	PLLVss	PLLVss
74	EXTAL	EXTAL	EXTAL	EXTAL
72	XTAL	XTAL	XTAL	XTAL
75	MD0	MD0	MD0	MD0
73	MD1	MD1	MD1	MD1
77	FWE	FWE	FWE	FWE
84	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
35	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
76	NMI	NMI	NMI	NMI
33	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$
51	PA0	PA0/$\overline{\text{CS4}}$/RXD0	PA0	PA0/RXD0
50	PA1	PA1/$\overline{\text{CS5}}$/TXD0	PA1	PA1/TXD0
49	PA2	PA2/A25/DREQ0/IRQ0/SCK0	PA2	PA2/DREQ0/IRQ0/SCK0
48	PA3	PA3/A24/RXD1	PA3	PA3/RXD1
47	PA4	PA4/A23/TXD1	PA4	PA4/TXD1
46	PA5	PA5/A22/DREQ1/IRQ1/SCK1	PA5	PA5/IRQ1/SCK1
45	PA6	PA6/$\overline{\text{CS2}}$/TCLKA	PA6	PA6/TCLKA
44	PA7	PA7/$\overline{\text{CS3}}$/TCLKB	PA7	PA7/TCLKB
43	PA8	PA8/RDWR/IRQ2/TCLKC	PA8	PA8/IRQ2/TCLKC
42	PA9	PA9/CKE/IRQ3/TCLKD	PA9	PA9/IRQ3/TCLKD
41	PA10	PA10/$\overline{\text{CS0}}$/$\overline{\text{POE4}}$	PA10	PA10/$\overline{\text{POE4}}$

Bit	Bit Name	Initial Value	R/W	Description
6	PE5MD2	0	R/W	PE5 Mode Select the function of the PE5/$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$/TIOC1B/TXD3/AUDATA1 pin. Fixed to AUDATA1 output when using the AUD function of the E10A. 000: PE5 I/O (port) 001: TIOC1B I/O (MTU2) 010: TXD3 output (SCIF) 101: $\overline{\text{CS6}}$/$\overline{\text{CE1B}}$ output (BSC)* Other than above: Setting prohibited
5	PE5MD1	0	R/W	
4	PE5MD0	0	R/W	
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PE4MD2	0	R/W	PE4 Mode Select the function of the PE4/$\overline{\text{IOIS16}}$/TIOC1A/RXD3/AUDATA2 pin. Fixed to AUDATA2 output when using the AUD function of the E10A. 000: PE4 I/O (port) 001: TIOC1A I/O (MTU2) 010: RXD3 input (SCIF) 101: $\overline{\text{IOIS16}}$ input (BSC)* Other than above: Setting prohibited
1	PE4MD1	0	R/W	
0	PE4MD0	0	R/W	

Note: * This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

		External Space (Burst ROM (Clock Synchronous))						
		32-bit Space						
Pin Name		Most Significant Byte	Second Byte	Third Byte	Least Significant Byte	Upper Word	Lower Word	Longword
$\overline{\text{WE}}$	R	H	H	H	H	H	H	H
	W	—	—	—	—	—	—	—
$\overline{\text{ICIOWR}}$	R	H	H	H	H	H	H	H
	W	—	—	—	—	—	—	—
A29 to A0		Address	Address	Address	Address	Address	Address	Address
D31 to D24		Data	Hi-Z	Hi-Z	Hi-Z	Data	Hi-Z	Data
D23 to D16		Hi-Z	Data	Hi-Z	Hi-Z	Data	Hi-Z	Data
D15 to D8		Hi-Z	Hi-Z	Data	Hi-Z	Hi-Z	Data	Data
D7 to D0		Hi-Z	Hi-Z	Hi-Z	Data	Hi-Z	Data	Data

[Legend]

R: Read

W: Write

Enabled: Chip select signals corresponding to accessed areas = Low.
The other chip select signals = High.

Table C.1 Pin States of Bus Related Signals (10)

	External Space (SDRAM)		
	16-bit Space		
Pin Name	Upper Byte	Lower Byte	Word/Longword
$\overline{\text{CS0}}$ to $\overline{\text{CS8}}$	Enabled*[1]	Enabled*[1]	Enabled*[1]
$\overline{\text{CE1A}}$, $\overline{\text{CE1B}}$, $\overline{\text{CE2A}}$, $\overline{\text{CE2B}}$	H	H	H
$\overline{\text{BS}}$	L	L	L
$\overline{\text{RASU}}$, $\overline{\text{RASL}}$	Enabled*[2]	Enabled*[2]	Enabled*[2]
$\overline{\text{CASU}}$, $\overline{\text{CASL}}$	Enabled*[2]	Enabled*[2]	Enabled*[2]
DQMUU	H	H	H
DQMUL	H	H	H
DQMLU	L	H	L
DQMLL	H	L	L

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>11.3.10 Timer A/D Converter Start Request Control Register (TADCR)</td><td>488</td><td>Table amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>0</td><td>ITB4VE</td><td>0*[1]*[2]*[3]</td><td>R/W</td><td>TCIV_4 Interrupt Skipping Link Enable
Select whether to link A/D converter start requests (TRG4BN) with TCIV_4 interrupt skipping operation.
0: Does not link with TCIV_4 interrupt skipping operation
1: Links with TCIV_4 interrupt skipping operation</td></tr>
</table>
Table note amended
Notes: 1. Set to 0 when complementary PWM mode is not selected.
2. Clear this bit to 0 when interrupt skipping is disabled (when the T3AEN or T4VEN bit in the timer interrupt skipping set register (TITCR) is cleared to 0 or when the skipping count set bit (3ACOR or 4VCOR) in TITCR is cleared to 0).
3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
15.4.3 Clock Synchronous Mode Figure 15.12 Sample Flowchart for Receiving Serial Data (Clock Synchronous Mode) (2)	790	Figure title and description amended Description amended 2. Receive data is shifted into SCRSR in order from the LSB to the MSB (when LSB-first transfer is selected).
Figure 15.13 Example of SCI Receive Operation (when LSB-First Transfer is Selected)	791	Figure title amended
Figure 15.14 Sample Flowchart for Transmitting/Receiving Serial Data (Clock Synchronous Mode)	792	Figure and title amended [4] Serial transmission/reception continuation procedure: To continue serial transmission/reception, before the last bit of the current frame is received, finish reading the RDRF flag, reading SCRDR, and clearing the RDRF flag to 0. Also, before the last bit of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to SCTDR and clear the TDRE flag to 0.
15.4.5 Multiprocessor Serial Data Transmission	795	Description amended Figure 15.16 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SCSSR to 1 before transmission, and maintain the MPBT value at 1 until the ID transmission actually completes. For a data transmission cycle, ...
Figure 15.16 Sample Multiprocessor Serial Transmission Flowchart	796	Figure replaced
15.4.6 Multiprocessor Serial Data Reception Figure 15.17 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit, LSB-first)	797	Figure title amended
Figure 15.18 Sample Multiprocessor Serial Reception Flowchart (1)	798	Figure replaced