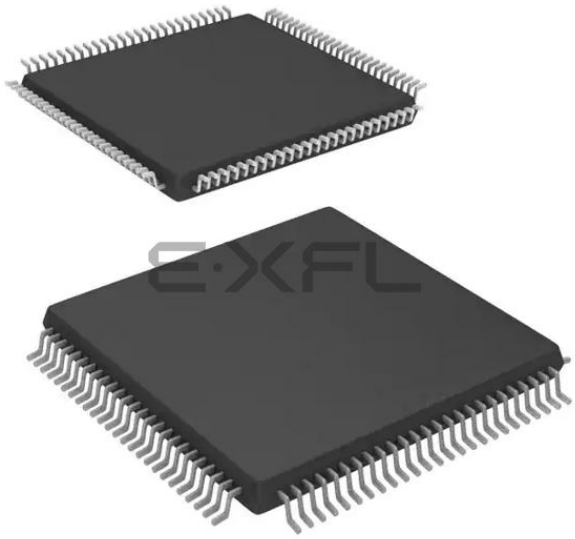
Renesas Electronics America Inc - DF70834AD80FTV Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70834ad80ftv

Items	Specification
Multi-function timer pulse unit 2 (MTU2)	• Maximum 16 lines (maximum 13 lines in SH7083) of pulse input/output and three lines of pulse input based on six channels of 16-bit timers • 21 output compare and input capture registers • A total of 21 independent comparators • Selection of eight counter input clocks • Input capture function • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Complementary PWM output mode — Six-phase (four-phase in SH7083) non-overlapping waveforms output for inverter control — Automatic dead time setting — 0% to 100% PWM duty cycle specifiable — Output suppression — A/D conversion delaying function — Dead time compensation — Interrupt skipping at crest or trough • Reset-synchronized PWM mode Three-phase PWM waveforms in positive and negative phases can be output with a required duty cycle • Phase counting mode Two-phase encoder pulse counting available
Multi-function timer pulse unit 2S (MTU2S)	• Subset of MTU2, including channels 3 to 5 • Operating at 80 MHz max.
Port output enable (POE)	• High-impedance control of waveform output pins in MTU2 and MTU2S
Compare match timer (CMT)	• 16-bit counters • Compare match interrupts can be generated • Two channels
Serial communication interface (SCI)	• Clock synchronous or asynchronous mode • Three channels

4.6.2 External Clock Input Method

Figure 4.4 shows an example of an external clock input connection. In this case, make the external clock high level to stop it when in software standby mode. During operation, make the external input clock frequency 5 to 12.5 MHz.

When leaving the XTAL pin open, make sure the parasitic capacitance is less than 10 pF.

Even when inputting an external clock, be sure to wait at least the oscillation stabilization time in power-on sequence or in releasing software standby mode, in order to ensure the PLL stabilization time.

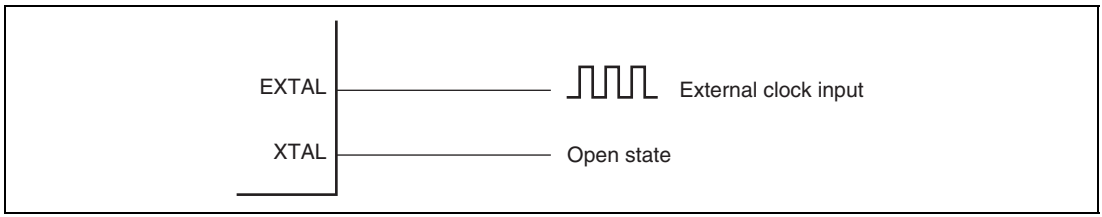


Figure 4.4 Example of External Clock Connection

Section 5 Exception Handling

5.1 Overview

5.1.1 Types of Exception Handling and Priority

Exception handling is started by four sources: resets, address errors, interrupts and instructions and have the priority, as shown in table 5.1. When several exceptions are detected at once, they are processed according to the priority.

Table 5.1 Types of Exceptions and Priority

Exception	Exception Source	Priority
Reset	Power-on reset	High
	Manual reset	
Interrupt	User break (break before instruction execution)	
Address error	CPU address error (instruction fetch)	
Instruction	General illegal instructions (undefined code)	
	Illegal slot instruction (undefined code placed immediately after a delayed branch instruction*1 or instruction that changes the PC value*2)	
	Trap instruction (TRAPA instruction)	
Address error	CPU address error (data access)	
Interrupt	User break (break after instruction execution or operand break)	
Address error	DMAC/DTC address error (data access)	
Interrupt	NMI	
	IRQ	
	On-chip peripheral modules	Low

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, and BRAF.
2. Instructions that change the PC value: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, TRAPA, BF/S, BT/S, BSRF, BRAF, LDC Rm,SR, LDC.L @Rm+,SR.

<Channel B>

Address: H'0003722E, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read/word

After an instruction with address H'00037226 is executed, a user break occurs before an instruction with address H'0003722E is executed.

(Example 1-3)

- Register specifications

  BARA = H'00027128, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000000, BDMRA = H'00000000, BARB = H'00031415, BAMRB = H'00000000, BBRB = H'0054, BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000000

  Specified conditions: Channel A/channel B independent mode

  <Channel A>

  Address: H'00027128, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

  <Channel B>

  Address: H'00031415, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

  On channel A, no user break occurs since instruction fetch is not a write cycle. On channel B, no user break occurs since instruction fetch is performed for an even address.

(Example 1-4)

- Register specifications

  BARA = H'00037226, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000000, BDMRA = H'00000000, BARB = H'0003722E, BAMRB = H'00000000, BBRB = H'0056, BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000008

  Specified conditions: Channel A/channel B sequential mode

  <Channel A>

  Address: H'00037226, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

Bit	Bit Name	Initial Value	R/W	Description
2, 1	—	All 0	R	Reserved These are read-only bits and cannot be modified.
0	ERR	0	R/(W)*	Transfer Stop Flag Indicates that the DTC address error or NMI interrupt request has occurred. If a DTC address error or NMI interrupt occurs while the DTC is active, address error handling or NMI interrupt handling processing is executed after the DTC has released the bus mastership. The DTC stops in the transfer information writing state after transferring data. 0: No interrupt occurs 1: An interrupt occurs [Clearing condition] • When writing 0 after reading 1

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

10.5.11 Number of Cycles per Access to On-Chip RAM by DMAC

The number of cycles required for read/write access to on-chip RAM from the DMAC is as shown in table 10.9, which differs depending on the frequency ratio of Iϕ (internal clock) to Bϕ (external bus clock).

Table 10.9 Number of Cycles per Access to On-Chip RAM by DMAC

Setting of Iϕ:Bϕ	Read	Write
1:1	3 × Bcyc	3 × Bcyc
1:1/2	2 × Bcyc	1 × Bcyc
1:1/3	2 × Bcyc	1 × Bcyc
1:1/4 or less	1 × Bcyc	1 × Bcyc

Notes: 1. Bcyc is the external bus clock cycle.
2. The number of cycles for access to the on-chip peripheral I/O or an external device are indicated in section 9.5.16, Access to On-Chip Peripheral I/O Registers by CPU, and section 9.5.17, Access to External Memory by CPU. The access cycles are obtained by subtracting the cycles of Iϕ required for L-bus access from the cycles required for access by the CPU.

10.5.12 Note on DMAC Transfer in Burst Mode when Activation Source Is MTU2

The corresponding bit among DMMTU4 to DMMTU0 in the bus function extending register (BSCEHR) must be set when performing DMA transfer in burst mode with the MTU2 specified as the activation source. For details, see section 9.4.8, Bus Function Extending Register (BSCEHR).

10.5.13 Bus Function Extending Register (BSCEHR)

With the bus function extending register (BSCEHR), it is possible to set the function to perform transfer by the DMAC preferentially. For details, see section 9.4.8, Bus Function Extending Register (BSCEHR).

11.8.4 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation, etc.

- When making a transition to a mode (Normal, PWM1, PWM2, PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of a TIOR setting.
- In PWM mode 1, since a waveform is not output to the TIOC*B (TIOC *D) pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 1.
- In PWM mode 2, since a waveform is not output to the cycle register pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 2.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, setting TIOR will not initialize the buffer register pins. If initialization is required, clear buffer mode, carry out initialization, then set buffer mode again.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, setting TIOR will not initialize the TGRC pin. To initialize the TGRC pin, clear buffer mode, carry out initialization, then set buffer mode again.
- When making a transition to a mode (CPWM, RPWM) in which the pin output level is selected by the timer output control register (TOCR) setting, switch to normal mode and perform initialization with TIOR, then restore TIOR to its initial value, and temporarily disable channel 3 and 4 output with the timer output master enable register (TOER). Then operate the unit in accordance with the mode setting procedure (TOCR setting, TMDR setting, TOER setting).

Note: Channel number is substituted for * indicated in this article.

Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in PWM Mode 1: Figure 11.154 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in PWM mode 1 after re-setting.

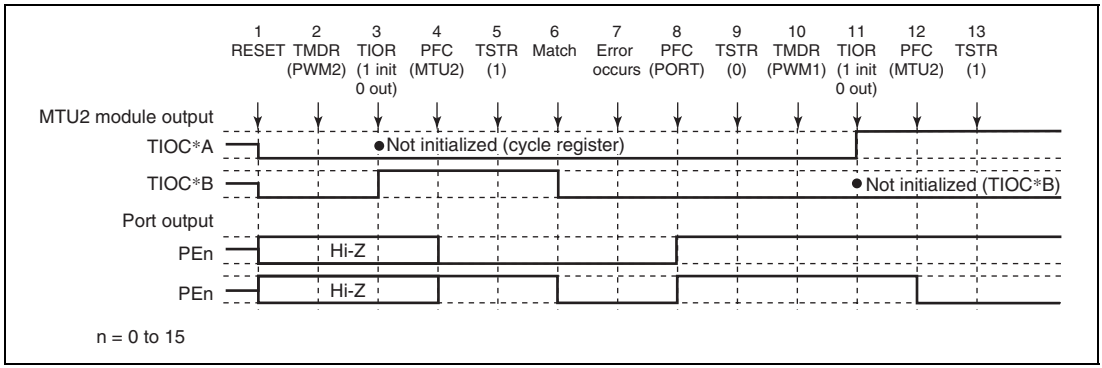


Figure 11.154 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 1

1 to 9 are the same as in figure 11.153.

10. Set PWM mode 1.
11. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized.)
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in Phase Counting Mode: Figure 11.156 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in phase counting mode after re-setting.

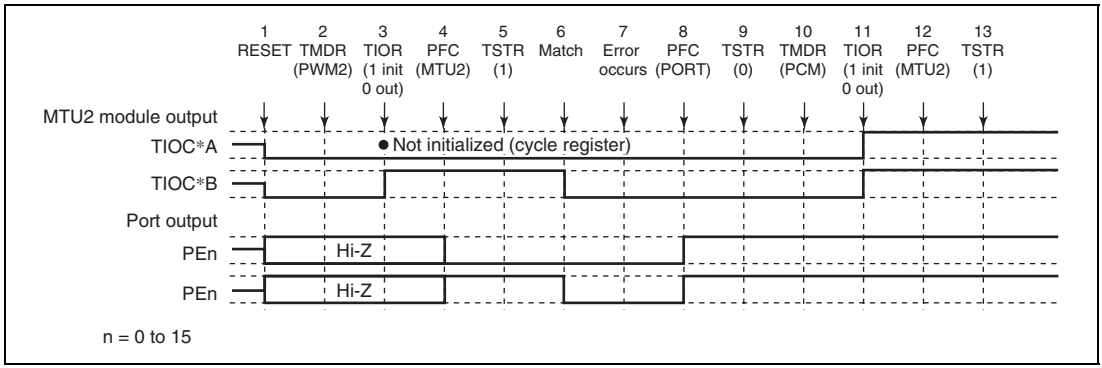


Figure 11.156 Error Occurrence in PWM Mode 2, Recovery in Phase Counting Mode

1 to 9 are the same as in figure 11.153.

10. Set phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

13.3.2 Output Level Control/Status Register 1 (OCSR1)

OCSR1 is a 16-bit readable/writable register that controls the enable/disable of both output level comparison and interrupts, and indicates status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSF1	-	-	-	-	-	OCE1	OIE1	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*1	R	R	R	R	R	R/W*2	R/W	R	R	R	R	R	R	R	R

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

2. Can be modified only once after a power-on reset.

Bit	Bit Name	Initial value	R/W	Description
15	OSF1	0	R/(W)*1	Output Short Flag 1 This flag indicates that any one of the three pairs of MTU2 2-phase outputs to be compared has simultaneously become an active level. [Clearing condition] • By writing 0 to OSF1 after reading OSF1 = 1 [Setting condition] • When any one of the three pairs of 2-phase outputs has simultaneously become an active level
14 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	OCE1	0	R/W*2	Output Short High-Impedance Enable 1 This bit specifies whether to place the pins in high-impedance state when the OSF1 bit in OCSR1 is set to 1. 0: Does not place the pins in high-impedance state 1: Places the pins in high-impedance state
8	OIE1	0	R/W	Output Short Interrupt Enable 1 This bit enables or disables interrupt requests when the OSF1 bit in OCSR is set to 1. 0: Interrupt requests disabled 1: Interrupt requests enabled

16.2 Input/Output Pins

The SCIF has the serial pins summarized in table 16.1.

Table 16.1 Pin Configuration

Channel	Pin Name	Abbreviation	I/O	Function
3	Serial clock pin	SCK3	I/O	Clock I/O
	Receive data pin	RXD3	Input	Receive data input
	Transmit data pin	TXD3	Output	Transmit data output
	Request to send pin	$\overline{\text{RTS3}}$	Output	Request to send
	Clear to send pin	$\overline{\text{CTS3}}$	Input	Clear to send

Note: In the following descriptions in this section, the channel number in the abbreviated pin names is omitted as in SCK, RXD, TXD, $\overline{\text{RTS}}$, and $\overline{\text{CTS}}$.

17.3.1 SS Control Register H (SSCRH)

SSCRH specifies master/slave device selection, bidirectional mode enable, SSO pin output value selection, SSCK pin selection, and $\overline{SCS}$ pin selection.

Bit:	7	6	5	4	3	2	1	0
	MSS	BIDE	-	SOL	SOLP	-	CSS[1:0]	
Initial value:	0	0	0	0	1	1	0	1
R/W:	R/W	R/W	R	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MSS	0	R/W	Master/Slave Device Select Selects that this module is used in master mode or slave mode. When master mode is selected, transfer clocks are output from the SSCK pin. When the CE bit in SSSR is set, this bit is automatically cleared. 0: Slave mode is selected. 1: Master mode is selected.
6	BIDE	0	R/W	Bidirectional Mode Enable Selects that both serial data input pin and output pin are used or one of them is used. However, transmission and reception are not performed simultaneously when bidirectional mode is selected. For details, section 17.4.3, Relationship between Data Input/Output Pins and Shift Register. 0: Standard mode (two pins are used for data input and output) 1: Bidirectional mode (one pin is used for data input and output)
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	RDRF	0	R/W	Receive Data Register Full Indicates whether or not SSRDR contains receive data. [Setting condition] • When receive data is transferred from SSTRSR to SSRDR after successful serial data reception [Clearing conditions] • When writing 0 after reading RDRF = 1 • When reading receive data from SSRDR with FCLRM = 1 • When the DTC is activated by an SSRXI interrupt and receive data is read into SSRDR while the DISEL bit in MRB of the DTC is 0 (except when DTC transfer counter value is H'0000)*1

Caution is required because writing data for transmission to ICDRT automatically clears TDRE and TEND and reading from ICDRR automatically clears RDRF. In particular, if TDRE is again set at the same time as data for transmission are written to ICDRT, an extra byte may be transmitted when TDRE is then cleared.

Table 18.4 Interrupt Requests

Interrupt Request	Abbreviation	Interrupt Condition	I²C Bus Format	Clocked Synchronous Serial Format	DTC Activation	Priority
NACK detection	IINAKI*	{(NACKF = 1) + (AL/OVE = 1)} • (NAKIE = 1)	√	—	—	High
Arbitration lost/ overrun error			√	√	—	
Transmit end	IITEI	(TEND = 1) • (TEIE = 1)	√	√	—	
Stop condition detection	IISTPI	(STOP = 1) • (STIE = 1)	√	—	—	
Transmit data empty	IITXI	(TDRE = 1) • (TIE = 1)	√	√	√	
Receive data full	IIRXI	(RDRF = 1) • (RIE = 1)	√	√	√	Low

Note: * In the case of IINAKI, the IPR bit in the INTC, which determines the priority, is different. Depending on the setting of the IPR bit, the priority may be lower than that of IIRXI.

Bit	Bit Name	Initial Value	R/W	Description
10	PB2MD2	0	R/W	PB2 Mode
9	PB2MD1	0	R/W	Select the function of the PB2/IRQ0/$\overline{\text{POE0}}$ pin.
8	PB2MD0	0	R/W	000: PB2 I/O (port)
				001: IRQ0 input (INTC)
				010: $\overline{\text{POE0}}$ input (POE)
				Other than above: Setting prohibited
7	—	0	R	Reserved
				This bit is always read as 0. The write value should always be 0.
6	PB1MD2	0	R/W	PB1 Mode
5	PB1MD1	0	R/W	Select the function of the PB1/A17/TIC5W pin.
4	PB1MD0	0*[1]	R/W	000: PB1 I/O (port)
				001: A17 output (BSC)*[2]
				011: TIC5W input (MTU2)
				Other than above: Setting prohibited
3	—	0	R	Reserved
				This bit is always read as 0. The write value should always be 0.
2	PB0MD2	0	R/W	PB0 Mode
1	PB0MD1	0	R/W	Select the function of the PB0/A16/TIC5WS pin.
0	PB0MD0	0*[1]	R/W	000: PB0 I/O (port)
				001: A16 output (BSC)*[2]
				011: TIC5WS input (MTU2S)
				Other than above: Setting prohibited

Notes: 1. The initial value is 1 in the on-chip ROM disabled external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

SH7086:

- Port E Control Register H2 (PECRH2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PE21 MD1	PE21 MD0	-	-	PE20 MD1	PE20 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PE21MD1	0	R/W	PE21 Mode
4	PE21MD0	0	R/W	Select the function of the PE21/TIOC4DS pin. 00: PE21 I/O (port) 01: TIOC4DS I/O (MTU2S) Other than above: Setting prohibited
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PE20MD1	0	R/W	PE20 Mode
0	PE20MD0	0	R/W	Select the function of the PE20/TIOC4CS pin. 00: PE20 I/O (port) 01: TIOC4CS I/O (MTU2S) Other than above: Setting prohibited

21.2 Usage Notes

1. In this LSI, the same function is available as a multiplexed function on multiple pins. This approach is intended to increase the number of selectable pin functions and to allow the easier design of boards. If two or more pins are specified for one function, however, there are two cautions shown below.
   — When the pin function is input
   Signals input to several pins are formed as one signal through OR or AND logic and the signal is transmitted into the LSI. Therefore, a signal that differs from the input signals may be transmitted to the LSI depending on the input signals in other pins that have the same functions. Table 21.22 shows the transmit forms of input functions allocated to several pins. When using one of the functions shown below in multiple pins, use it with care of signal polarity considering the transmit forms.

Table 21.22 Transmit Forms of Input Functions Allocated to Multiple Pins

OR Type	AND Type
SCK0, SCK3, RXD0, RXD3, TIOC3AS to TIOC3DS, TIOC4AS to TIOC4DS, TIC5U, TIC5V, TIC5W, TIC5US, TIC5VS, TIC5WS	IRQ0 to IRQ7, DREQ0, DREQ1, $\overline{\text{BREQ}}$, $\overline{\text{WAIT}}$, $\overline{\text{ADTRG}}$, $\overline{\text{POE4}}$ to $\overline{\text{POE8}}$

   OR type: Signals input to several pins are formed as one signal through OR logic and the signal is transmitted into the LSI.
   AND type: Signals input to several pins are formed as one signal through AND logic and the signal is transmitted into the LSI.
   — When the pin function is output
   Each selected pin can output the same function.
2. When the port input is switched from a low level to the DREQ or the IRQ edge for the pins that are multiplexed with input/output and DREQ or IRQ, the corresponding edge is detected.
3. Do not set functions other than those specified in tables 21.17 to 21.20. Otherwise, correct operation cannot be guaranteed.
4. PFC setting in single-chip mode (MCU operating mode 3)
   In single-chip mode, do not set the PFC to select address bus, data bus, bus control, or the $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, CK, DACK, or TEND signals. If they are selected, address bus signals function as high- or low-level outputs, data bus signals function as high-impedance outputs, and the other output signals function as high-level outputs. As $\overline{\text{BREQ}}$ and $\overline{\text{WAIT}}$ function as inputs, do not leave them open. However, the bus-mastership-request inputs and external waits are disabled.

22.6 Port F

Port F in the SH7083, SH7084, and SH7085 is an input-only port with the 8 pins shown in figure 22.15.

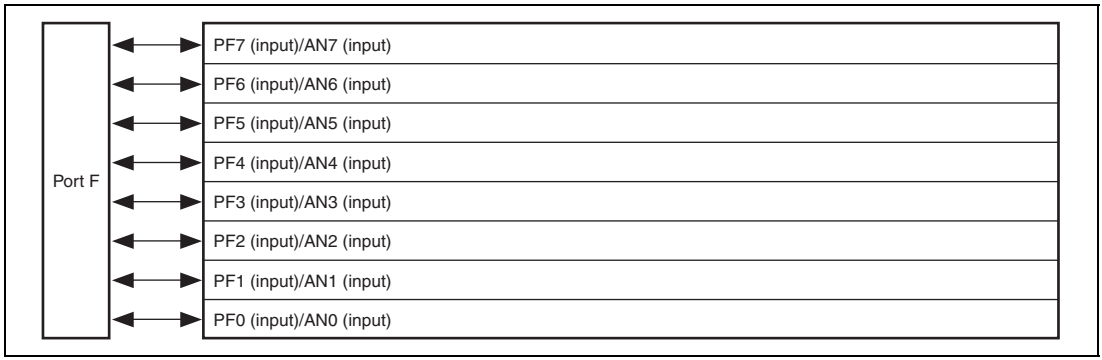


Figure 22.15 Port F (SH7083, SH7084, SH7085)

Port F in the SH7086 is an input-only port with the 16 pins shown in figure 22.16.

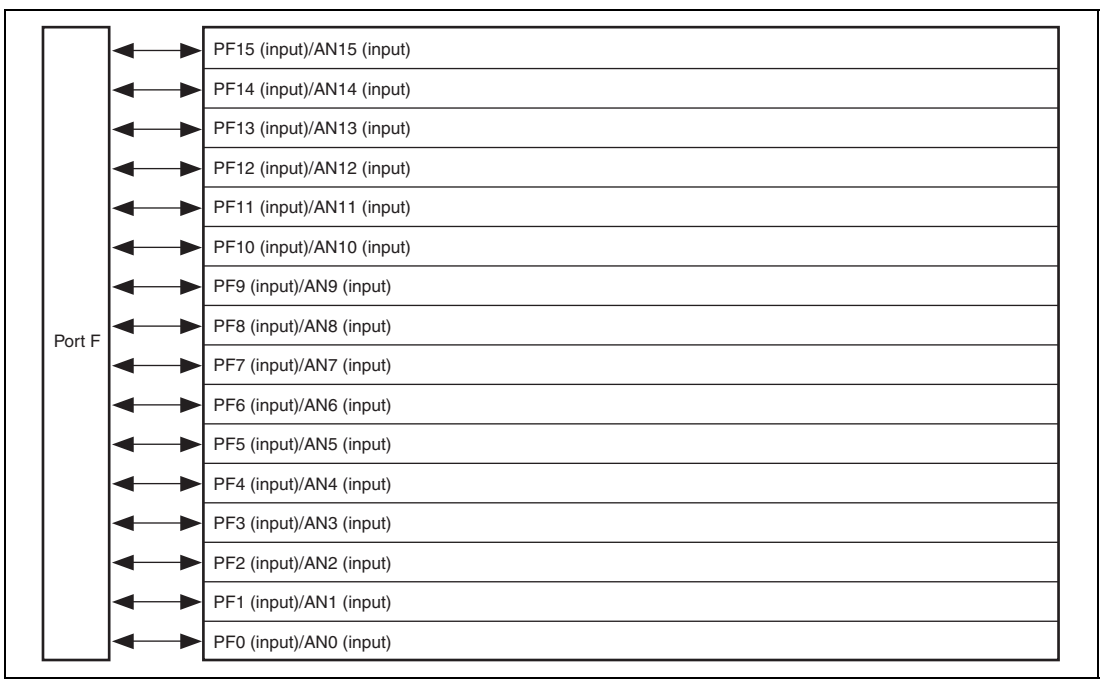
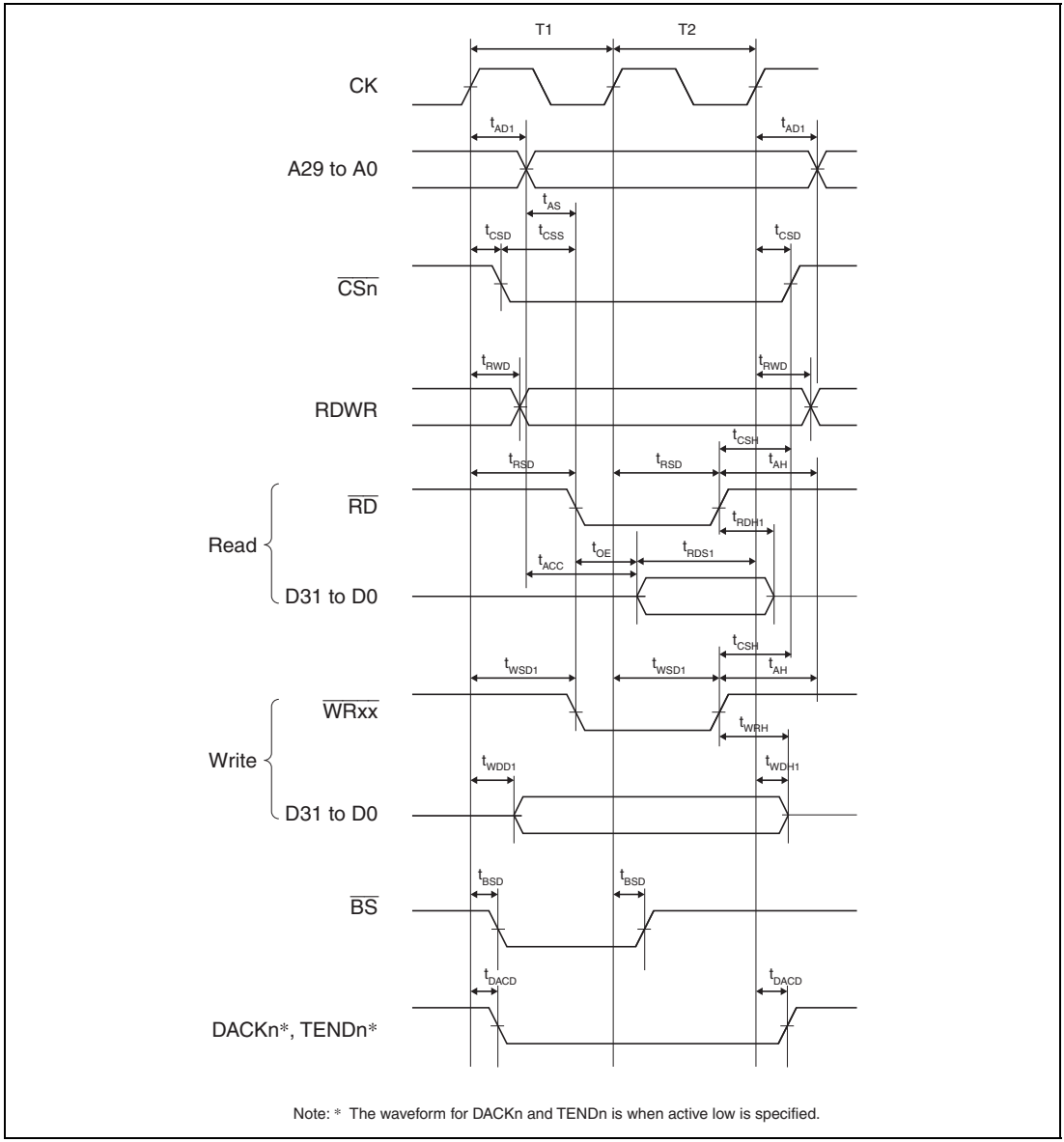
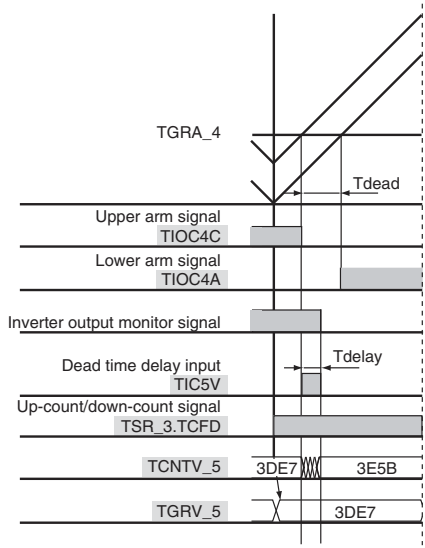
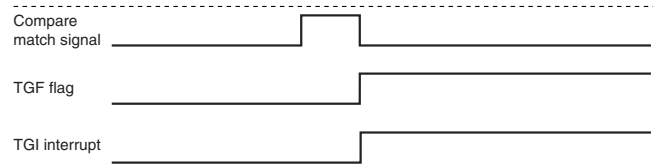


Figure 22.16 Port F (SH7086)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 28.11 Basic Bus Timing for Normal Space (No Wait)

Item	Page	Revision (See Manual for Details)
11.4.13 TCNTU_5/TCNTV_5/TCNTW_5 Capture at Crest and/or Trough in Complementary PWM Operation Figure 11.92 TCNTU_5/TCNTV_5/TCNTW_5 Capturing at Crest and/or Trough in Complementary PWM Operation	616	Figure and title amended 
11.6.2 Interrupt Signal Timing Figure 11.110 TGI Interrupt Timing (Compare Match) (Channel 5)	629	Figure amended  Note: The compare match is generated even though TCNT is stopped.
11.7.24 Notes on Using the A/D Converter Start Request Delaying Function in Complementary PWM Mode	651	Section added