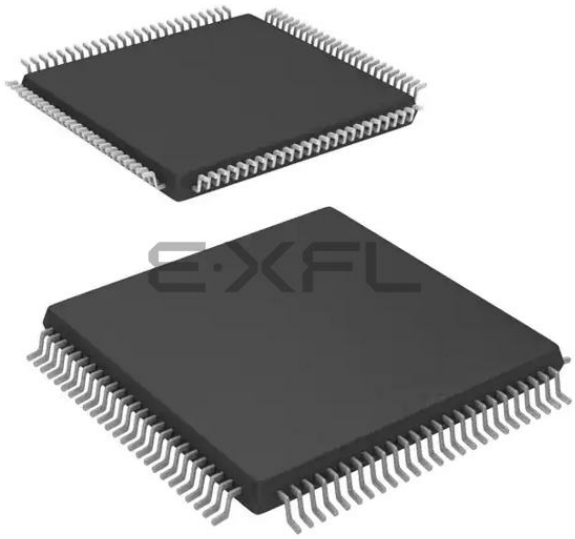
Renesas Electronics America Inc - DF70834AN80FTV Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70834an80ftv

Classification	Symbol	I/O	Name	Function
Bus control	$\overline{\text{CE2A}}$	O	Upper byte selection for PCMCIA card	Chip enable for PCMCIA connected to area 5 Available only in the SH7085/SH7086.
	$\overline{\text{CE2B}}$	O	Upper byte selection for PCMCIA card	Chip enable for PCMCIA connected to area 6 Available only in the SH7085/SH7086.
	$\overline{\text{ICIOWR}}$	O	Write strobe for PCMCIA I/O	Connected to the PCMCIA I/O write strobe signal Available only in the SH7085/SH7086.
	$\overline{\text{ICIORD}}$	O	Read strobe for PCMCIA I/O	Connected to the PCMCIA I/O read strobe signal Available only in the SH7085/SH7086.
	$\overline{\text{WE}}$	O	Write strobe for PCMCIA memory	Connected to the PCMCIA memory write strobe signal Available only in the SH7085/SH7086.
	$\overline{\text{IOIS16}}$	I	PCMCIA dynamic bus sizing	Indicates 16-bit I/O for PCMCIA in little endian mode. This LSI does not support little endian and this pin must be held low. Available only in the SH7085/SH7086.
Direct memory access controller (DMAC)	DREQ3 to DREQ0	I	DMA-transfer request	Input pins to receive external requests for DMA transfer. Only DREQ1 and DREQ0 are available in the SH7083/SH7084.
	DACK3 to DACK0	O	DMA-transfer strobe	Strobe signal output pins for the external device that has requested DMA transfer. Only DACK1 and DACK0 are available in the SH7083/SH7084.
	TEND1, TEND0	O	DMA-transfer end	Output pins for DMA transfer end signals

Instruction	Operation	Code	Execution Cycles	T Bit
DMULU.L Rm,Rn	Unsigned operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bits	0011nnnnmmmm0101	2 to 5*	—
DT Rn	Rn - 1 → Rn, if Rn = 0, 1 → T, else 0 → T	0100nnnn00010000	1	Comparison result
EXTS.B Rm,Rn	A byte in Rm is sign-extended → Rn	0110nnnnmmmm1110	1	—
EXTS.W Rm,Rn	A word in Rm is sign-extended → Rn	0110nnnnmmmm1111	1	—
EXTU.B Rm,Rn	A byte in Rm is zero-extended → Rn	0110nnnnmmmm1100	1	—
EXTU.W Rm,Rn	A word in Rm is zero-extended → Rn	0110nnnnmmmm1101	1	—
MAC.L @Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 32 × 32 + 64 → 64 bits	0000nnnnmmmm1111	2 to 5*	—
MAC.W @Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 16 × 16 + 64 → 64 bits	0100nnnnmmmm1111	2 to 4*	—
MUL.L Rm,Rn	Rn × Rm → MACL 32 × 32 → 32 bits	0000nnnnmmmm0111	2 to 5*	—
MULS.W Rm,Rn	Signed operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1111	1 to 3*	—
MULU.W Rm,Rn	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1110	1 to 3*	—
NEG Rm,Rn	0-Rm → Rn	0110nnnnmmmm1011	1	—
NEGC Rm,Rn	0-Rm-T → Rn, Borrow → T	0110nnnnmmmm1010	1	Borrow
SUB Rm,Rn	Rn-Rm → Rn	0011nnnnmmmm1000	1	—
SUBC Rm,Rn	Rn-Rm–T → Rn, Borrow → T	0011nnnnmmmm1010	1	Borrow
SUBV Rm,Rn	Rn-Rm → Rn, Underflow → T	0011nnnnmmmm1011	1	Overflow

Note: * Indicates the number of execution cycles for normal operation.

Table 9.24 Relationship between BSZ[1:0], A2ROW[1:0]/A3ROW[1:0], A2COL[1:0]/A3COL[1:0], and Address Multiplex Output (5)-2

Setting				
BSZ[1:0]	**A2ROW[1:0]/ A3ROW[1:0]**	**A2COL[1:0]/ A3COL[1:0]**		
10 (16 bits)	**01 (12 bits)**	**10 (10 bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25	A15		
A14	A24*[2]	A24*[2]	A13 (BA1)	Specifies bank
A13	A23*[2]	A23*[2]	A12 (BA0)	
A12	A22	A12	A11	Address
A11	A21	L/H*[1]	A10/AP	Specifies address/precharge
A10	A20	A10	A9	Address
A9	A19	A9	A8	
A8	A18	A8	A7	
A7	A17	A7	A6	
A6	A16	A6	A5	
A5	A15	A5	A4	
A4	A14	A4	A3	
A3	A13	A3	A2	
A2	A12	A2	A1	
A1	A11	A1	A0	
A0	A10	A0		Unused
Example of connected memory				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 10 bits product): 1				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
2. Bank address specification

10.3.2 DMA Destination Address Registers_0 to _3 (DAR_0 to DAR_3)

DAR are 32-bit readable/writable registers that specify the destination address of a DMA transfer. During a DMA transfer, these registers indicate the next destination address. When the data is transferred from an external device with the DACK in single address mode, the DAR is ignored.

To transfer data in 16 bits or in 32 bits, specify the address with 16-bit or 32-bit address boundary. When transferring data in 16-byte units, a 16-byte boundary must be set for the destination address value. The initial value is undefined.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.3.3 DMA Transfer Count Registers_0 to _3 (DMATCR_0 to DMATCR_3)

DMATCR are 32-bit readable/writable registers that specify the DMA transfer count. The number of transfers is 1 when the setting is H'00000001, 16,777,215 when H'00FFFFFF is set, and 16,777,216 (the maximum) when H'00000000 is set. During a DMA transfer, these registers indicate the remaining transfer count.

The upper eight bits of DMATCR are always read as 0, and the write value should always be 0. To transfer data in 16 bytes, one 16-byte transfer (128 bits) counts one. The initial value is undefined.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Burst Mode

  In burst mode, once the DMAC obtains the bus mastership, the transfer is performed continuously without releasing the bus mastership until the transfer end condition is satisfied. In external request mode with level detection of the DREQ pin, however, when the DREQ pin is not active, the bus mastership passes to the other bus master after the DMAC transfer request that has already been accepted ends, even if the transfer end conditions have not been satisfied.

Figure 10.12 shows DMA transfer timing in burst mode.

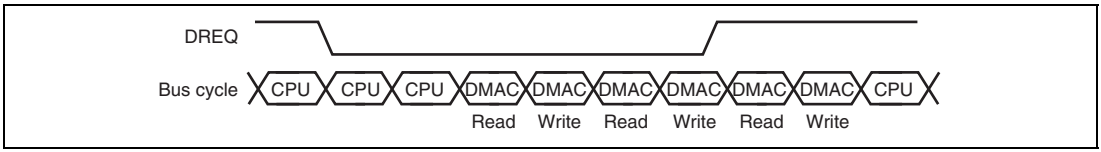


Figure 10.12 DMA Transfer Example in Burst Mode (Dual Address, DREQ Low Level Detection)

Table 11.11 Setting of Operation Mode by Bits MD[3:0]

Bit 3 MD3	Bit 2 MD2	Bit 1 MD1	Bit 0 MD0	Description
0	0	0	0	Normal operation
			1	Setting prohibited
		1	0	PWM mode 1
			1	PWM mode 2*1
	1	0	0	Phase counting mode 1*2
			1	Phase counting mode 2*2
		1	0	Phase counting mode 3*2
			1	Phase counting mode 4*2
1	0	0	0	Reset synchronous PWM mode*3
			1	Setting prohibited
		1	x	Setting prohibited
	1	0	0	Setting prohibited
			1	Complementary PWM mode 1 (transmit at crest)*3
		1	0	Complementary PWM mode 2 (transmit at trough)*3
			1	Complementary PWM mode 2 (transmit at crest and trough)*3

[Legend]

x: Don't care

Notes: 1. PWM mode 2 can not be set for channels 3 and 4.

2. Phase counting mode can not be set for channels 0, 3, and 4.

3. Reset synchronous PWM mode and complementary PWM mode can only be set for channel 3. When channel 3 is set to reset synchronous PWM mode or complementary PWM mode, the channel 4 settings become ineffective and automatically conform to the channel 3 settings. However, do not set channel 4 to reset synchronous PWM mode or complementary PWM mode. Reset synchronous PWM mode and complementary PWM mode cannot be set for channels 0, 1, and 2.

Bit	Bit Name	Initial Value	R/W	Description
2	I2AE	0	R/W	Input Capture Enable Specifies whether to include the TIOC2A pin in the TGRA_1 input capture conditions. 0: Does not include the TIOC2A pin in the TGRA_1 input capture conditions 1: Includes the TIOC2A pin in the TGRA_1 input capture conditions
1	I1BE	0	R/W	Input Capture Enable Specifies whether to include the TIOC1B pin in the TGRB_2 input capture conditions. 0: Does not include the TIOC1B pin in the TGRB_2 input capture conditions 1: Includes the TIOC1B pin in the TGRB_2 input capture conditions
0	I1AE	0	R/W	Input Capture Enable Specifies whether to include the TIOC1A pin in the TGRA_2 input capture conditions. 0: Does not include the TIOC1A pin in the TGRA_2 input capture conditions 1: Includes the TIOC1A pin in the TGRA_2 input capture conditions

(1) Input Capture/Compare Match Interrupt

An interrupt is requested if the TGIE bit in TIER is set to 1 when the TGF flag in TSR is set to 1 by the occurrence of a TGR input capture/compare match on a particular channel. The interrupt request is cleared by clearing the TGF flag to 0. The MTU2 has 21 input capture/compare match interrupts, six for channel 0, four each for channels 3 and 4, two each for channels 1 and 2, and three for channel 5. The TGFE_0 and TGFF_0 flags in channel 0 are not set by the occurrence of an input capture.

(2) Overflow Interrupt

An interrupt is requested if the TCIEV bit in TIER is set to 1 when the TCFV flag in TSR is set to 1 by the occurrence of TCNT overflow on a channel. The interrupt request is cleared by clearing the TCFV flag to 0. The MTU2 has five overflow interrupts, one for each channel.

(3) Underflow Interrupt

An interrupt is requested if the TCIEU bit in TIER is set to 1 when the TCFU flag in TSR is set to 1 by the occurrence of TCNT underflow on a channel. The interrupt request is cleared by clearing the TCFU flag to 0. The MTU2 has two underflow interrupts, one each for channels 1 and 2.

11.5.2 DTC/DMAC Activation

(1) DTC Activation

The DTC can be activated by the TGR input capture/compare match interrupt in each channel or the overflow interrupt in channel 4. For details, see section 8, Data Transfer Controller (DTC).

A total of 20 MTU2 input capture/compare match interrupts and overflow interrupts can be used as DTC activation sources, four each for channels 0 and 3, two each for channels 1 and 2, five for channel 4, and three for channel 5.

(2) DMAC Activation

The DMAC can be activated by the TGRA input capture/compare match interrupt in each channel. For details, see section 10, Direct Memory Access Controller (DMAC).

In the MTU2, a total of five TGRA input capture/compare match interrupts can be used as DMAC activation sources, one each for channels 0 to 4.

When the DMAC is activated by the MTU2, the activation source is cleared at the point the DMAC requests the internal bus mastership. Therefore, the request for DMAC transfer may be kept pending for a certain period even after the activation source is cleared depending on the

Pin initialization procedures are described below for the numbered combinations in table 11.59. The active level is assumed to be low.

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Normal Mode: Figure 11.141 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in normal mode after re-setting.

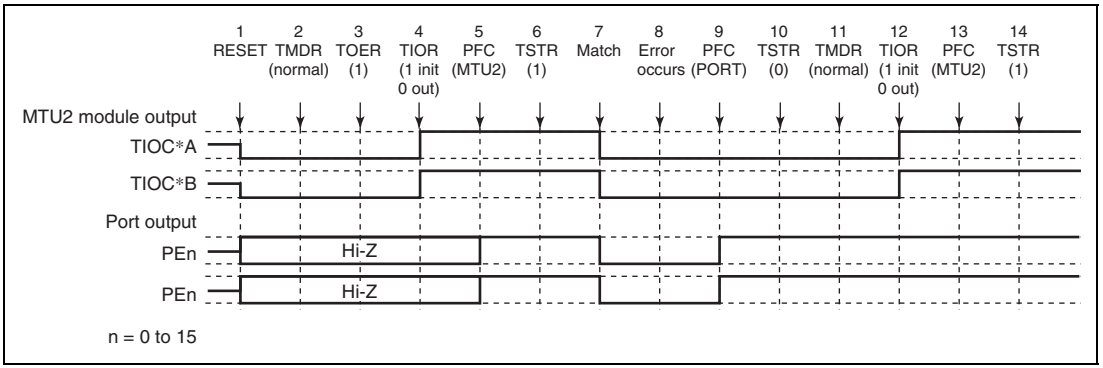


Figure 11.141 Error Occurrence in Normal Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. After a reset, the TMDR setting is for normal mode.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Not necessary when restarting in normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Operation when Error Occurs during Reset-Synchronized PWM Mode Operation, and Operation is Restarted in PWM Mode 1: Figure 11.167 shows an explanatory diagram of the case where an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

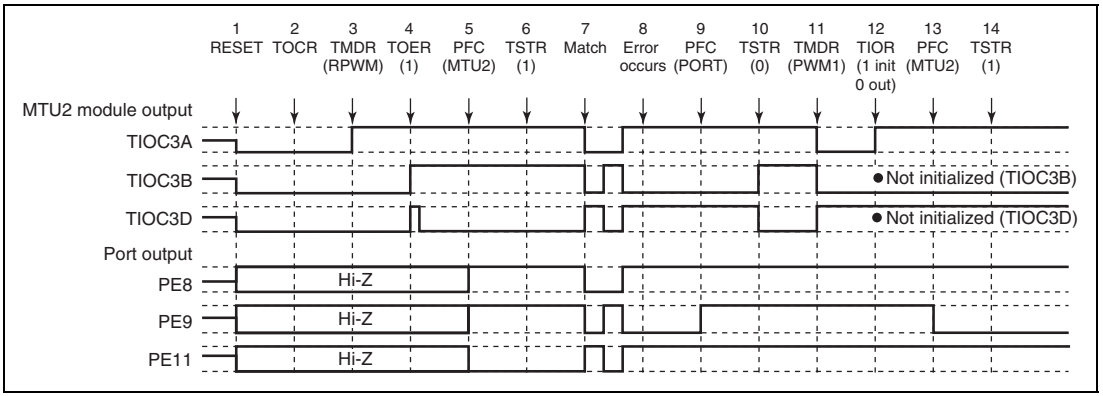


Figure 11.167 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 11.166.

11. Set PWM mode 1. (MTU2 positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

18.7 Bit Synchronous Circuit

In master mode, this module has a possibility that high level period may be short in the two states described below.

- When SCL is driven to low by the slave device
- When the rising speed of SCL is lowered by the load of the SCL line (load capacitance or pull-up resistance)

Therefore, it monitors SCL and communicates by bit with synchronization.

Figure 18.24 shows the timing of the bit synchronous circuit and table 18.6 shows the time when SCL output changes from low to Hi-Z then SCL is monitored.

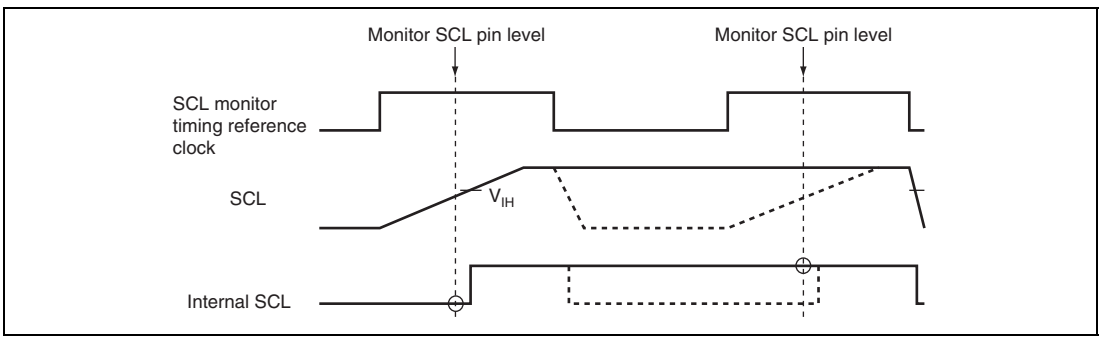


Figure 18.24 The Timing of the Bit Synchronous Circuit

Table 18.6 Time for Monitoring SCL

CKS3	CKS2	NF2CYC	Time for Monitoring SCL*1
0	0	0	6.5 t_{pcyc}*2
		1	5.5 t_{pcyc}*2
	1	0	18.5 t_{pcyc}*2
		1	17.5 t_{pcyc}*2
1	0	0	16.5 t_{pcyc}*2
		1	15.5 t_{pcyc}*2
	1	0	40.5 t_{pcyc}*2
		1	39.5 t_{pcyc}*2

Notes: 1. SCL pin level is monitored after "time for monitoring SCL" has elapsed from the rising edge of the reference clock for monitoring SCL.
2. t_{pcyc} indicates the period of the peripheral clock.

19.3.3 A/D Control Registers_0 to _2 (ADCR_0 to ADCR_2)

ADCR for each module controls A/D conversion.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	ADST	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	ADST	0	R/W	A/D Start Starts or stops A/D conversion. When this bit is set to 1, A/D conversion is started. When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. In single or single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by software, reset, or in software standby mode or module standby mode.
12 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	MSTP13	1	R/W	Module Stop Bit 13 When this bit is set to 1, the supply of the clock to the SCI_2 is halted. 0: SCI_2 operates 1: Clock supply to SCI_2 halted
4	MSTP12	1	R/W	Module Stop Bit 12 When this bit is set to 1, the supply of the clock to the SCI_1 is halted. 0: SCI_1 operates 1: Clock supply to SCI_1 halted
3	MSTP11	1	R/W	Module Stop Bit 11 When this bit is set to 1, the supply of the clock to the SCI_0 is halted. 0: SCI_0 operates 1: Clock supply to SCI_0 halted
2	MSTP10	1	R/W	Module Stop Bit 10 When this bit is set to 1, the supply of the clock to the SSU is halted. 0: SSU operates 1: Clock supply to SSU halted
1, 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

26.3.4 Standby Control Register 4 (STBCR4)

STBCR4 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	MSTP23	MSTP22	MSTP21	-	-	MSTP18	MSTP17	MSTP16
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

26.3.6 Standby Control Register 6 (STBCR6)

STBCR6 is an 8-bit readable/writable register that specifies the state of the power-down modes.

Bit:	7	6	5	4	3	2	1	0
	AUD SRST	HIZ	-	-	-	-	STBY MD	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7	AUDSRST	0	R/W	AUD Software Reset This bit controls the AUD reset by software. When 0 is written to AUDSRST, the AUD module shifts to the power-on reset state. 0: Shifts to the AUD reset state 1: Clears the AUD reset When setting this bit to 1, the MSTP25 bit in STBCR5 should be 0.
6	HIZ	0	R/W	Port High-Impedance In software standby mode, this bit selects whether the pin state is retained or changed to high-impedance. 0: In software standby mode, the pin state is retained 1: In software standby mode, the pin state is changed to high-impedance
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	STBYMD	0	R/W	Software Standby Mode Select This bit selects a transition to software standby mode or deep software standby mode by executing the SLEEP instruction when the STBY bit is 1 in STBCR1. 0: Transition to deep software standby mode 1: Transition to software standby mode
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

28.3.2 Control Signal Timing

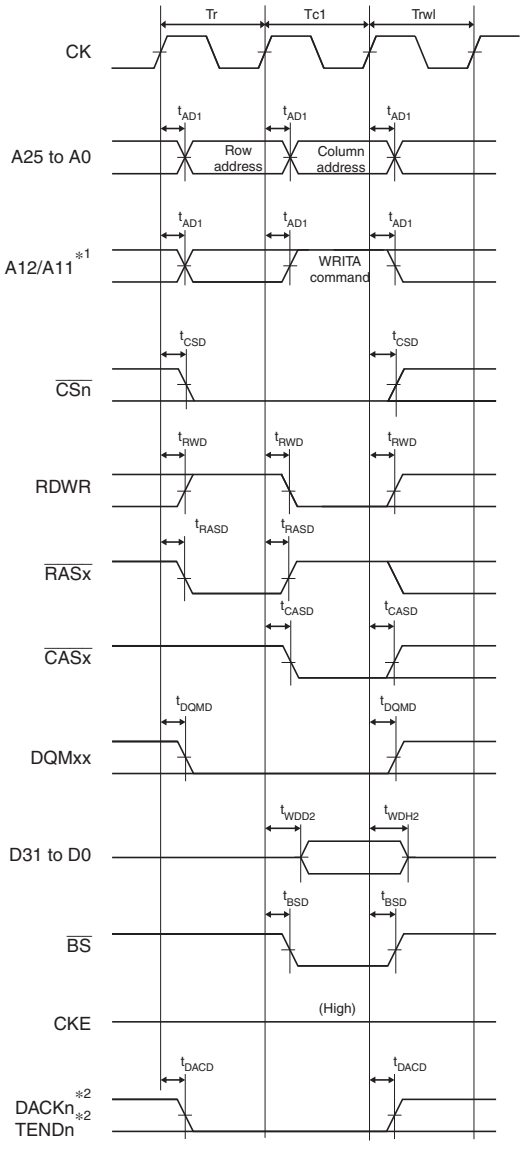
Table 28.7 Control Signal Timing

Conditions: V_{CC} = 3.0 V to 3.6 V or 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +85°C (consumer applications), T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{RES}$ pulse width	t_{RESW}	20*[2]	—	t_{Bcyc}*[4]	Figures 28.3, 28.4,
$\overline{RES}$ setup time*[1]	t_{RESS}	65	—	ns	28.6, 28.7
$\overline{RES}$ hold time	t_{RESH}	15	—	ns	
$\overline{MRES}$ pulse width	t_{MRESW}	20*[3]	—	t_{Bcyc}*[4]	
$\overline{MRES}$ setup time*[1]	t_{MRESS}	25	—	ns	
$\overline{MRES}$ hold time	t_{MRESH}	15	—	ns	
MD1, MD0, FWE setup time	t_{MDS}	20	—	t_{Bcyc}*[4]	Figure 28.6
$\overline{BREQ}$ setup time	t_{BREQS}	$1/2t_{Bcyc}$ + 15	—	ns	Figure 28.9
$\overline{BREQ}$ hold time	t_{BREQH}	$1/2t_{Bcyc}$ + 10	—	ns	
NMI setup time*[1]	t_{NMIS}	60	—	ns	Figure 28.7
NMI hold time	t_{NMIH}	10	—	ns	
IRQ7 to IRQ0 setup time*[1]	t_{IRQS}	35	—	ns	
IRQ7 to IRQ0 hold time	t_{IRQH}	35	—	ns	
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	—	100	ns	Figure 28.8
$\overline{BACK}$ delay time	t_{BACKD}	—	$1/2t_{Bcyc}$ + 20	ns	Figures 28.9, 28.10
Bus tri-state delay time	t_{BOFF}	0	100	ns	
Bus buffer on time	t_{BON}	0	100	ns	

Notes: 1. The $\overline{RES}$, $\overline{MRES}$, NMI, $\overline{BREQ}$, and IRQ7 to IRQ0 signals are asynchronous signals. When the setup time is satisfied, change of signal level is detected at the rising edge of the clock. If not, the detection is delayed until the next rising edge of the clock.

2. In standby mode, t_{RESW} = t_{OSC2} (10 ms).
3. In standby mode, t_{MRESW} = t_{OSC2} (10 ms).
4. t_{Bcyc} indicates external bus clock cycle time (Bϕ = CK).



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

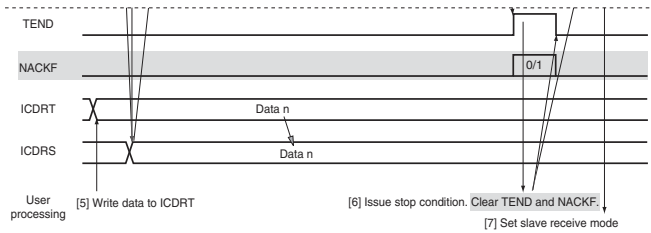
Figure 28.28 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, TRWL = 1 Cycle)

Pin Function		Pin State										
		Reset State					Power-Down State					
		Power-On										
Type	Pin Name	Expansion without ROM 16 bits	Expansion without ROM 32 bits	Expansion with ROM	Single-chip	Manual	Deep Software Standby	Software Standby	Sleep	Bus Master-ship Release	Oscillation Stop Detected	POE Function Used
SCIF	TXD3 (PE5)	Z				O	Z	O*1	O	O	O	O
	TXD3 (PE12)	Z				O	Z	Z (MZIZEL in HCPCR = 0) O*1 (MZIZEL in HCPCR = 1)	O	O	O*6	O
	$\overline{\text{RTS3}}$	Z				O	Z	Z (MZIZEL in HCPCR = 0) O*1 (MZIZEL in HCPCR = 1)	O	O	O*6	O
	$\overline{\text{CTS3}}$	Z				I	Z	Z	I	I	I*6	I
SSU	SSCK	Z				I/O	Z	Z	I/O	I/O	I/O	I/O
	$\overline{\text{SCS}}$	Z				I/O	Z	Z	I/O	I/O	I/O*6	I/O
	SSI	Z				I/O	Z	Z	I/O	I/O	I/O	I/O
	SSO	Z				I/O	Z	Z	I/O	I/O	I/O	I/O
IIC2	SCL	Z				I/O	Z	Z	I/O	I/O	I/O	I/O
	SDA	Z				I/O	Z	Z	I/O	I/O	I/O	I/O
UBC	$\overline{\text{UBCTRG}}$	Z				O	Z	O*1	O	O	O	O
A/D Converter	AN0 to AN7	Z				I	Z	Z	I	I	I	I
	$\overline{\text{ADTRG}}$	Z				I	Z	Z	I	I	I	I
I/O Port	PA0 to PA25	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	PB0 to PB9	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	PC0 to PC15	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	PD0 to PD8, PD10, PD16 to PD23, PD30, PD31	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O

C. Pin States of Bus Related Signals

Table C.1 Pin States of Bus Related Signals (1)

Pin Name		On-chip ROM Space	On-chip RAM Space	On-chip Peripheral Module Space
$\overline{CS0}$ to $\overline{CS8}$		H	H	H
$\overline{CE1A}$, $\overline{CE1B}$, $\overline{CE2A}$, $\overline{CE2B}$		H	H	H
$\overline{BS}$		H	H	H
$\overline{RASU}$, $\overline{RASL}$		H	H	H
$\overline{CASU}$, $\overline{CASL}$		H	H	H
DQMUU		H	H	H
DQMUL		H	H	H
DQMLU		H	H	H
DQMLL		H	H	H
$\overline{AH}$		L	L	L
$\overline{FRAME}$		H	H	H
RDWR	R	H	H	H
	W	—	H	H
$\overline{RD}$	R	H	H	H
	W	—	H	H
$\overline{ICIORD}$	R	H	H	H
	W	—	H	H
$\overline{WRHH}$	R	H	H	H
	W	—	H	H
$\overline{WRHL}$	R	H	H	H
	W	—	H	H
$\overline{WRH}$	R	H	H	H
	W	—	H	H
$\overline{WRL}$	R	H	H	H
	W	—	H	H
$\overline{WE}$	R	H	H	H
	W	—	H	H

Item	Page	Revision (See Manual for Details)
18.4.2 Master Transmit Operation Figure 18.6 Master Transmit Mode Operation Timing (2)	942	Figure amended 
Figure 18.7 Flowchart of Initialization of I²C Bus Interface 2	943	Figure added
18.4.3 Master Receive Operation	944	Description amended The reception procedure and operations in master receive mode are shown below. For operation up to transmission of the 1st frame (slave address + R/$\overline{W}$), see 18.4.2, Master Transmit Operation. ... 3. After the reception of first frame data is completed, the RDRF bit in ICSR is set to 1 at the rise of 9th receive clock pulse. At this time, the receive data is read by reading ICDRR, and RDRF is cleared to 0. The continuous reception is performed by reading ICDRR every time RDRF is set. If reading of ICDRR cannot take place before the rising edge of the 8th clock pulse of SCL, set RCVD in ICCR1 to 1 and perform communication one byte at a time. 4. If next frame is the last receive data, set the RCVD bit in ICCR1 and ACKBT bit in ICIER to 1 before reading ICDRR. This enables the issuance of the stop condition after the next reception. 5. When RDRF is set to 1 at the 9th receive clock pulse, wait until 0 is read from SCLO in ICCR2. Then issue the stop condition. 6. When STOP is set to 1, read the final receive data from ICDRR. 7. Clear RCVD and MST to 0 to return to slave receive mode.