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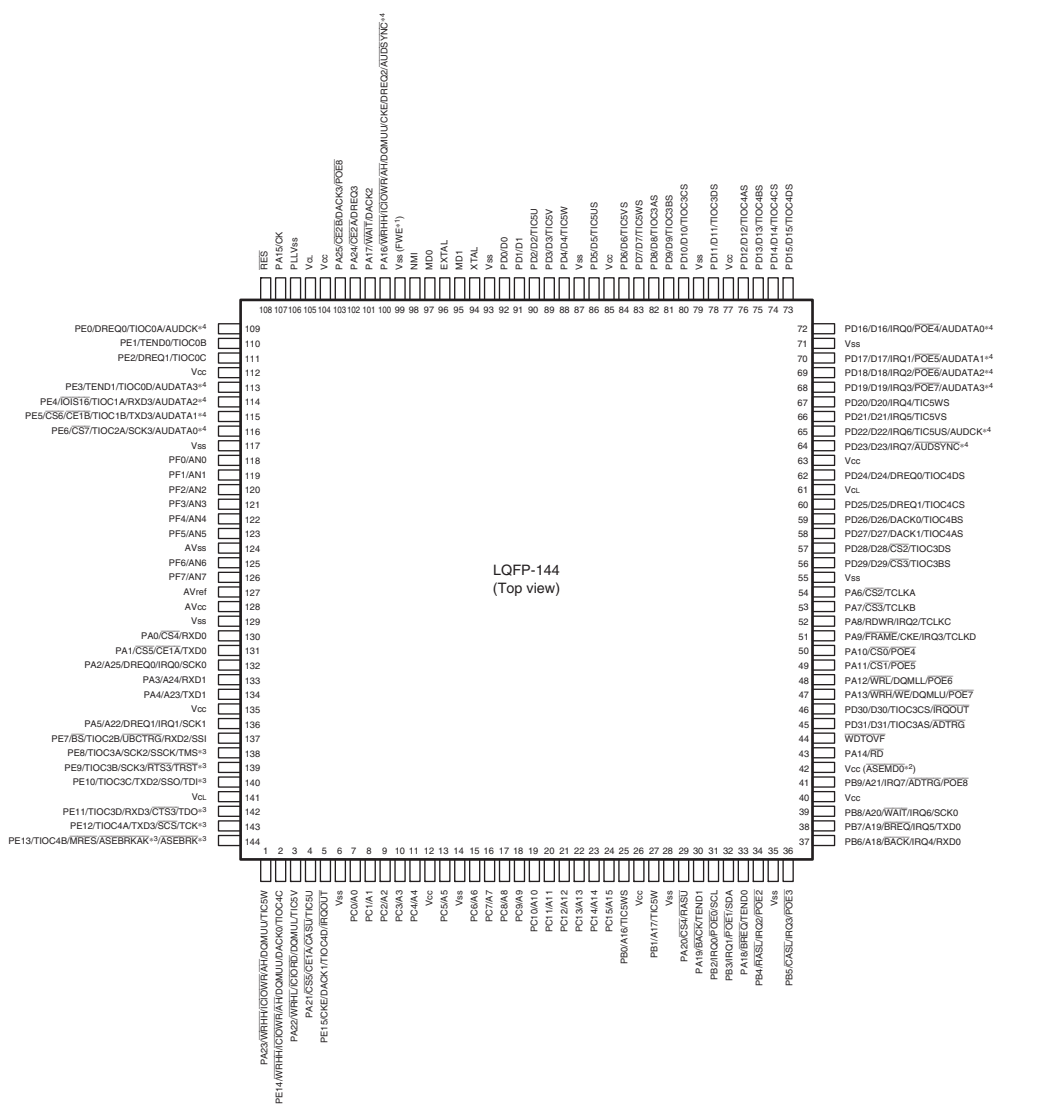
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70835ad80bgv



Notes: 1. This pin is fixed to Vss in the mask ROM and ROM-less versions and is used as the FWE input pin in the F-ZTAT version.
2. This pin is for the E10A emulator. It is fixed to Vcc in the mask ROM and ROM-less versions and is used as the ASEMD0 input pin in the F-ZTAT version.
3. These pin functions are only available in the F-ZTAT version (i.e., they are not available in the mask ROM and ROM-less versions).
4. These pin functions are only available in the F-ZTAT version supporting full functions of E10A (not available in normal F-ZTAT version).

Figure 1.4 Pin Assignments of SH7085

Instruction	Operation	Code	Execution Cycles	T Bit
DMULU.L Rm,Rn	Unsigned operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bits	0011nnnnmmmm0101	2 to 5*	—
DT Rn	Rn - 1 → Rn, if Rn = 0, 1 → T, else 0 → T	0100nnnn00010000	1	Comparison result
EXTS.B Rm,Rn	A byte in Rm is sign-extended → Rn	0110nnnnmmmm1110	1	—
EXTS.W Rm,Rn	A word in Rm is sign-extended → Rn	0110nnnnmmmm1111	1	—
EXTU.B Rm,Rn	A byte in Rm is zero-extended → Rn	0110nnnnmmmm1100	1	—
EXTU.W Rm,Rn	A word in Rm is zero-extended → Rn	0110nnnnmmmm1101	1	—
MAC.L @Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 32 × 32 + 64 → 64 bits	0000nnnnmmmm1111	2 to 5*	—
MAC.W @Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 16 × 16 + 64 → 64 bits	0100nnnnmmmm1111	2 to 4*	—
MUL.L Rm,Rn	Rn × Rm → MACL 32 × 32 → 32 bits	0000nnnnmmmm0111	2 to 5*	—
MULS.W Rm,Rn	Signed operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1111	1 to 3*	—
MULU.W Rm,Rn	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1110	1 to 3*	—
NEG Rm,Rn	0-Rm → Rn	0110nnnnmmmm1011	1	—
NEGC Rm,Rn	0-Rm-T → Rn, Borrow → T	0110nnnnmmmm1010	1	Borrow
SUB Rm,Rn	Rn-Rm → Rn	0011nnnnmmmm1000	1	—
SUBC Rm,Rn	Rn-Rm–T → Rn, Borrow → T	0011nnnnmmmm1010	1	Borrow
SUBV Rm,Rn	Rn-Rm → Rn, Underflow → T	0011nnnnmmmm1011	1	Overflow

Note: * Indicates the number of execution cycles for normal operation.

4.6 Oscillator

Clock pulses can be supplied from a connected crystal resonator or an external clock.

4.6.1 Connecting Crystal Resonator

A crystal resonator can be connected as shown in figure 4.2. Use the damping resistance (Rd) listed in table 4.6. Use a crystal resonator that has a resonance frequency of 5 to 12.5 MHz. It is recommended to consult the crystal resonator manufacturer concerning the compatibility of the crystal resonator and the LSI.

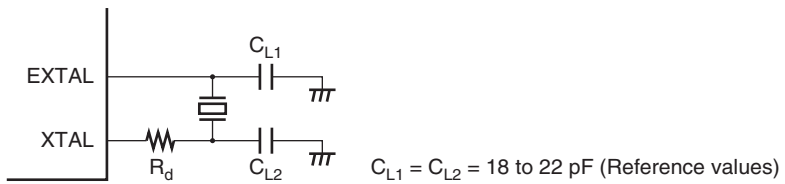


Figure 4.2 Connection of Crystal Resonator (Example)

Table 4.6 Damping Resistance Values (Reference Values)

Frequency (MHz)	5	8	10	12.5
Rd (Ω)(Reference values)	500	200	0	0

Figure 4.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator with the characteristics listed in table 4.7.

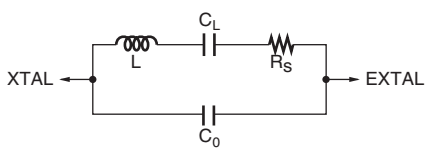


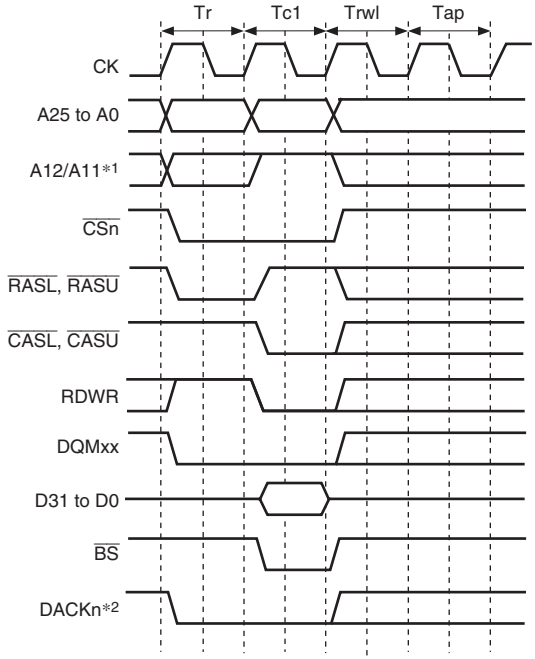
Figure 4.3 Crystal Resonator Equivalent Circuit

Table 4.7 Crystal Resonator Characteristics

Frequency (MHz)	5	8	10	12.5
Rs Max. (Ω) (Reference values)	120	80	60	50
C_0 Max. (pF) (Reference values)	7	7	7	7

Single Write: A write access ends in one cycle when the data bus width is larger than or equal to access size. This is called single write.

Figure 9.22 shows the single write basic timing.



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.22 Single Write Basic Timing (Auto-Precharge)

Bank Active: The SDRAM bank function is used to support high-speed accesses to the same row address. When the BACTV bit in SDCR is 1, accesses are performed using commands without auto-precharge (READ or WRIT). This function is called bank-active function. This function is valid only for area 3. When area 3 is set to bank-active mode, area 2 should be set to normal space or SRAM with byte selection. When areas 2 and 3 are both set to SDRAM, auto-precharge mode must be set.

In this case, precharging is not performed when the access ends. When accessing the same row address in the same bank, it is possible to issue the READ or WRIT command immediately, without issuing an ACTV command. As SDRAM is internally divided into several banks, it is possible to activate one row address in each bank. If the next access is to a different row address, a PRE command is first issued to precharge the relevant bank, then when precharging is completed,

(2) Transfer from the normal space interface to the external device with DACK

BSC Register Setting*4		Minimum Number of Idle Cycles	
CSnWCR.WM Setting	CSnBCR Idle Setting	When Access Size is Greater than Bus Width*1	When Access Size is Less than or Equal to Bus Width*2
1	0	0	2
0	0	1	3
1	1	1	2
0	1	1	3
1	2	2	2
0	2	2	3
1	4	4	4
0	4	4	4

Notes: DMAC is driven by Bϕ. The minimum number of idle cycles is not affected by changing a clock ratio.

1. Minimum number of idle cycles between the word access to address 0 and the word access to address 2 in the 32-bit access with a 16-bit bus width,
minimum number of idle cycles between the byte access to address 0 and the byte access to address 1 in the 16-bit access with an 8-bit bus width,
minimum number of idle cycles between the byte accesses to address 0, to address 1, to address 2, and to address 3 in the 32-bit access with an 8-bit bus width, and
minimum number of idle cycles between consecutive accesses in 16-byte transfer.
2. Other than the above cases.
3. For single address mode transfer from the external device with DACK to the normal space interface, the minimum number of idle cycles is not affected by the IWW, IWRWD, IWRWS, IWRRD, and IWRRS bits in CSnBCR.
4. For single address mode transfer from the normal space interface to the external device with DACK, the minimum number of idle cycles is not affected by the DMAIWA and DMAIW bits in CMNCR.
5. When the HW[1:0] in the CSnWCR is set to specify 2.5 cycles or more, the number of idle cycles will be 0.

Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Reset-Synchronized PWM Mode: Figure 11.152 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

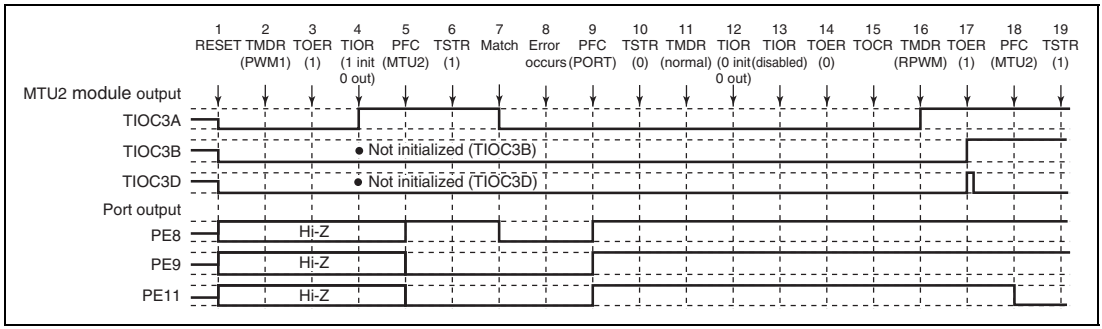


Figure 11.152 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

1 to 14 are the same as in figure 11.151.

15. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
16. Set reset-synchronized PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

Table 15.7 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (Clock Synchronous Mode)

	Discontinuous Transmission/Reception			Continuous Transmission/Reception		
		Settings			Settings	
Pϕ (MHz)	Maximum Bit Rate (bits/s)	n	N	Maximum Bit Rate (bits/s)	n	N
10	2500000	0	0	1250000	0	1
12	3000000	0	0	1500000	0	1
14	3500000	0	0	1750000	0	1
16	4000000	0	0	2000000	0	1
18	4500000	0	0	2250000	0	1
20	5000000	0	0	2500000	0	1
22	5500000	0	0	2750000	0	1
24	6000000	0	0	3000000	0	1
26	6500000	0	0	3250000	0	1
28	7000000	0	0	3500000	0	1
30	7500000	0	0	3750000	0	1
32	8000000	0	0	4000000	0	1
34	8500000	0	0	4250000	0	1
36	9000000	0	0	4500000	0	1
38	9500000	0	0	4750000	0	1
40	10000000	0	0	5000000	0	1

Bit	Bit Name	Initial Value	R/W	Description
4	NAKIE	0	R/W	NACK Receive Interrupt Enable NAKIE enables or disables the NACK detection and arbitration lost/overrun error interrupt request (IINAKI) when the NACKF or AL/OVE bit in ICSR is set to 1. IINAKI can be canceled by clearing the NACKF, AL/OVE, or NAKIE bit to 0. 0: NACK detection and arbitration lost/overrun error interrupt request (IINAKI) is disabled. 1: NACK detection and arbitration lost/overrun error interrupt request (IINAKI) is enabled.
3	STIE	0	R/W	Stop Condition Detection Interrupt Enable This bit enables or disables the stop condition detection interrupt request (IISTPI) when the STOP bit in ICSR is set. 0: Stop condition detection interrupt request (IISTPI) is disabled. 1: Stop condition detection interrupt request (IISTPI) is enabled.
2	ACKE	0	R/W	Acknowledge Bit Judgment Select 0: The value of the receive acknowledge bit is ignored, and continuous transfer is performed. 1: If the receive acknowledge bit is 1, continuous transfer is halted.
1	ACKBR	0	R	Receive Acknowledge In transmit mode, this bit stores the acknowledge data that are returned by the receive device. This bit cannot be modified. This bit can be canceled by setting the BBSY bit in ICCR2 to 1. 0: Receive acknowledge = 0 1: Receive acknowledge = 1
0	ACKBT	0	R/W	Transmit Acknowledge In receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 is sent at the acknowledge timing. 1: 1 is sent at the acknowledge timing.

20.5.3 Conflict between Word-Write and Count-Up Processes of CMCNT

Even when the count-up occurs in the T2 cycle while writing to CMCNT counter in words, the writing has priority over the count-up. In this case, the count-up is not performed. Figure 20.6 shows the timing to write to CMCNT in words.

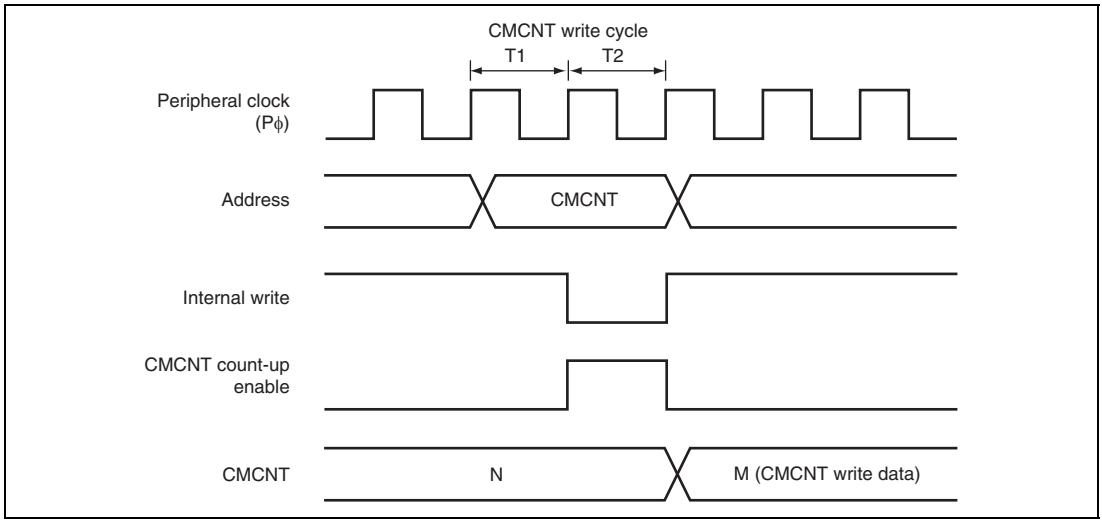


Figure 20.6 Conflict between Word-Write and Count-Up Processes of CMCNT

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA16 I/O (port)	WRHH/ICIOWR/AH/ DQMUU output (BSC)	CKE output (BSC)	DREQ2 input (DMAC)	AUDSYNC output (AUD) *
	PA17 I/O (port)	WAIT input (BSC)	DACK2 output (DMAC)	—	—
	PA18 I/O (port)	BREQ input (BSC)	TEND0 output (DMAC)	—	—
	PA19 I/O (port)	BACK output (BSC)	TEND1 output (DMAC)	—	—
	PA20 I/O (port)	CS4 output (BSC)	RASU output (BSC)	—	—
	PA21 I/O (port)	CS5/CE1A output (BSC)	CASU output (BSC)	TIC5U input (MTU2)	—
	PA22 I/O (port)	WRHL/ICIORD /DQMUL output (BSC)	TIC5V input (MTU2)	—	—
	PA23 I/O (port)	WRHH/ICIOWR/AH/ DQMUU output (BSC)	TIC5W input (MTU2)	—	—
	PA24 I/O (port)	CE2A output (BSC)	DREQ3 input (DMAC)	—	—
	PA25 I/O (port)	CE2B output (BSC)	DACK3 output (DMAC)	POE8 input (POE)	—

Note: * Only in F-ZTAT version supporting full functions of E10A.

Table 21.4 SH7086 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA0 I/O (port)	CS4 output (BSC)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	CS5/CE1A output (BSC)	TXD0 output (SCI)	—	—
	PA2 I/O (port)	A25 output (BSC)	DREQ0 input (DMAC)	IRQ0 input (INTC)	SCK0 I/O (SCI)
	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA6 I/O (port)	CS2 output (BSC)	TCLKA input (MTU2)	—	—
	PA7 I/O (port)	CS3 output (BSC)	TCLKB input (MTU2)	—	—
	PA8 I/O (port)	RDWR output (BSC)	IRQ2 input (INTC)	TCLKC input (MTU2)	—
	PA9 I/O (port)	FRAME output (BSC)	CKE output (BSC)	IRQ3 input (INTC)	TCLKD input (MTU2)
	PA10 I/O (port)	CS0 output (BSC)	POE4 input (POE)	—	—
	PA11 I/O (port)	CS1 output (BSC)	POE5 input (POE)	—	—

	Pin Name			
	On-Chip ROM Disabled (MCU Mode 0)		On-Chip ROM Disabled (MCU Mode 1)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
104	PE6	PE6/$\overline{CS7}$/TIOC2A/SCK3	PE6	PE6/$\overline{CS7}$/TIOC2A/SCK3
105	PE7	PE7/$\overline{BS}$/TIOC2B/$\overline{UBCTRG}$ /RXD2/SSI	PE7	PE7/$\overline{BS}$/TIOC2B/$\overline{UBCTRG}$ /RXD2/SSI
106	PE8	PE8/TIOC3A/SCK2/SSCK	PE8	PE8/TIOC3A/SCK2/SSCK
107	PE9	PE9/TIOC3B/SCK3/$\overline{RTS3}$	PE9	PE9/TIOC3B/SCK3/$\overline{RTS3}$
108	PE10	PE10/TIOC3C/TXD2/SSO	PE10	PE10/TIOC3C/TXD2/SSO
110	PE11	PE11/TIOC3D/RXD3/$\overline{CTS3}$	PE11	PE11/TIOC3D/RXD3/$\overline{CTS3}$
111	PE12	PE12/TIOC4A/TXD3/$\overline{SCS}$	PE12	PE12/TIOC4A/TXD3/$\overline{SCS}$
112	PE13	PE13/TIOC4B/$\overline{MRES}$	PE13	PE13/TIOC4B/$\overline{MRES}$
1	PE14	PE14/$\overline{AH}$/DACK0/TIOC4C	PE14	PE14/$\overline{AH}$/DACK0/TIOC4C
2	PE15	PE15/CKE/DACK1/TIOC4D /$\overline{IRQOUT}$	PE15	PE15/CKE/DACK1/TIOC4D /$\overline{IRQOUT}$
91	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0
92	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1
93	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2
94	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3
95	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4
96	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5
98	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6
99	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{TRST}$, TDI, TDO, TCK, and $\overline{ASEBRKAK}$/$\overline{ASEBRK}$ when using the E10A (in $\overline{ASEMD0}$ = low).

2. Only in F-ZTAT version supporting full functions of E10A. Fixed as AUD pins when using the AUD function of the E10A.

Bit	Bit Name	Initial Value	R/W	Description
1	PE0MD1	0	R/W	PE0 Mode
0	PE0MD0	0	R/W	Select the function of the PE0/DREQ0/TIOC0A/TMS pin. Fixed to TMS input when using E10A (in $\overline{\text{ASEMD0}}$ = low). 00: PE0 I/O (port) 01: TIOC0A I/O (MTU2) 10: DREQ0 input (DMAC) Other than above: Setting prohibited

Note: * This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

SH7084:

- Port E Control Registers H2 and H1 (PECRH2 and PECRH1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Port E Control Register L4 (PECRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PE15 MD2	PE15 MD1	PE15 MD0	-	PE14 MD2	PE14 MD1	PE14 MD0	-	-	PE13 MD1	PE13 MD0	-	PE12 MD2	PE12 MD1	PE12 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- PAPRH (SH7084)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA17PR	PA16PR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PA17PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
0	PA16PR	Pin state	R	

- PAPRH (SH7085)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PA25PR	PA24PR	PA23PR	PA22PR	PA21PR	PA20PR	PA19PR	PA18PR	PA17PR	PA16PR
Initial value:	0	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PA25PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
8	PA24PR	Pin state	R	
7	PA23PR	Pin state	R	
6	PA22PR	Pin state	R	
5	PA21PR	Pin state	R	
4	PA20PR	Pin state	R	
3	PA19PR	Pin state	R	
2	PA18PR	Pin state	R	
1	PA17PR	Pin state	R	
0	PA16PR	Pin state	R	

- PCPRH (SH7086)

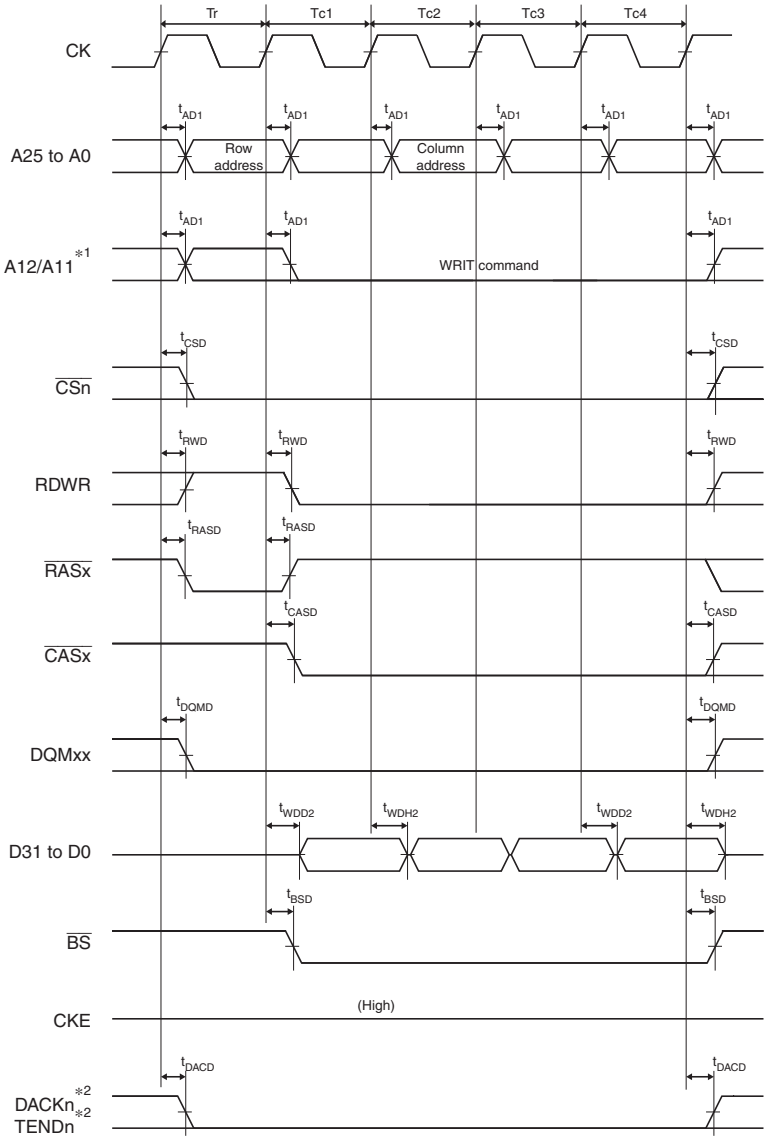
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PC25PR	PC24PR	PC23PR	PC22PR	PC21PR	PC20PR	PC19PR	PC18PR	-	-
Initial value:	0	0	0	0	0	0	*	*	*	*	*	*	*	*	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PC25PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
8	PC24PR	Pin state	R	
7	PC23PR	Pin state	R	
6	PC22PR	Pin state	R	
5	PC21PR	Pin state	R	
4	PC20PR	Pin state	R	
3	PC19PR	Pin state	R	
2	PC18PR	Pin state	R	
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	SCO	0	(R)/W	Source Program Copy Operation Requests the on-chip programming/erasing program to be downloaded to the on-chip RAM. When this bit is set to 1, the on-chip program which is selected by FPCS/FECS is automatically downloaded in the on-chip RAM area specified by FTDAR. In order to set this bit to 1, RAM emulation state must be canceled, H'A5 must be written to FKEY, and this operation must be in the on-chip RAM. Four NOP instructions must be executed immediately after setting this bit to 1. For interrupts during download, see section 23.8.2, Interrupts during Programming/Erasing. For the download time, see section 23.8.3, Other Notes. Since this bit is cleared to 0 when download is completed, this bit cannot be read as 1. Download by setting the SCO bit to 1 requires a special interrupt processing that performs bank switching to the on-chip program storage area. Therefore, before issuing a download request (SCO = 1), set VBR to H'84000000. Otherwise, the CPU gets out of control. Once download end is confirmed, VBR can be changed to any other value. The mode in which the FWE pin is high must be used when using the SCO function. 0: Download of the on-chip programming/erasing program to the on-chip RAM is not executed. [Clearing condition] When download is completed 1: Request that the on-chip programming/erasing program is downloaded to the on-chip RAM is generated [Setting conditions] When all of the following conditions are satisfied and 1 is written to this bit • FKEY is written to H'A5 • During execution in the on-chip RAM • Not in RAM emulation mode (RAMS in RAMCR = 0)

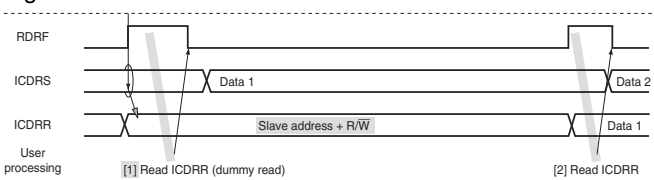
Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
Port C I/O register H	PCIORH	16	H'FFFFD204	PFC	8, 16, 32	Pϕ reference	16 bits
Port C I/O register L	PCIORL	16	H'FFFFD206		8, 16	B:2	
Port C control register H3	PCCRH3	16	H'FFFFD20A		8, 16	W:2	
Port C control register H2	PCCRH2	16	H'FFFFD20C		8, 16, 32	L:4	
Port C control register H1	PCCRH1	16	H'FFFFD20E		8, 16		
Port C control register L4	PCCRL4	16	H'FFFFD210		8, 16, 32		
Port C control register L3	PCCRL3	16	H'FFFFD212		8, 16		
Port C control register L2	PCCRL2	16	H'FFFFD214		8, 16, 32		
Port C control register L1	PCCRL1	16	H'FFFFD216		8, 16		
Port C port register H	PCPRH	16	H'FFFFD21C	I/O	8, 16, 32		
Port C port register L	PCPRL	16	H'FFFFD21E		8, 16		
Port D data register H	PDDRH	16	H'FFFFD280		8, 16, 32		
Port D data register L	PDDRL	16	H'FFFFD282		8, 16		
Port D I/O register H	PDIORH	16	H'FFFFD284	PFC	8, 16, 32		
Port D I/O register L	PDIORL	16	H'FFFFD286		8, 16		
Port D control register H4	PDCRH4	16	H'FFFFD288		8, 16, 32		
Port D control register H3	PDCRH3	16	H'FFFFD28A		8, 16		
Port D control register H2	PDCRH2	16	H'FFFFD28C		8, 16, 32		
Port D control register H1	PDCRH1	16	H'FFFFD28E		8, 16		
Port D control register L4	PDCRL4	16	H'FFFFD290		8, 16, 32		
Port D control register L3	PDCRL3	16	H'FFFFD292		8, 16		
Port D control register L2	PDCRL2	16	H'FFFFD294		8, 16, 32		
Port D control register L1	PDCRL1	16	H'FFFFD296		8, 16		
Port D port register H	PDPRH	16	H'FFFFD29C	I/O	8, 16, 32		
Port D port register L	PDPRL	16	H'FFFFD29E		8, 16		
Port E data register H	PEDRH	16	H'FFFFD300		8, 16, 32		
Port E data register L	PEDRL	16	H'FFFFD302		8, 16		
Port E I/O register H	PEIORH	16	H'FFFFD304	PFC	8, 16, 32		
Port E I/O register L	PEIORL	16	H'FFFFD306		8, 16		
Port E control register H2	PECRH2	16	H'FFFFD30C		8, 16, 32		
Port E control register H1	PECRH1	16	H'FFFFD30E		8, 16		

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Deep Software Standby	Module Standby	Sleep	Module
PACRL2	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PACRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PAPRH	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PAPRL	Initialized	Retained	Retained	Initialized	—	Retained	
PBDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PBIORL	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PBCRL3	Initialized	Retained	Retained	Initialized	—	Retained	
PBCRL2	Initialized	Retained	Retained	Initialized	—	Retained	
PBCRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PBPRL	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PCDRH	Initialized	Retained	Retained	Initialized	—	Retained	
PCDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PCIORH	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PCIORL	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH3	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH2	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH1	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL4	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL3	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL2	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PCPRH	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PCPRL	Initialized	Retained	Retained	Initialized	—	Retained	
PDDRH	Initialized	Retained	Retained	Initialized	—	Retained	
PDDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PDIORH	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PDIORL	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH4	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH3	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH2	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH1	Initialized	Retained	Retained	Initialized	—	Retained	



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 28.35 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: ACT + WRITE Commands, WTRCD = 0 Cycle, TRWL = 0 Cycle)

Item	Page	Revision (See Manual for Details)
18.4.5 Slave Receive Operation	950	Description amended The reception procedure and operations in slave receive mode are described below. For operation up to reception of the 1st frame (slave address + R/$\overline{W}$), see 18.4.4, Slave Transmit Operation. 1. Perform a dummy read of ICDRR. (The read data indicates slave address + R/$\overline{W}$, and is therefore unnecessary.) The slave device outputs to SDA the level indicated by the setting of ACKBT in ICIER at the 9th clock pulse of the receive clock. 2. After reception of one frame of data finishes, RDRF in ICSR is set to 1 at the rising edge of the 9th receive clock pulse. At this time, the received data can be read by reading ICDRR, and RDRF is cleared to 0 simultaneously. Continuous receive operation can be accomplished by reading ICDRR each time RDRF is set to 1. If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read. 3. If the next receive operation is the final frame, set ACKBT in ICIER to 1 before reading ICDRR. 4. When RDRF in ICSR is set to 1, read the final receive data from ICDRR.
Figure 18.12 Slave Receive Mode Operation Timing (1)		Figure amended 
Figure 18.13 Slave Receive Mode Operation Timing (2)	951	Figure amended