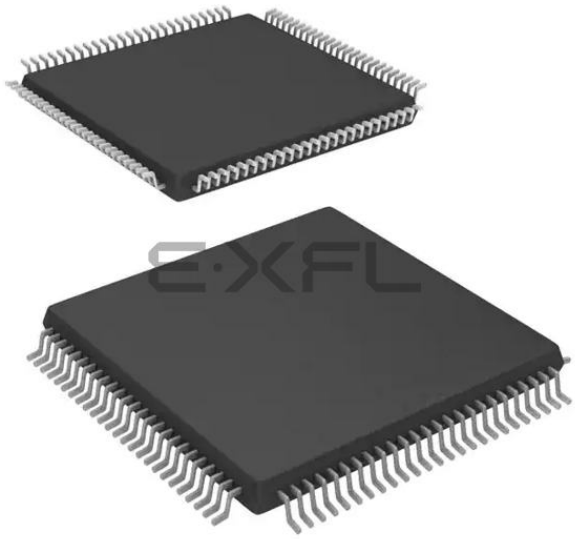
Renesas Electronics America Inc - DF70835AD80FTV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70835ad80ftv

2.2.3 System Registers

There are four 32-bit system registers, designated two multiply and accumulate registers (MACH and MACL), a procedure register (PR), and program counter (PC).

- Multiply and accumulate registers (MACH and MACL)
  This register stores the results of multiplication and multiply-and-accumulate operation.
- Procedure register (PR)
  This register stores the return-destination address from subroutine procedures.
- Program counter (PC)
  The PC indicates the point which is four bytes (two instructions) after the current execution instruction.

2.2.4 Initial Values of Registers

Table 2.1 lists the initial values of registers after a reset.

Table 2.1 Initial Values of Registers

Type of register	Register	Default
General register	R0 to R14	Undefined
	R15 (SP)	SP value set in the exception handling vector table
Control register	SR	I3 to I0: 1111 (H'F) Reserved bits: 0 Other bits: Undefined
	GBR	Undefined
	VBR	H'00000000
System register	MACH, MACL, PR	Undefined
	PC	PC value set in the exception handling vector table

Table 8.7 Register Function in Repeat Transfer Mode

		Written Back Value	
Register	**Function**	**CRAL is not 1**	**CRAL is 1**
SAR	Source address	Incremented/decremented/fixed*	DTS = 0: Incremented/ decremented/fixed* DTS = 1: SAR initial value
DAR	Destination address	Incremented/decremented/fixed*	DTS = 0: DAR initial value DTS = 1: Incremented/ decremented/fixed*
CRAH	Transfer count storage	CRAH	CRAH
CRAL	Transfer count A	CRAL – 1	CRAH
CRB	Transfer count B	Not updated	Not updated

Note: * Transfer information writeback is skipped.

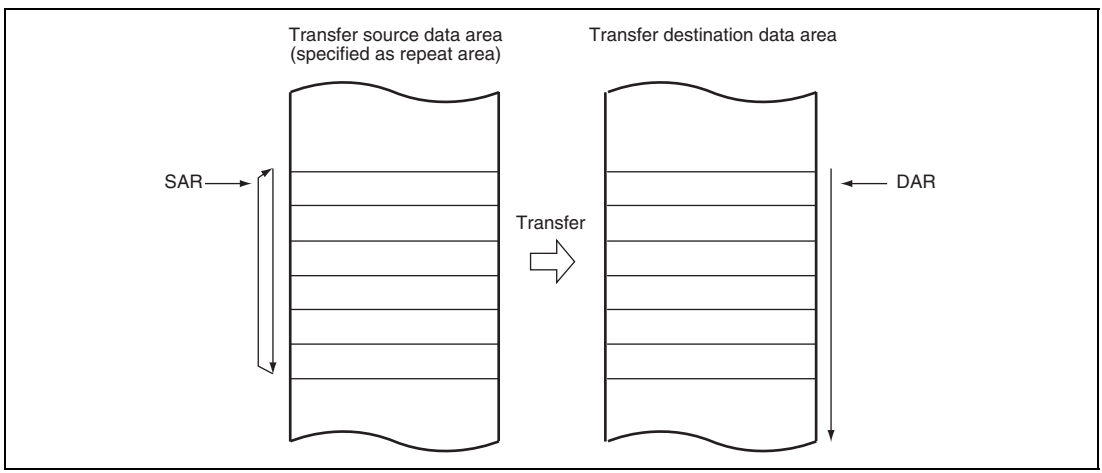

Figure 8.7 Memory Map in Repeat Transfer Mode (When Transfer Source Is Specified as Repeat Area)

3. For the second transfer, set repeat transfer mode (with the source side as the repeat area) for re-setting the transfer destination address for the first data transfer. Use the upper eight bits of DAR in the first transfer information area as the transfer destination. Set CHNE = DISEL = 0. If the above input buffer is specified as H'200000 to H'21FFFF, set the transfer counter to 2.
4. Execute the first data transfer 65536 times by means of interrupts. When the transfer counter for the first data transfer reaches 0, the second data transfer is started. Set the upper eight bits of the transfer destination address for the first data transfer to H'21. The lower 16 bits of the transfer destination address of the first data transfer and the transfer counter are H'0000.
5. Next, execute the first data transfer the 65536 times specified for the first data transfer by means of interrupts. When the transfer counter for the first data transfer reaches 0, the second data transfer is started. Set the upper eight bits of the transfer destination address for the first data transfer to H'20. The lower 16 bits of the transfer destination address of the first data transfer and the transfer counter are H'0000.
6. Steps 4 and 5 are repeated endlessly. As repeat mode is specified for the second data transfer, no interrupt request is sent to the CPU.

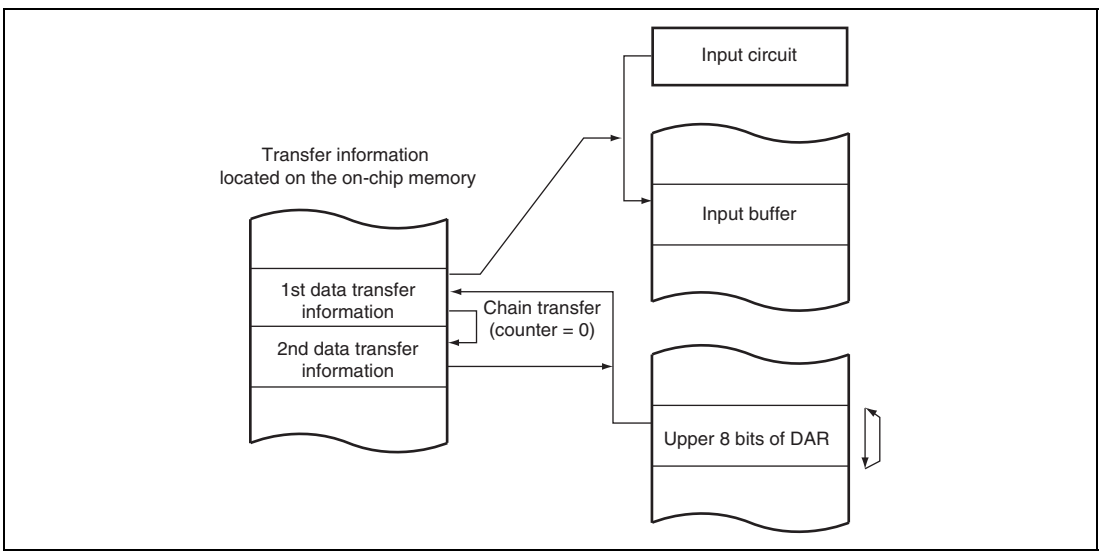

Figure 8.19 Chain Transfer when Counter = 0

Bit	Bit Name	Initial Value	R/W	Description
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait is valid 1: External wait is ignored
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(7) Burst ROM (Clock Synchronous)

- CS0WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	BW[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	W[3:0]				WM	-	-	-	-	-	-
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	BW[1:0]	00	R/W	Number of Burst Wait Cycles Specify the number of wait cycles to be inserted in the second or subsequent access cycles in burst access. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3 cycles

Table 9.23 Relationship between BSZ[1:0], A2ROW[1:0]/A3ROW[1:0], A2COL[1:0]/A3COL[1:0], and Address Multiplex Output (4)-1

Setting				
BSZ[1:0]	**A2ROW[1:0]/ A3ROW[1:0]**	**A2COL[1:0]/ A3COL[1:0]**		
10 (16 bits)	**00 (11 bits)**	**00 (8 bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23	A15		
A14	A22	A14		
A13	A21*2	A21*2	A12 (BA1)	Specifies bank
A12	A20*2	A20*2	A11 (BA0)	
A11	A19	L/H*1	A10/AP	Specifies address/precharge
A10	A18	A10	A9	Address
A9	A17	A9	A8	
A8	A16	A8	A7	
A7	A15	A7	A6	
A6	A14	A6	A5	
A5	A13	A5	A4	
A4	A12	A4	A3	
A3	A11	A3	A2	
A2	A10	A2	A1	
A1	A9	A1	A0	
A0	A8	A0		Unused
Example of connected memory				
16-Mbit product (512 kwords × 16 bits × 2 banks, column 8 bits product): 1				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
2. Bank address specification

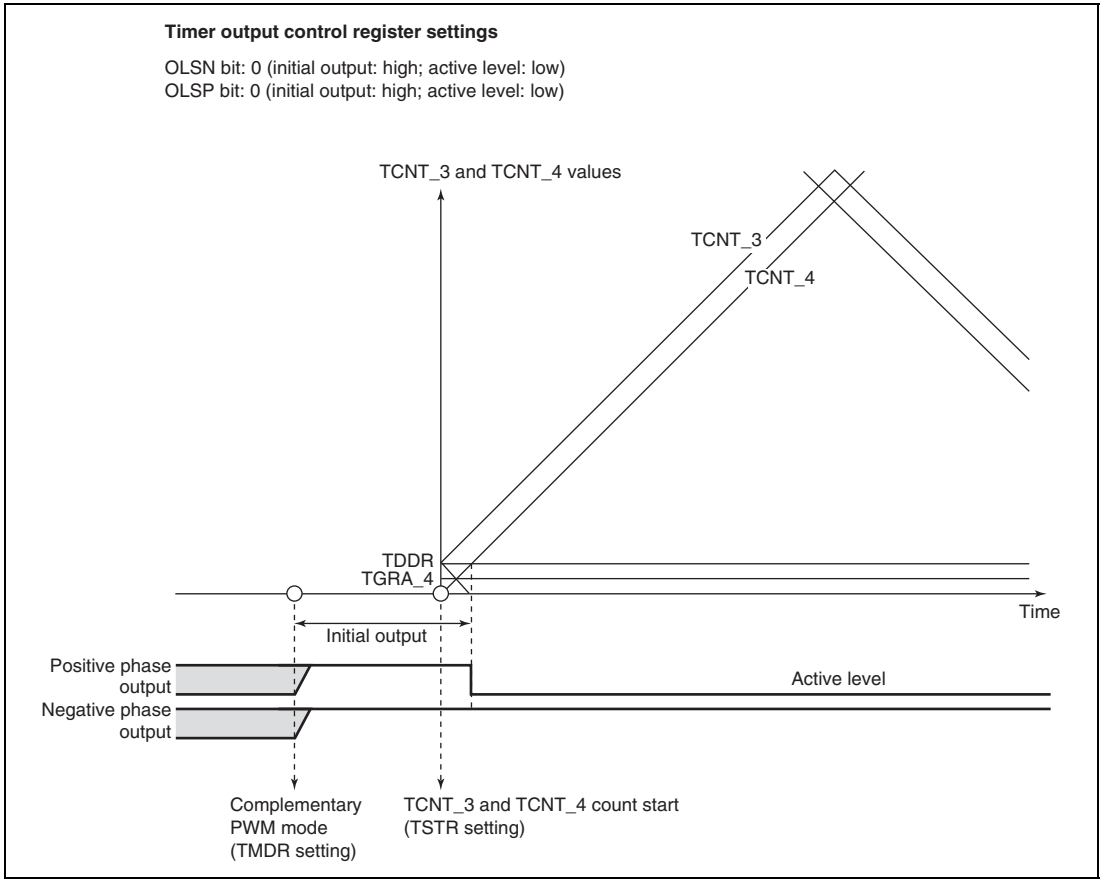

Figure 11.45 Example of Initial Output in Complementary PWM Mode (2)

(b) Examples of Synchronous Counter Start Operation

Figures 11.84 (1), 11.84 (2), 11.84 (3), and 11.84 (4) show examples of synchronous counter start operation when the clock frequency ratio between the MTU2 and MTU2S is 1:1, 1:2, 1:3, and 1:4, respectively.

In these examples, the count clock settings are MPϕ/1 (MTU2) and MIϕ/1 (MTU2S).

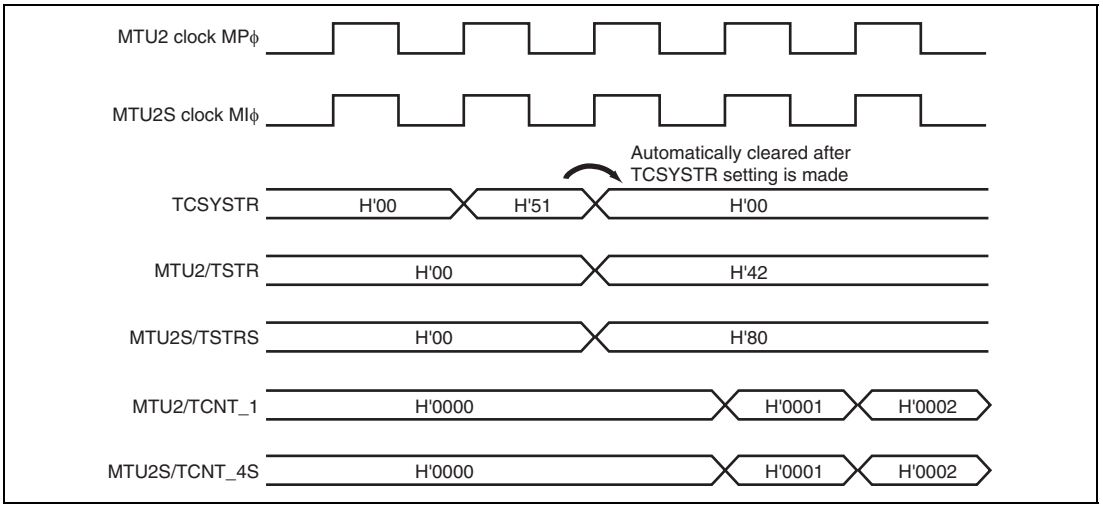

Figure 11.84 (1) Example of Synchronous Counter Start Operation (MTU2-to-MTU2S Clock Frequency Ratio = 1:1)

(4) Timing for Counter Clearing by Compare Match/Input Capture

Figures 11.100 and 11.101 show the timing when counter clearing on compare match is specified, and figure 11.102 shows the timing when counter clearing on input capture is specified.

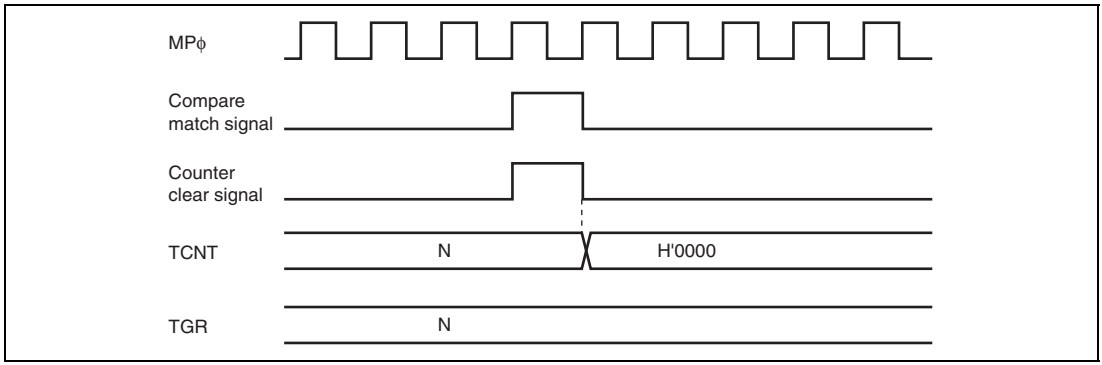

Figure 11.100 Counter Clear Timing (Compare Match) (Channels 0 to 4)

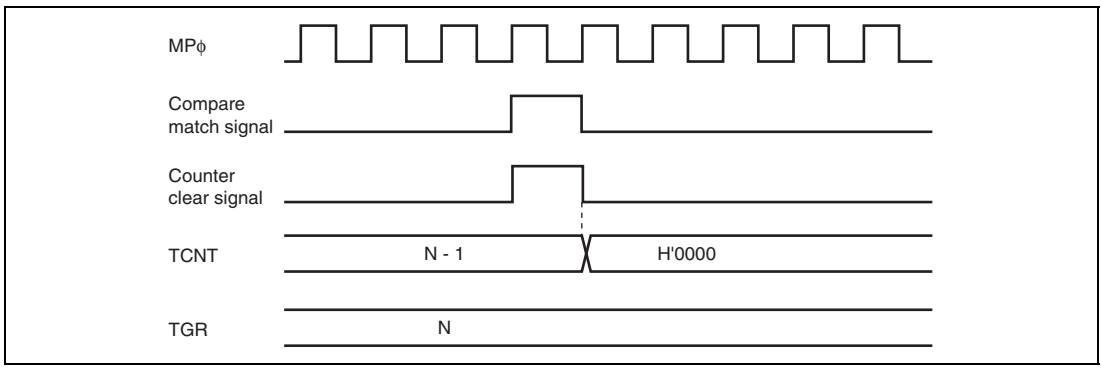

Figure 11.101 Counter Clear Timing (Compare Match) (Channel 5)

(3) TCFV Flag/TCFU Flag Setting Timing

Figure 11.113 shows the timing for setting of the TCFV flag in TSR on overflow, and TCIV interrupt request signal timing.

Figure 11.114 shows the timing for setting of the TCFU flag in TSR on underflow, and TCIU interrupt request signal timing.

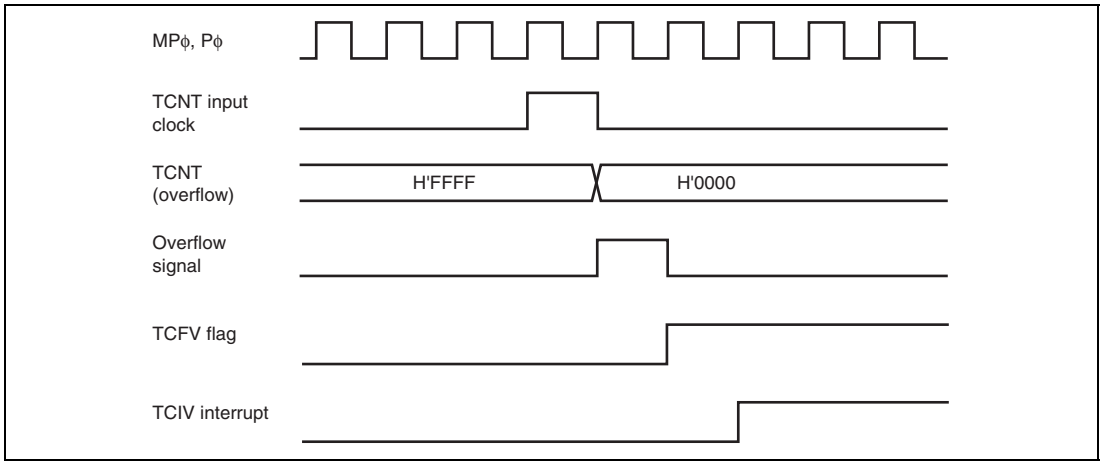

Figure 11.113 TCIV Interrupt Setting Timing

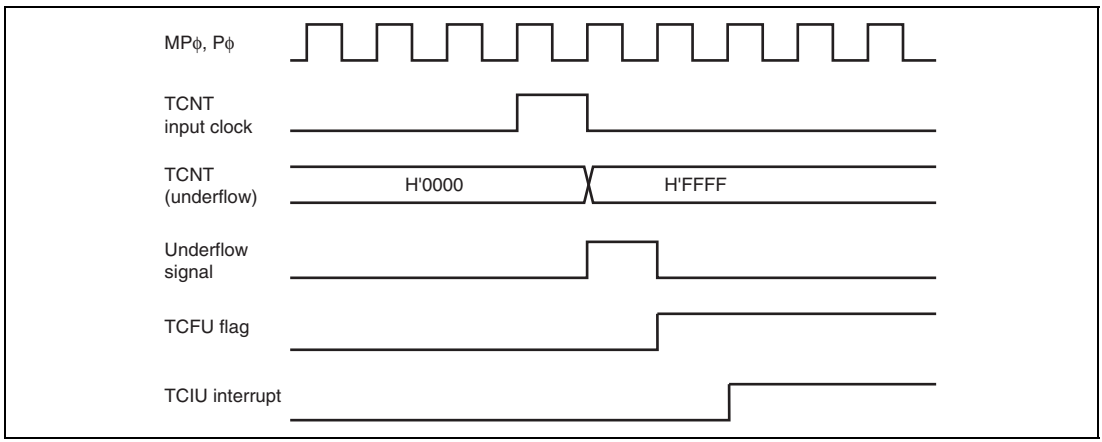

Figure 11.114 TCIU Interrupt Setting Timing

Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Normal Mode: Figure 11.161 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in normal mode after re-setting.

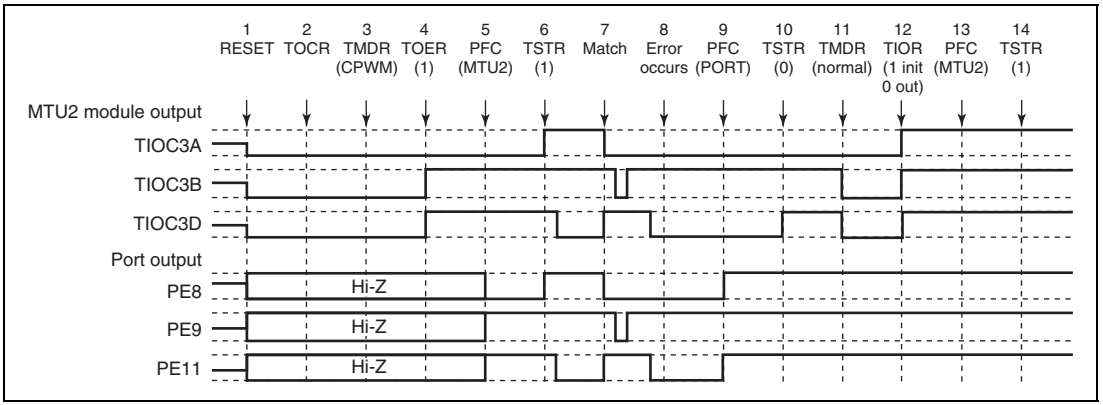

Figure 11.161 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
3. Set complementary PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. The complementary PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU2 output becomes the complementary PWM output initial value.)
11. Set normal mode. (MTU2 output goes low.)
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

15.3.7 Serial Status Register (SCSSR)

SCSSR is an 8-bit register that contains status flags to indicate the SCI operating state.

The CPU can always read and write to SCSSR, but cannot write 1 to status flags TDRE, RDRF, ORER, PER, and FER. These flags can be cleared to 0 only after 1 is read from the flags. The TEND flag is a read-only bit and cannot be modified.

Bit:	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value:	1	0	0	0	0	1	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Indicates whether data has been transferred from the transmit data register (SCTDR) to the transmit shift register (SCTSR) and SCTDR has become ready to be written with next serial transmit data. 0: Indicates that SCTDR holds valid transmit data [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC is activated by a TXI interrupt and transmit data is written to SCTDR • When the DTC is activated by a TXI interrupt and transmit data is transferred to SCTDR while the DISEL bit of MRB in the DTC is 0 (except when the transfer counter value of the DTC is H'0000) 1: Indicates that SCTDR does not hold valid transmit data [Setting conditions] • By a power-on reset or in standby mode • When the TE bit in SCSCR is 0 • When data is transferred from SCTDR to SCTSR and data can be written to SCTDR

Transmitting Serial Data (Clock Synchronous Mode): Figure 16.13 shows a sample flowchart for transmitting serial data.

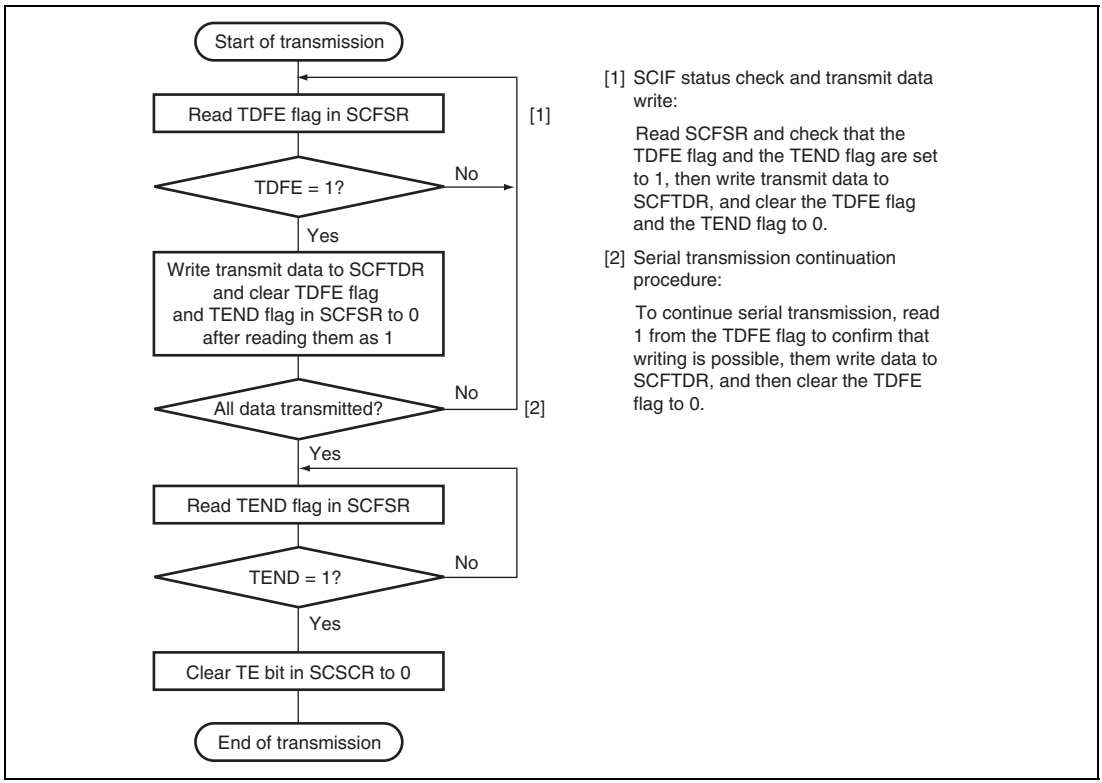

Figure 16.13 Sample Flowchart for Transmitting Serial Data

Bit	Bit Name	Initial Value	R/W	Description
5	PD29MD1	0	R/W	PD29 Mode
4	PD29MD0	0*[1]	R/W	Select the function of the PD29/D29/$\overline{CS3}$/TIOC3BS pin. 00: PD29 I/O (port) 01: D29 I/O (BSC)*[2] 10: $\overline{CS3}$ output (BSC)*[2] 11: TIOC3BS I/O (MTU2S)
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PD28MD1	0	R/W	PD28 Mode
0	PD28MD0	0*[1]	R/W	Select the function of the PD28/D28/$\overline{CS2}$/TIOC3DS pin. 00: PD28 I/O (port) 01: D28 I/O (BSC)*[2] 10: $\overline{CS2}$ output (BSC)*[2] 11: TIOC3DS I/O (MTU2S)

Notes: 1. The initial value is 1 in the on-chip ROM disabled 32-bit external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

- Port D Control Register H3 (PDCRH3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PD27 MD1	PD27 MD0	-	-	PD26 MD1	PD26 MD0	-	-	PD25 MD1	PD25 MD0	-	-	PD24 MD1	PD24 MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Note: * The initial value is 1 in the on-chip ROM disabled 32-bit external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

21.2 Usage Notes

1. In this LSI, the same function is available as a multiplexed function on multiple pins. This approach is intended to increase the number of selectable pin functions and to allow the easier design of boards. If two or more pins are specified for one function, however, there are two cautions shown below.
   — When the pin function is input
   Signals input to several pins are formed as one signal through OR or AND logic and the signal is transmitted into the LSI. Therefore, a signal that differs from the input signals may be transmitted to the LSI depending on the input signals in other pins that have the same functions. Table 21.22 shows the transmit forms of input functions allocated to several pins. When using one of the functions shown below in multiple pins, use it with care of signal polarity considering the transmit forms.

Table 21.22 Transmit Forms of Input Functions Allocated to Multiple Pins

OR Type	AND Type
SCK0, SCK3, RXD0, RXD3, TIOC3AS to TIOC3DS, TIOC4AS to TIOC4DS, TIC5U, TIC5V, TIC5W, TIC5US, TIC5VS, TIC5WS	IRQ0 to IRQ7, DREQ0, DREQ1, $\overline{\text{BREQ}}$, $\overline{\text{WAIT}}$, $\overline{\text{ADTRG}}$, $\overline{\text{POE4}}$ to $\overline{\text{POE8}}$

   OR type: Signals input to several pins are formed as one signal through OR logic and the signal is transmitted into the LSI.
   AND type: Signals input to several pins are formed as one signal through AND logic and the signal is transmitted into the LSI.
   — When the pin function is output
   Each selected pin can output the same function.
2. When the port input is switched from a low level to the DREQ or the IRQ edge for the pins that are multiplexed with input/output and DREQ or IRQ, the corresponding edge is detected.
3. Do not set functions other than those specified in tables 21.17 to 21.20. Otherwise, correct operation cannot be guaranteed.
4. PFC setting in single-chip mode (MCU operating mode 3)
   In single-chip mode, do not set the PFC to select address bus, data bus, bus control, or the $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, CK, DACK, or TEND signals. If they are selected, address bus signals function as high- or low-level outputs, data bus signals function as high-impedance outputs, and the other output signals function as high-level outputs. As $\overline{\text{BREQ}}$ and $\overline{\text{WAIT}}$ function as inputs, do not leave them open. However, the bus-mastership-request inputs and external waits are disabled.

22.6.1 Register Descriptions

Port F is an 8-bit input-only port in the SH7083, SH7084, and SH7085; a 16-bit input-only port in the SH7086. Port F has the following register. For details on register addresses and register states during each processing, refer to section 27, List of Registers.

Table 22.11 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port F data register L	PFDRL	R	H'xxxx	H'FFFFD382	8, 16

22.6.2 Port F Data Register L (PFDRL)

The port F data register L (PFDRL) is a 16-bit read-only register that stores port F data. Bits PF7DR to PF0DR correspond to pins PF7 to PF0 (multiplexed functions omitted here) in the SH7083, SH7084, and SH7085. Bits PF15DR to PF0DR correspond to pins PF15 to PF0 (multiplexed functions omitted here) in the SH7086.

Any value written into these bits is ignored, and there is no effect on the state of the pins. When any of the bits are read, the pin state rather than the bit value is read directly. However, when an A/D converter analog input is being sampled, values of 1 are read out. Table 22.12 summarizes port F data register L read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	UA31 to UA0	Undefined	R/W	User Branch Destination Address When the user branch is not required, address 0 (H'00000000) must be set. The user branch destination must be an area other than the flash memory, an area other than the RAM area in which on-chip program has been transferred, or the external bus space. Note that the CPU must not branch to an area without the execution code and get out of control. The on-chip program download area and stack area must not be overwritten. If CPU runaway occurs or the download area or stack area is overwritten, the value of flash memory cannot be guaranteed. The download of the on-chip program, initialization, initiation of the programming/erasing program must not be executed in the processing of the user branch destination. Programming or erasing cannot be guaranteed when returning from the user branch destination. The program data which has already been prepared must not be programmed. Store general registers R8 to R15. General registers R0 to R7 are available without storing them. Moreover, the programming/erasing interface registers must not be written to or RAM emulation mode must not be entered in the processing of the user branch destination. After the processing of the user branch has ended, the programming/erasing program must be returned to by using the RTS instruction. For the execution intervals of the user branch processing, see note 2 (User branch processing intervals) in section 23.8.3, Other Notes.

28.3.1 Clock Timing

Table 28.6 Clock Timing

Conditions: V_{CC} = 3.0 V to 3.6 V or 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +85°C (consumer applications), T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
EXTAL clock input frequency	f_{EX}	5	12.5	MHz	Figure 28.1
EXTAL clock input cycle time	t_{EXcyc}	80	200	ns	
EXTAL clock input low pulse width	t_{EXL}	20	—	ns	
EXTAL clock input high pulse width	t_{EXH}	20	—	ns	
EXTAL clock input rise time	t_{EXr}	—	5	ns	
EXTAL clock input fall time	t_{EXf}	—	5	ns	
CK clock output frequency	f_{OP}	10	40	MHz	Figure 28.2
CK clock output cycle time	t_{cyc}	25	100	ns	
CK clock output low pulse width	t_{CKL}	$1/2t_{cyc}$–7.5	—	ns	
CK clock output high pulse width	t_{CKH}	$1/2t_{cyc}$–7.5	—	ns	
CK clock output rise time	t_{CKr}	—	5	ns	
CK clock output fall time	t_{CKf}	—	5	ns	
Power-on oscillation settling time	t_{OSC1}	10	—	ms	Figure 28.3
Standby return oscillation settling time 1	t_{OSC2}	10	—	ms	Figure 28.4
Standby return oscillation settling time 2	t_{OSC3}	10	—	ms	Figure 28.5

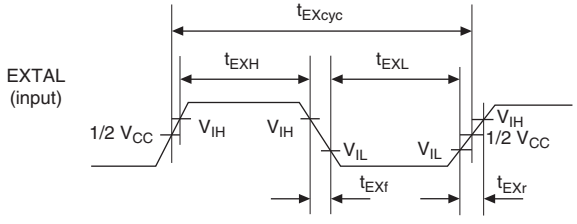

Figure 28.1 EXTAL Clock Input Timing

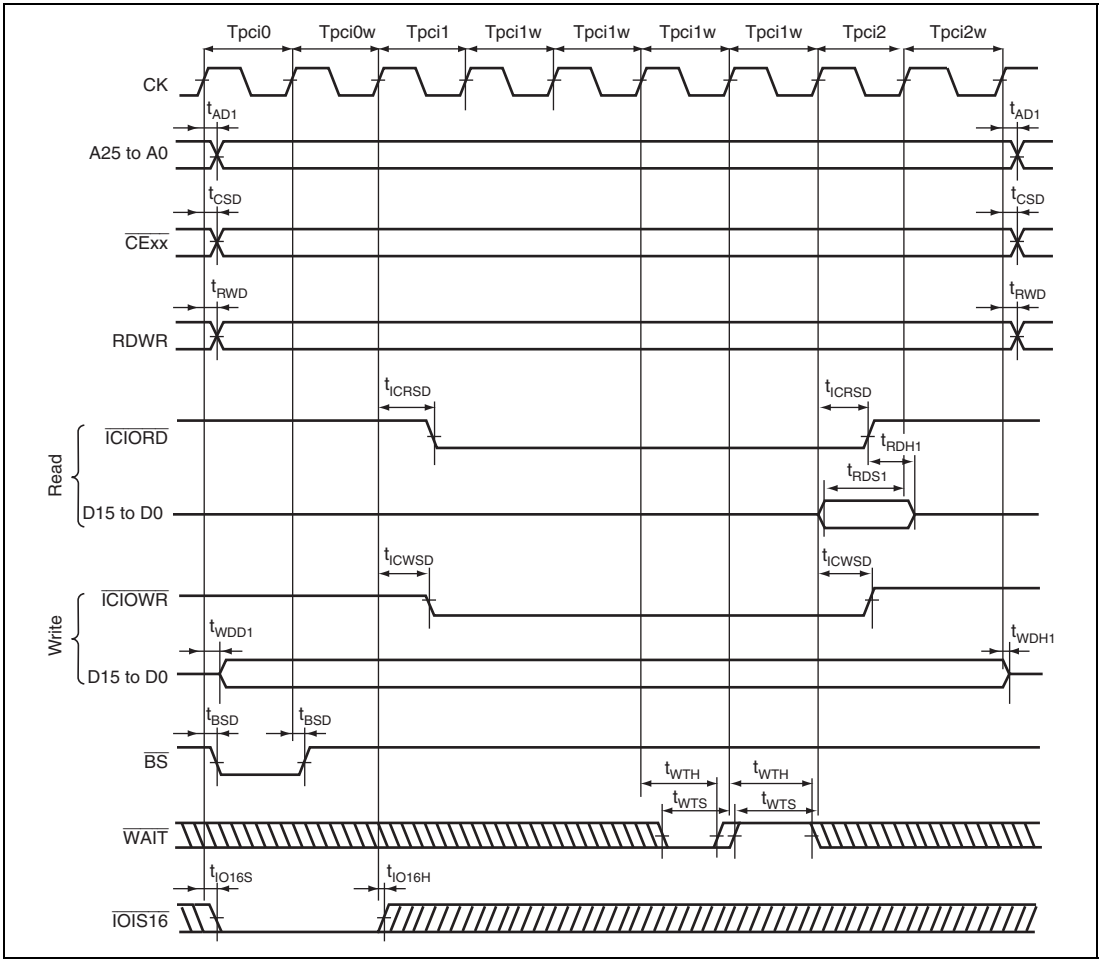

Figure 28.44 PCMCIA I/O Card Interface Bus Timing (TED = 2.5 Cycles, TEH = 1.5 Cycles, One External Wait Cycle)

28.3.14 UBC Trigger Timing

Table 28.19 UBC Trigger Timing

Conditions: V_{CC} = 3.0 V to 3.6 V or 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +85°C (consumer applications), T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{\text{UBCTRG}}$ delay time	t_{UBCTGD}	—	150	ns	Figure 28.61

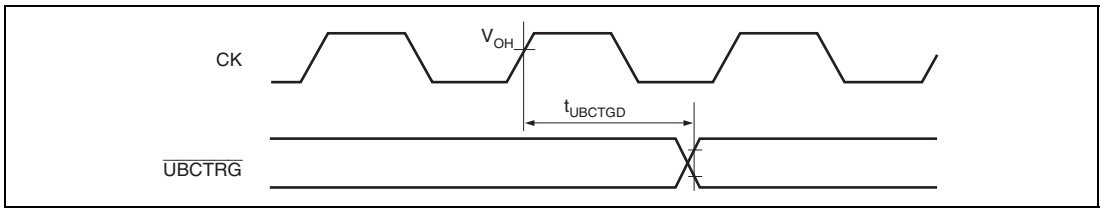

Figure 28.61 UBC Trigger Timing