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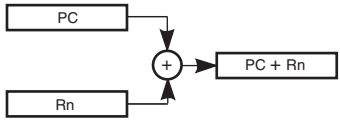
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70835an80bgv

Addressing Mode	Instruction Format	Effective Address Calculation Method	Calculation Formula
PC relative	Rn	Effective address is sum of PC and Rn. 	PC + Rn
Immediate	#imm:8	8-bit immediate data imm of TST, AND, OR, or XOR instruction is zero-extended.	—
	#imm:8	8-bit immediate data imm of MOV, ADD, or CMP/EQ instruction is sign-extended.	—
	#imm:8	8-bit immediate data imm of TRAPA instruction is zero-extended and multiplied by 4.	—

2.4.3 Instruction Formats

This section describes the instruction formats, and the meaning of the source and destination operands. The meaning of the operands depends on the instruction code. The following symbols are used in the table.

`xxxx`: Instruction code

`mmmm`: Source register

`nnnn`: Destination register

`iiii`: Immediate data

`dddd`: Displacement

8.2.3 DTC Source Address Register (SAR)

SAR is a 32-bit register that designates the source address of data to be transferred by the DTC.

SAR cannot be accessed directly from the CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

*: Undefined

8.2.4 DTC Destination Address Register (DAR)

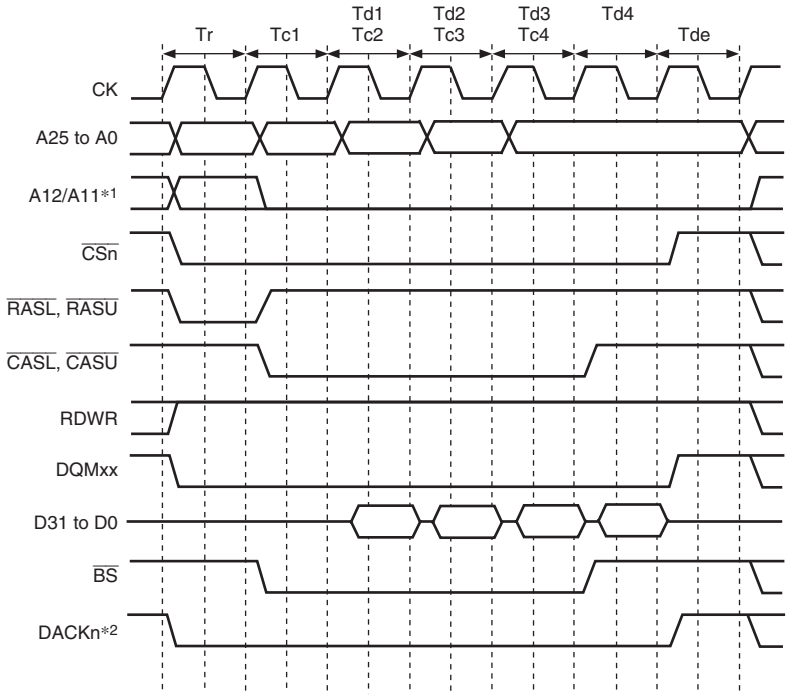
DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC.

DAR cannot be accessed directly from the CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

*: Undefined



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.23 Burst Read Timing (No Auto-Precharge)

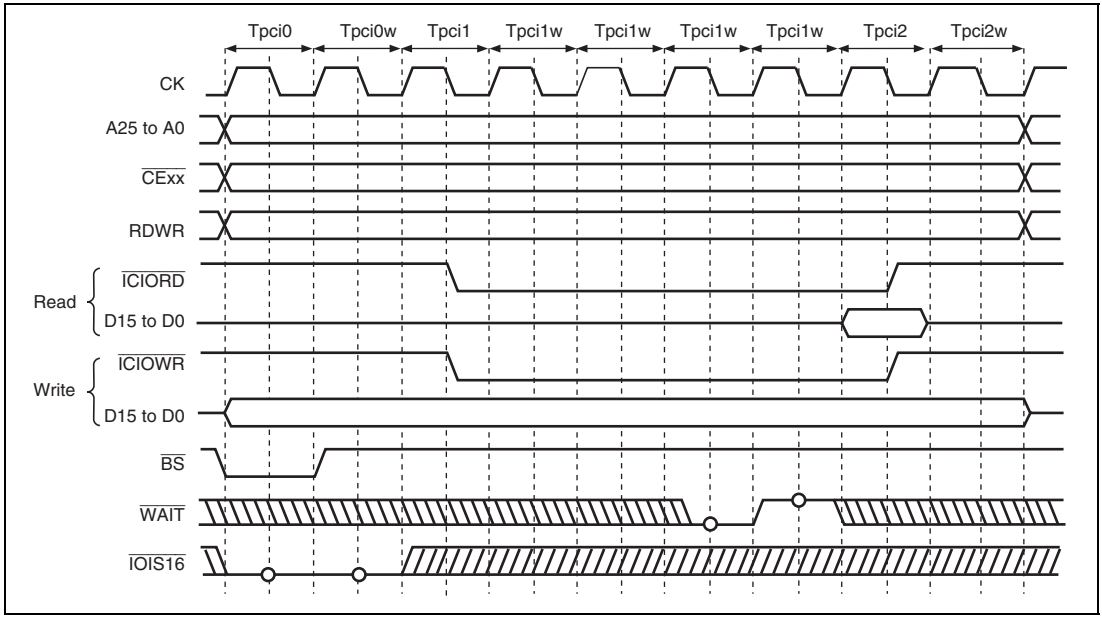


Figure 9.43 Wait Timing for PCMCIA I/O Card Interface Timing (TED[3:0] = B'0010, TEH[3:0] = B'0001, Hardware Wait 1)

- TSR_5

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	CMFU5	CMFV5	CMFW5
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CMFU5	0	R/(W)*[1]	Compare Match/Input Capture Flag U5 Status flag that indicates the occurrence of TGRU_5 input capture or compare match. [Setting conditions] • When TCNTU_5 = TGRU_5 and TGRU_5 is functioning as output compare register • When TCNTU_5 value is transferred to TGRU_5 by input capture signal and TGRU_5 is functioning as input capture register • When TCNTU_5 value is transferred to TGRU_5 and TGRU_5 is functioning as a register for measuring the pulse width of the external input signal. The transfer timing is specified by the IOC bits in timer I/O control register U_5 (TIORU_5).*[2] [Clearing conditions] • When DTC is activated by a TGIU_5 interrupt and the DISEL bit of MRB in DTC is 0 • When 0 is written to CMFU5 after reading CMFU5 = 1

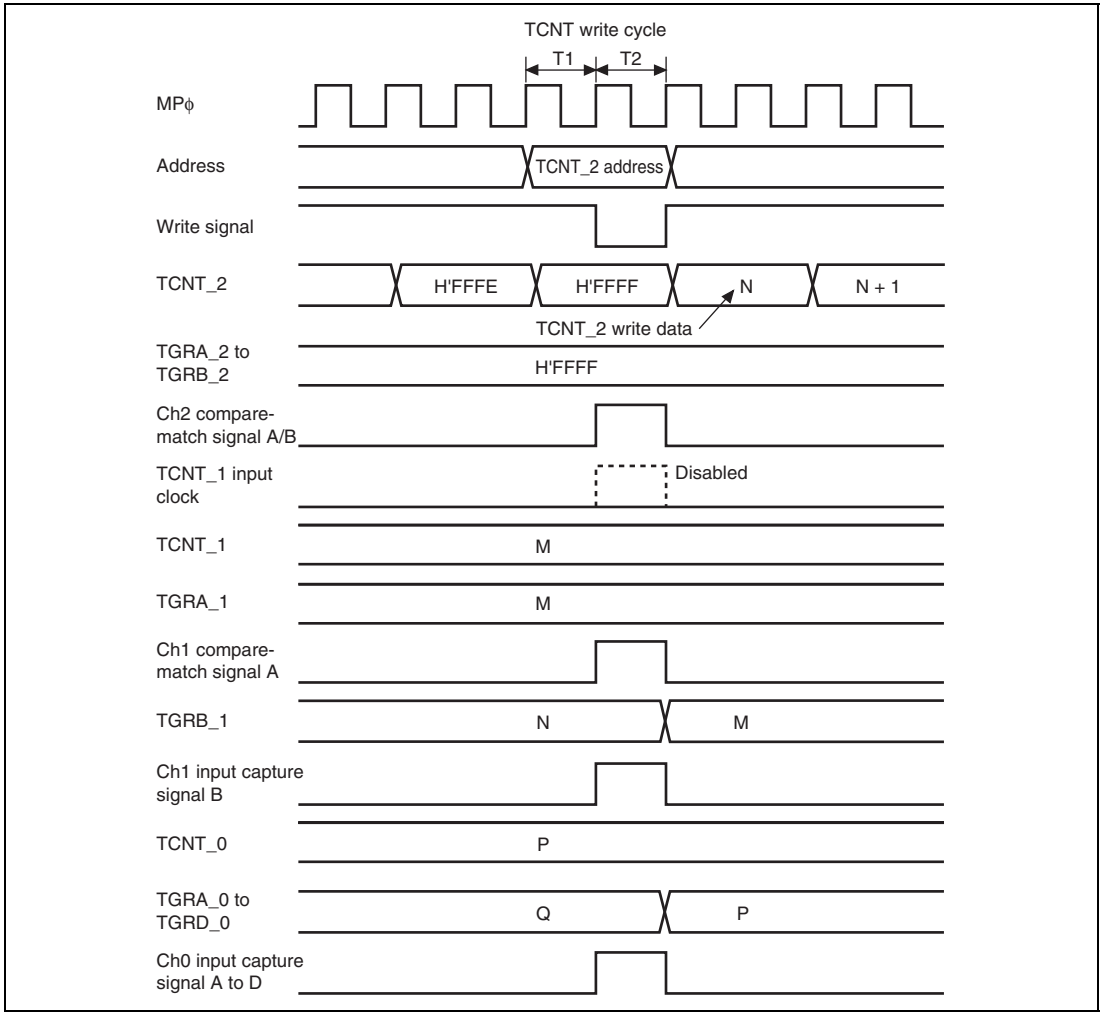


Figure 11.131 TCNT_2 Write and Overflow/Underflow Contention with Cascade Connection

11.7.18 Contention between TCNT Write and Overflow/Underflow

If there is an up-count or down-count in the T2 state of a TCNT write cycle, and overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 11.136 shows the operation timing when there is contention between TCNT write and overflow.

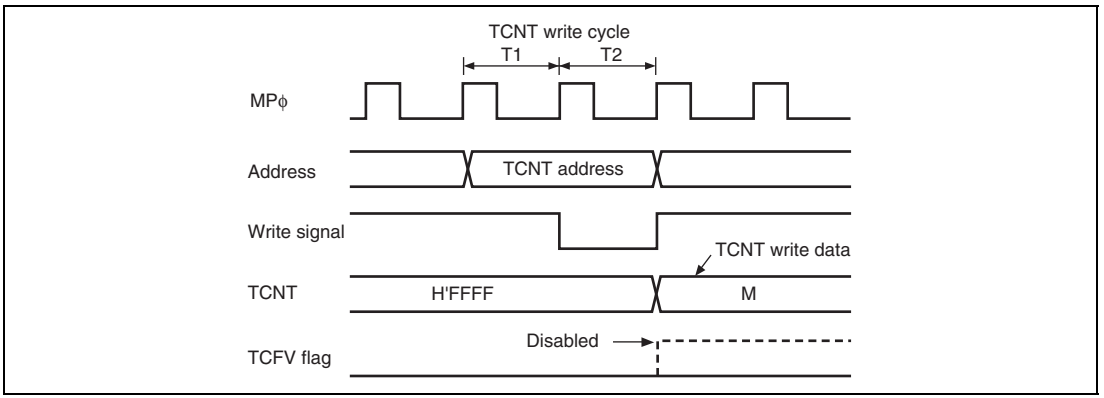


Figure 11.136 Contention between TCNT Write and Overflow

11.7.19 Cautions on Transition from Normal Operation or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from channel 3 or 4 normal operation or PWM mode 1 to reset-synchronized PWM mode, if the counter is halted with the output pins (TIOC3B, TIOC3D, TIOC4A, TIOC4C, TIOC4B, TIOC4D) in the high-level state, followed by the transition to reset-synchronized PWM mode and operation in that mode, the initial pin output will not be correct.

When making a transition from normal operation to reset-synchronized PWM mode, write H'11 to registers TIORH_3, TIORL_3, TIORH_4, and TIORL_4 to initialize the output pins to low level output, then set an initial register value of H'00 before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, first switch to normal operation, then initialize the output pins to low level output and set an initial register value of H'00 before making the transition to reset-synchronized PWM mode.

Operation when Error Occurs during Phase Counting Mode Operation, and Operation is Restarted in Phase Counting Mode: Figure 11.160 shows an explanatory diagram of the case where an error occurs in phase counting mode and operation is restarted in phase counting mode after re-setting.

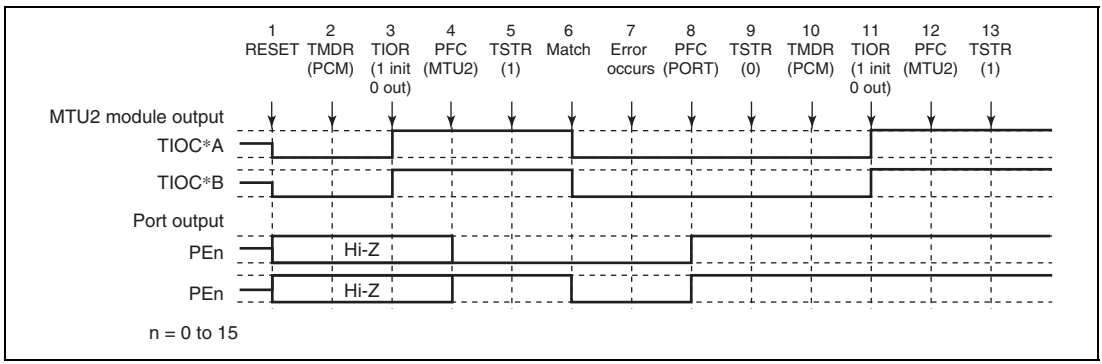


Figure 11.160 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

1 to 9 are the same as in figure 11.157.

10. Not necessary when restarting in phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

Tables 15.4 shows examples of SCBRR settings in asynchronous mode, and tables 15.5 shows examples of SCBRR settings in clock synchronous mode.

Table 15.4 Bit Rates and SCBRR Settings in Asynchronous Mode (1)

	Pϕ (MHz)																	
Bit Rate (bits/s)	10			12			14			16			18			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	177	-0.25	2	212	0.03	2	248	-0.17	3	70	0.03	3	79	-0.12	3	88	-0.25
150	2	129	0.16	2	155	0.16	2	181	0.16	2	207	0.16	2	233	0.16	3	64	0.16
300	2	64	0.16	2	77	0.16	2	90	0.16	2	103	0.16	2	116	0.16	2	129	0.16
600	1	129	0.16	1	155	0.16	1	181	0.16	1	207	0.16	1	233	0.16	2	64	0.16
1200	1	64	0.16	1	77	0.16	1	90	0.16	1	103	0.16	1	116	0.16	1	129	0.16
2400	0	129	0.16	0	155	0.16	0	181	0.16	0	207	0.16	0	233	0.16	1	64	0.16
4800	0	64	0.16	0	77	0.16	0	90	0.16	0	103	0.16	0	116	0.16	0	129	0.16
9600	0	32	-1.36	0	38	0.16	0	45	-0.93	0	51	0.16	0	58	-0.69	0	64	0.16
14400	0	21	-1.36	0	25	0.16	0	29	1.27	0	34	-0.79	0	38	0.16	0	42	0.94
19200	0	15	1.73	0	19	-2.34	0	22	-0.93	0	25	0.16	0	28	1.02	0	32	-1.36
28800	0	10	-1.36	0	12	0.16	0	14	1.27	0	16	2.12	0	19	-2.34	0	21	-1.36
31250	0	9	0.00	0	11	0.00	0	13	0.00	0	15	0.00	0	17	0.00	0	19	0.00
38400	0	7	1.73	0	9	-2.34	0	10	3.57	0	12	0.16	0	14	-2.34	0	15	1.73
115200	0	2	-9.58	0	2	8.51	0	3	-5.06	0	3	8.51	0	4	-2.34	0	4	8.51
500000	0	0*	-37.5	0	0*	-25.0	0	0*	-12.5	0	0*	0.00	0	0*	12.5	0	0*	25.0

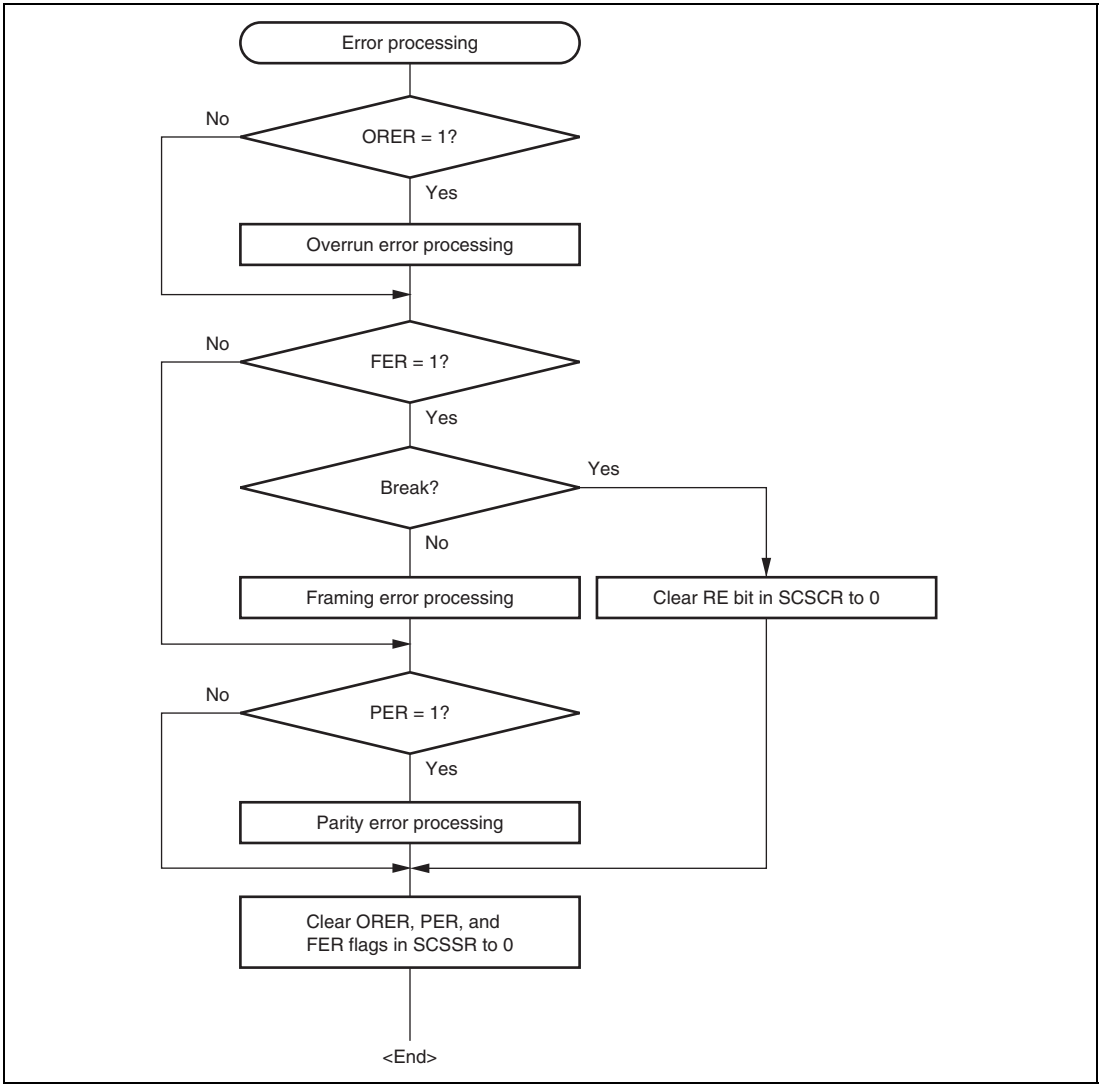


Figure 15.6 Sample Flowchart for Receiving Serial Data (Asynchronous Mode) (2)

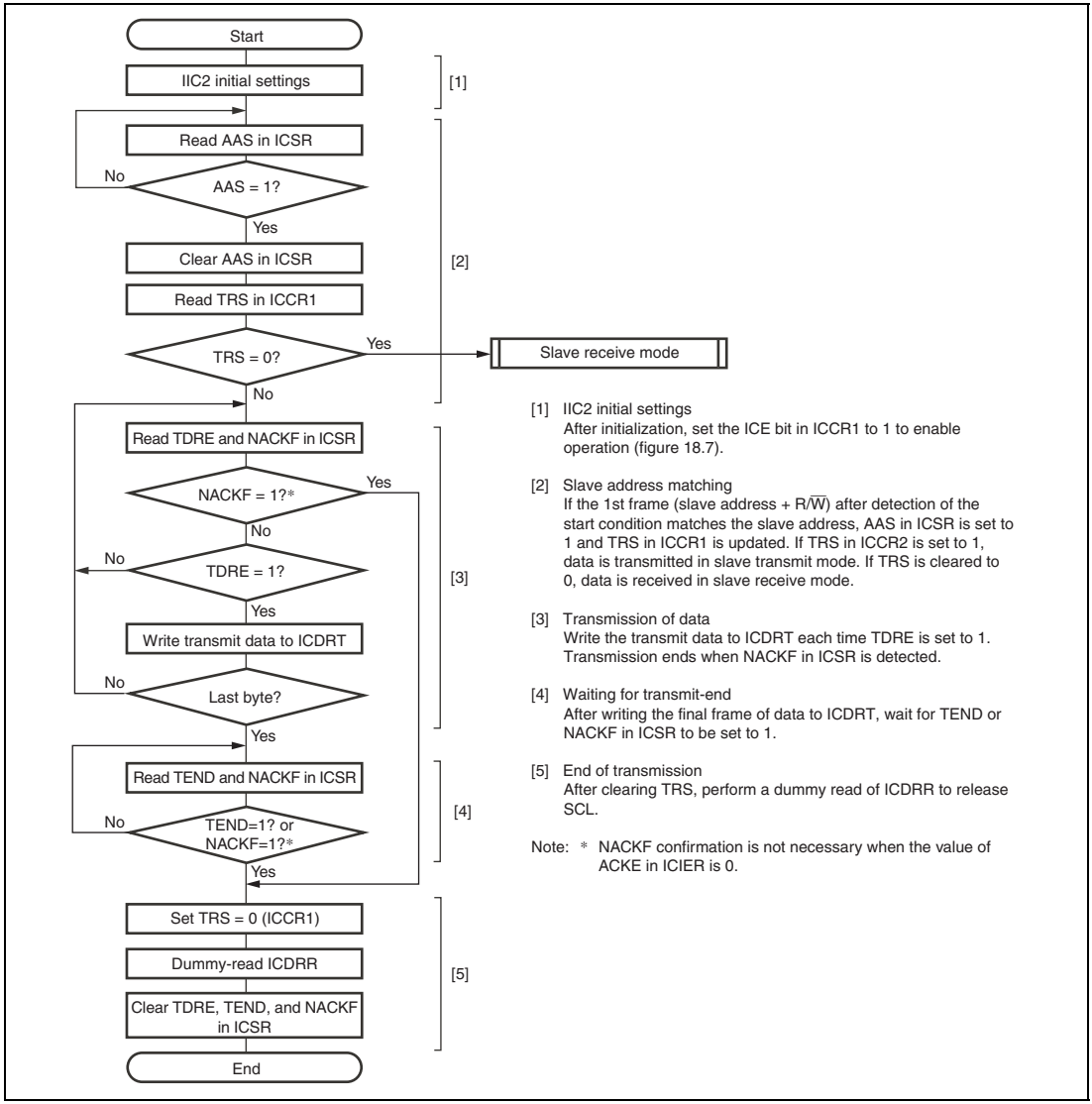


Figure 18.22 Sample Flowchart for Slave Transmit Mode

19.2 Input/Output Pins

Table 19.1 summarizes the input pins used by the A/D converter. The SH7083/SH7084/SH7085 has two A/D conversion modules and the SH7086 has three A/D conversion modules, each of which can be operated independently. The input channels of A/D modules 0 and 1 are divided into two channel groups.

Table 19.1 Pin Configuration

Module Type	Pin Name	I/O	Function		Product Classification SH7083	SH7084	SH7085	SH7086
Common	AV_{CC}	Input	Analog block power supply and reference voltage		√	√	√	√
	AV_{ref}	Input	A/D conversion reference voltage		√	—	√	√
	AV_{SS}	Input	Analog block ground and reference voltage		√	√	√	√
	$\overline{ADTRG}$	Input	A/D external trigger input pin		√	√	√	√
A/D module 0 (A/D_0)	AN0	Input	Analog input pin 0	Group 0	√	√	√	√
	AN1	Input	Analog input pin 1		√	√	√	√
	AN2	Input	Analog input pin 2	Group 1	√	√	√	√
	AN3	Input	Analog input pin 3		√	√	√	√
A/D module 1 (A/D_1)	AN4	Input	Analog input pin 4	Group 0	√	√	√	√
	AN5	Input	Analog input pin 5		√	√	√	√
	AN6	Input	Analog input pin 6	Group 1	√	√	√	√
	AN7	Input	Analog input pin 7		√	√	√	√
A/D module 2 (A/D_2)	AN8	Input	Analog input pin 8		—	—	—	√
	AN9	Input	Analog input pin 9		—	—	—	√
	AN10	Input	Analog input pin 10		—	—	—	√
	AN11	Input	Analog input pin 11		—	—	—	√
	AN12	Input	Analog input pin 12		—	—	—	√
	AN13	Input	Analog input pin 13		—	—	—	√
	AN14	Input	Analog input pin 14		—	—	—	√
	AN15	Input	Analog input pin 15		—	—	—	√

Note: The connected A/D module differs for each pin. The control registers of each module must be set.

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA8 I/O (port)	RDWR output (BSC)	IRQ2 input (INTC)	TCLKC input (MTU2)	—
	PA9 I/O (port)	CKE output (BSC)	IRQ3 input (INTC)	TCLKD input (MTU2)	—
	PA10 I/O (port)	$\overline{\text{CS0}}$ output (BSC)	$\overline{\text{POE4}}$ input (POE)	—	—
	PA11 I/O (port)	$\overline{\text{CS1}}$ output (BSC)	$\overline{\text{POE5}}$ input (POE)	—	—
	PA12 I/O (port)	$\overline{\text{WRL}}$/DQMLL output (BSC)	$\overline{\text{POE6}}$ input (POE)	—	—
	PA13 I/O (port)	$\overline{\text{WRH}}$/DQMLU output (BSC)	$\overline{\text{POE7}}$ input (POE)	—	—
	PA14 I/O (port)	$\overline{\text{RD}}$ output (BSC)	—	—	—
	PA15 I/O (port)	CK output (CPG)	—	—	—
	PA16 I/O (port)	$\overline{\text{AH}}$ output (BSC)	CKE output (BSC)	—	—
	PA17 I/O (port)	$\overline{\text{WAIT}}$ input (BSC)	—	—	—

Table 21.3 SH7085 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA0 I/O (port)	$\overline{\text{CS4}}$ output (BSC)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	$\overline{\text{CS5}}$/$\overline{\text{CE1A}}$ output (BSC)	TXD0 output (SCI)	—	—
	PA2 I/O (port)	A25 output (BSC)	DREQ0 input (DMAC)	IRQ0 input (INTC)	SCK0 I/O (SCI)
	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA6 I/O (port)	$\overline{\text{CS2}}$ output (BSC)	TCLKA input (MTU2)	—	—
	PA7 I/O (port)	$\overline{\text{CS3}}$ output (BSC)	TCLKB input (MTU2)	—	—
	PA8 I/O (port)	RDWR output (BSC)	IRQ2 input (INTC)	TCLKC input (MTU2)	—
	PA9 I/O (port)	$\overline{\text{FRAME}}$ output (BSC)	CKE output (BSC)	IRQ3 input (INTC)	TCLKD input (MTU2)
	PA10 I/O (port)	$\overline{\text{CS0}}$ output (BSC)	$\overline{\text{POE4}}$ input (POE)	—	—
	PA11 I/O (port)	$\overline{\text{CS1}}$ output (BSC)	$\overline{\text{POE5}}$ input (POE)	—	—
	PA12 I/O (port)	$\overline{\text{WRL}}$/DQMLL output (BSC)	$\overline{\text{POE6}}$ input (POE)	—	—
	PA13 I/O (port)	$\overline{\text{WRH}}$/$\overline{\text{WE}}$/DQMLU output (BSC)	$\overline{\text{POE7}}$ input (POE)	—	—
	PA14 I/O (port)	$\overline{\text{RD}}$ output (BSC)	—	—	—
	PA15 I/O (port)	CK output (CPG)	—	—	—

Table 21.11 SH7083 Multiplexed Pins (Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)
E	PE0 I/O (port)	DREQ0 input (DMAC)	TIOC0A I/O (MTU2)	TMS input (H-UDI)*	—	—
	PE1 I/O (port)	TEND0 output (DMAC)	TIOC0B I/O (MTU2)	$\overline{\text{TRST}}$ input (H-UDI)*	—	—
	PE2 I/O (port)	DREQ1 input (DMAC)	TIOC0C I/O (MTU2)	TDI input (H-UDI)*	—	—
	PE3 I/O (port)	TEND1 output (DMAC)	TIOC0D I/O (MTU2)	TDO output (H-UDI)*	—	—
	PE4 I/O (port)	TIOC1A I/O (MTU2)	RXD3 input (SCIF)	TCK input (H-UDI)*	—	—
	PE6 I/O (port)	$\overline{\text{CS7}}$ output (BSC)	TIOC2A I/O (MTU2)	SCK3 I/O (SCIF)	—	—
	PE7 I/O (port)	$\overline{\text{BS}}$ output (BSC)	TIOC2B I/O (MTU2)	$\overline{\text{UBCTRG}}$ output (UBC)	RXD2 input (SCI)	SSI I/O (SSU)
	PE8 I/O (port)	TIOC3A I/O (MTU2)	SCK2 I/O (SCI)	SSCK I/O (SSU)	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	TXD2 output (SCI)	SSO I/O (SSU)	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	TXD3 output (SCIF)	$\overline{\text{SCS}}$ I/O (SSU)	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	$\overline{\text{ASEBRKAK}}$ output (E10A)*	$\overline{\text{ASEBRK}}$ input (E10A)*	—
	PE14 I/O (port)	DACK0 output (DMAC)	TIOC4C I/O (MTU2)	—	—	—
	PE15 I/O (port)	CKE output (BSC)	DACK1 output (DMAC)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—

Note: * Only in F-ZTAT version.

Table 21.18 SH7084 Pin Functions in Each Operating Mode (1)

	Pin Name			
	On-Chip ROM Disabled (MCU Mode 0)		On-Chip ROM Disabled (MCU Mode 1)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
21, 37, 65, 80, 103	Vcc	Vcc	Vcc	Vcc
3, 27, 39, 55, 61, 71, 90, 101	Vss	Vss	Vss	Vss
23, 81, 109	VCL	VCL	VCL	VCL
100	AVcc	AVcc	AVcc	AVcc
97	AVss	AVss	AVss	AVss
82	PLLVss	PLLVss	PLLVss	PLLVss
74	EXTAL	EXTAL	EXTAL	EXTAL
72	XTAL	XTAL	XTAL	XTAL
75	MD0	MD0	MD0	MD0
73	MD1	MD1	MD1	MD1
77	FWE	FWE	FWE	FWE
84	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
35	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
76	NMI	NMI	NMI	NMI
33	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$
51	PA0	PA0/$\overline{\text{CS4}}$/RXD0	PA0	PA0/$\overline{\text{CS4}}$/RXD0
50	PA1	PA1/$\overline{\text{CS5}}$/TXD0	PA1	PA1/$\overline{\text{CS5}}$/TXD0
49	PA2	PA2/A25/DREQ0/IRQ0/SCK0	PA2	PA2/A25/DREQ0/IRQ0/SCK0
48	PA3	PA3/A24/RXD1	PA3	PA3/A24/RXD1
47	PA4	PA4/A23/TXD1	PA4	PA4/A23/TXD1
46	PA5	PA5/A22/DREQ1/IRQ1/SCK1	PA5	PA5/A22/DREQ1/IRQ1/SCK1
45	PA6	PA6/$\overline{\text{CS2}}$/TCLKA	PA6	PA6/$\overline{\text{CS2}}$/TCLKA
44	PA7	PA7/$\overline{\text{CS3}}$/TCLKB	PA7	PA7/$\overline{\text{CS3}}$/TCLKB
43	PA8	PA8/RDWR/IRQ2/TCLKC	PA8	PA8/RDWR/IRQ2/TCLKC
42	PA9	PA9/CKE/IRQ3/TCLKD	PA9	PA9/CKE/IRQ3/TCLKD
41	$\overline{\text{CS0}}$	PA10/$\overline{\text{CS0}}$/$\overline{\text{POE4}}$	$\overline{\text{CS0}}$	PA10/$\overline{\text{CS0}}$/$\overline{\text{POE4}}$

	Pin Name			
	On-Chip ROM Disabled (MCU Mode 0)		On-Chip ROM Disabled (MCU Mode 1)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
16	A12	PC12/A12	A12	PC12/A12
17	A13	PC13/A13	A13	PC13/A13
18	A14	PC14/A14	A14	PC14/A14
19	A15	PC15/A15	A15	PC15/A15
70	D0	PD0/D0	D0	PD0/D0
69	D1	PD1/D1	D1	PD1/D1
68	D2	PD2/D2/TIC5U	D2	PD2/D2/TIC5U
67	D3	PD3/D3/TIC5V	D3	PD3/D3/TIC5V
66	D4	PD4/D4/TIC5W	D4	PD4/D4/TIC5W
64	D5	PD5/D5/TIC5US	D5	PD5/D5/TIC5US
63	D6	PD6/D6/TIC5VS	D6	PD6/D6/TIC5VS
62	D7	PD7/D7/TIC5WS	D7	PD7/D7/TIC5WS
60	PD8/(AUDATA0*2)	PD8/D8/TIOC3AS	D8/(AUDATA0*2)	PD8/D8/TIOC3AS
59	PD9/(AUDATA1*2)	PD9/D9/TIOC3BS	D9/(AUDATA1*2)	PD9/D9/TIOC3BS
58	PD10 /(AUDATA2*2)	PD10/D10/TIOC3CS	D10/(AUDATA2*2)	PD10/D10/TIOC3CS
57	PD11 /(AUDATA3*2)	PD11/D11/TIOC3DS	D11/(AUDATA3*2)	PD11/D11/TIOC3DS
56	PD12	PD12/D12/TIOC4AS	D12	PD12/D12/TIOC4AS
54	PD13	PD13/D13/TIOC4BS	D13	PD13/D13/TIOC4BS
53	PD14/(AUDCK*2)	PD14/D14/TIOC4CS	D14/(AUDCK*2)	PD14/D14/TIOC4CS
52	PD15 /($\overline{\text{AUDSYNC}}$*2)	PD15/D15/TIOC4DS	D15/($\overline{\text{AUDSYNC}}$*2)	PD15/D15/TIOC4DS
85	PE0/(TMS*1)	PE0/DREQ0/TIOC0A	PE0/(TMS*1)	PE0/DREQ0/TIOC0A
86	PE1/($\overline{\text{TRST}}$*1)	PE1/TEND0/TIOC0B	PE1/($\overline{\text{TRST}}$*1)	PE1/TEND0/TIOC0B
87	PE2/(TDI*1)	PE2/DREQ1/TIOC0C	PE2/(TDI*1)	PE2/DREQ1/TIOC0C
88	PE3/(TDO*1)	PE3/TEND1/TIOC0D	PE3/(TDO*1)	PE3/TEND1/TIOC0D
89	PE4/(TCK*1)	PE4/TIOC1A/RXD3	PE4/(TCK*1)	PE4/TIOC1A/RXD3
102	PE5/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE5/$\overline{\text{CS6}}$/TIOC1B/TXD3	PE5/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE5/$\overline{\text{CS6}}$/TIOC1B/TXD3

Bit	Bit Name	Initial Value	R/W	Description
6	PA13MD2	0	R/W	PA13 Mode
5	PA13MD1	0	R/W	Select the function of the
4	PA13MD0	0*[2]	R/W	PA13/$\overline{\text{WRH}}$/$\overline{\text{WE}}$/DQMLU/$\overline{\text{POE7}}$ pin. 000: PA13 I/O (port) 001: $\overline{\text{WRH}}$/$\overline{\text{WE}}$/DQMLU output (BSC)*[3] 011: $\overline{\text{POE7}}$ input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PA12MD2	0	R/W	PA12 Mode
1	PA12MD1	0	R/W	Select the function of the PA12/$\overline{\text{WRL}}$/DQMLL/$\overline{\text{POE6}}$
0	PA12MD0	0*[2]	R/W	pin. 000: PA12 I/O (port) 001: $\overline{\text{WRL}}$/DQMLL output (BSC)*[3] 011: $\overline{\text{POE6}}$ input (POE) Other than above: Setting prohibited

Notes: 1. The initial value is 1 in the on-chip ROM enabled/disabled external-extension mode.
2. The initial value is 1 in the on-chip ROM disabled external-extension mode.
3. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

- Port A Control Register L3 (PACRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PA11 MD2	PA11 MD1	PA11 MD0	-	PA10 MD2	PA10 MD1	PA10 MD0	-	PA9 MD2	PA9 MD1	PA9 MD0	-	PA8 MD2	PA8 MD1	PA8 MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- PADRH (SH7086)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PA29 DR	PA28 DR	PA27 DR	PA26 DR	PA25 DR	PA24 DR	PA23 DR	PA22 DR	PA21 DR	PA20 DR	PA19 DR	PA18 DR	PA17 DR	PA16 DR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	PA29DR	0	R/W	See table 22.2.
12	PA28DR	0	R/W	
11	PA27DR	0	R/W	
10	PA26DR	0	R/W	
9	PA25DR	0	R/W	
8	PA24DR	0	R/W	
7	PA23DR	0	R/W	
6	PA22DR	0	R/W	
5	PA21DR	0	R/W	
4	PA20DR	0	R/W	
3	PA19DR	0	R/W	
2	PA18DR	0	R/W	
1	PA17DR	0	R/W	
0	PA16DR	0	R/W	

- **Programming/Erasure State**

In this state, the boot program must select the form of programming corresponding to the programming-selection command and then write data in response to 128-byte programming commands, or perform erasure in block units in response to the erasure-selection and block-erasure commands.

The programming and erasure commands are listed in table 23.14.

Table 23.14 Programming and Erasure Commands

Command	Command Name	Function
H'42	Selection of user boot MAT programming	Selects transfer of the program for user boot MAT programming.
H'43	Selection of user MAT programming	Selects transfer of the program for user MAT programming.
H'50	128-byte programming	Executes 128-byte programming.
H'48	Erasure selection	Selects transfer of the erasure program.
H'58	Block erasure	Executes erasure of the specified block.
H'52	Memory read	Reads from memory.
H'4A	Sum checking of user boot MAT	Executes sum checking of the user boot MAT.
H'4B	Sum checking of user MAT	Executes sum checking of the user MAT.
H'4C	Blank checking of user boot MAT	Executes blank checking of the user boot MAT.
H'4D	Blank checking of user MAT	Executes blank checking of the user MAT.
H'4F	Inquiry on boot program state	Requests information on the state of boot processing.

	External Space (Burst MPX-I/O)						
	32-bit Space						
Pin Name	Most Significant Byte	Second Byte	Third Byte	Least Significant Byte	Upper Word	Lower Word	Longword
D15 to D8	Address	Address	Address/ Data	Address	Address	Address/ Data	Address/ Data
D7 to D0	Address	Address	Address	Address/ Data	Address	Address/ Data	Address/ Data

[Legend]

R: Read

W: Write

Enabled: Chip select signals corresponding to accessed areas = Low.
The other chip select signals = High.

Table C.1 Pin States of Bus Related Signals (14)

		External Space (PCMCIA Memory Card Interface)			
			16-bit Space		
Pin Name		8-bit Space	Upper Byte	Lower Byte	Word/Longword
$\overline{CS0}$ to $\overline{CS8}$		H	H	H	H
$\overline{CE1A}$, $\overline{CE1B}$, $\overline{CE2A}$, $\overline{CE2B}$		Enabled	Enabled	Enabled	Enabled
$\overline{BS}$		L	L	L	L
$\overline{RASU}$, $\overline{RASL}$		H	H	H	H
$\overline{CASU}$, $\overline{CASL}$		H	H	H	H
DQMUU		H	H	H	H
DQMUL		H	H	H	H
DQMLU		H	H	H	H
DQMLL		H	H	H	H
$\overline{AH}$		L	L	L	L
$\overline{FRAME}$		H	H	H	H
RDWR	R	H	H	H	H
	W	L	L	L	L