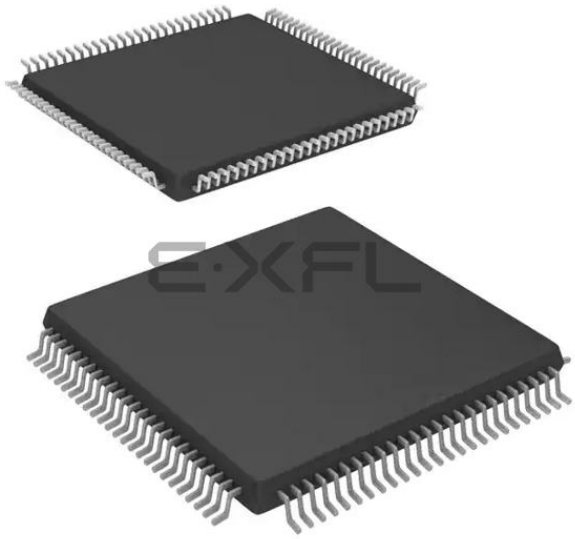

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70835an80ftv

23.3 Input/Output Pins 1251
23.4 Register Descriptions 1251
23.4.1 Registers 1251
23.4.2 Programming/Erasing Interface Registers 1254
23.4.3 Programming/Erasing Interface Parameters 1261
23.4.4 RAM Emulation Register (RAMER) 1276
23.5 On-Board Programming Mode 1278
23.5.1 Boot Mode 1278
23.5.2 User Program Mode 1282
23.5.3 User Boot Mode 1293
23.6 Protection 1298
23.6.1 Hardware Protection 1298
23.6.2 Software Protection 1299
23.6.3 Error Protection 1299
23.7 Flash Memory Emulation in RAM 1301
23.8 Usage Notes 1304
23.8.1 Switching between User MAT and User Boot MAT 1304
23.8.2 Interrupts during Programming/Erasing 1305
23.8.3 Other Notes 1307
23.9 Supplementary Information 1309
23.9.1 Specifications of the Standard Serial Communications Interface in Boot Mode 1309
23.9.2 Areas for Storage of the Procedural Program and Data for Programming 1339
23.10 Programmer Mode 1346

Section 24 Mask ROM 1347
24.1 Usage Notes 1348
24.1.1 Module Standby Mode Setting 1348

Section 25 RAM 1349
25.1 Usage Notes 1350
25.1.1 Module Standby Mode Setting 1350
25.1.2 Address Error 1350
25.1.3 Initial Values in RAM 1350

Section 26 Power-Down Modes 1351
26.1 Features 1351
26.1.1 Types of Power-Down Modes 1351
26.2 Input/Output Pins 1353
26.3 Register Descriptions 1354

Classification	Symbol	I/O	Name	Function
A/D converter (ADC)	AN15 to AN0	I	Analog input pins	Analog input pins. AN7 to AN0 are available in the SH7083/SH7084/SH7085.
	$\overline{\text{ADTRG}}$	I	A/D conversion trigger input	External trigger input pin for starting A/D conversion.
	AVref	I	Analog reference power supply	Reference voltage pin for the A/D converter. Available only in the SH7083/SH7085/SH7086. (In the SH7084, this pin is connected to AVcc inside this LSI.)
	AVcc	I	Analog power supply	Power supply pin for the A/D converter. Connect all AVcc pins to the system power supply (Vcc) when the A/D converter is not used. The A/D converter does not work if any pin is open.
	AVss	I	Analog ground	Ground pin for the A/D converter. Connect it to the system ground (0 V). Connect all AVss pins to the system ground (0 V) correctly. The A/D converter does not work if any pin is open.
I/O ports	PA29 to PA0	I/O	General port	30-bit general input/output port pins. PA15 to PA12, PA10 to PA7, and PA5 to PA3 are available in the SH7083. PA17 to PA0 are available in the SH7084. PA25 to PA0 are available in the SH7085.
	PB9 to PB0	I/O	General port	10-bit general input/output port pins. PB9 to PB4 and PB2 to PB0 are available in the SH7083.
	PC25 to PC18, PC15 to PC0	I/O	General port	24-bit general input/output port pins. PC15 to PC0 are available in the SH7083/SH7084/SH7085.

2.5 Instruction Set

2.5.1 Instruction Set by Type

Table 2.10 lists the instructions classified by type.

Table 2.10 Instruction Types

Type	Kinds of Instruction	Op Code	Function	Number of Instructions
Data transfer instructions	5	MOV	Data transfer Immediate data transfer Peripheral module data transfer Structure data transfer	39
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Upper/lower swap	
		XTRCT	Extraction of middle of linked registers	
Arithmetic operation instructions	21	ADD	Binary addition	33
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Signed division initialization	
		DIV0U	Unsigned division initialization	
		DMULS	Signed double-precision multiplication	
		DMULU	Unsigned double-precision multiplication	
		DT	Decrement and test	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiply-and-accumulate, double-precision multiply-and-accumulate	
		MUL	Double-precision multiplication	

2.5.6 Branch Instructions

Table 2.15 Branch Instructions

Instruction		Operation	Code	Execution Cycles	T Bit
BF	label	If T = 0, disp × 2 + PC → PC; if T = 1, nop	10001011dddddddd	3/1*	—
BF/S	label	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, nop	10001111dddddddd	2/1*	—
BT	label	If T = 1, disp × 2 + PC → PC; if T = 0, nop	10001001dddddddd	3/1*	—
BT/S	label	Delayed branch, if T = 1, disp × 2 + PC → PC; if T = 0, nop	10001101dddddddd	2/1*	—
BRA	label	Delayed branch, disp × 2 + PC → PC	1010dddddddddddd	2	—
BRAF	Rm	Delayed branch, Rm + PC → PC	0000mmmm00100011	2	—
BSR	label	Delayed branch, PC → PR, disp × 2 + PC → PC	1011dddddddddddd	2	—
BSRF	Rm	Delayed branch, PC → PR, Rm + PC → PC	0000mmmm00000011	2	—
JMP	@Rm	Delayed branch, Rm → PC	0100mmmm00101011	2	—
JSR	@Rm	Delayed branch, PC → PR, Rm → PC	0100mmmm00001011	2	—
RTS		Delayed branch, PR → PC	0000000000001011	2	—

Note: * One cycle when the branch is not executed.

3. When data access (address only) is specified as a break condition:

   The address of the instruction immediately after the instruction that matched the break condition is saved in the stack. The instruction that matches the condition is executed, and the user break occurs before the next instruction is executed. However when a delay slot instruction matches the condition, the branch destination address is saved in the stack.

4. When data access (address + data) is specified as a break condition:

   When a data value is added to the break conditions, the address of an instruction that is within two instructions of the instruction that matched the break condition is saved in the stack. At which instruction the user break occurs cannot be determined accurately.

   When a delay slot instruction matches the condition, the branch destination address is saved in the stack. If the instruction following the instruction that matches the break condition is a branch instruction, the user break may occur after the branch instruction or delay slot has finished. In this case, the branch destination address is saved in the stack.

7.4.6 PC Trace

1. Setting PCTE in BRCR to 1 enables PC traces. When branch (branch instruction, and interrupt exception) is generated, the branch source address and branch destination address are stored in BRSR and BRDR, respectively.
2. The values stored in BRSR and BRDR are as given below due to the kind of branch.
   - If a branch occurs due to a branch instruction, the address of the branch instruction is saved in BRSR and the address of the branch destination instruction is saved in BRDR.
   - If a branch occurs due to an interrupt or exception, the value saved in stack due to exception occurrence is saved in BRSR and the start address of the exception handling routine is saved in BRDR.
3. BRSR and BRDR have four pairs of queue structures (eight pairs for the F-ZTAT version supporting full functions of E10A). The top of queues is read first when the address stored in the PC trace register is read. BRSR and BRDR share the read pointer. Read BRSR and BRDR in order, the queue only shifts after BRDR is read. After switching the PCTE bit (in BRCR) off and on, the values in the queues are invalid.
4. Since four pairs (eight pairs for the F-ZTAT version supporting full functions of E10A) of queue are shared with the AUD, set the PCTE bit in BRCR to 1 after setting the MSTP25 bit in STBCR5 to 0 and the AUDSRST bit in STBCR6 to 1. Although the AUD is only available in the F-ZTAT version supporting full functions of the E10A, this setting should also be made in the normal F-ZTAT version.

There is no access size specification when reading. The correct access start address is output in the least significant bit of the address, but since there is no access size specification, 32 bits are always read in a 32-bit device or 16 bits are always read in a 16-bit device. When writing, only the $\overline{\text{WRxx}}$ signal for the byte to be written is asserted.

It is necessary to control of outputing the data that has been read using $\overline{\text{RD}}$ when a buffer is established in the data bus. The RDWR signal is in a read state (high output) when no access has been carried out. Therefore, care must be taken when controlling the external data buffer using RDWR, to avoid collision.

Figures 9.3 and 9.4 show the basic timings of continuous accesses to normal space. If the WM bit in CSnWCR is cleared to 0, a Tnop cycle is inserted to evaluate the external wait (figure 9.3). If the WM bit in CSnWCR is set to 1, external waits are ignored and no Tnop cycle is inserted (figure 9.4).

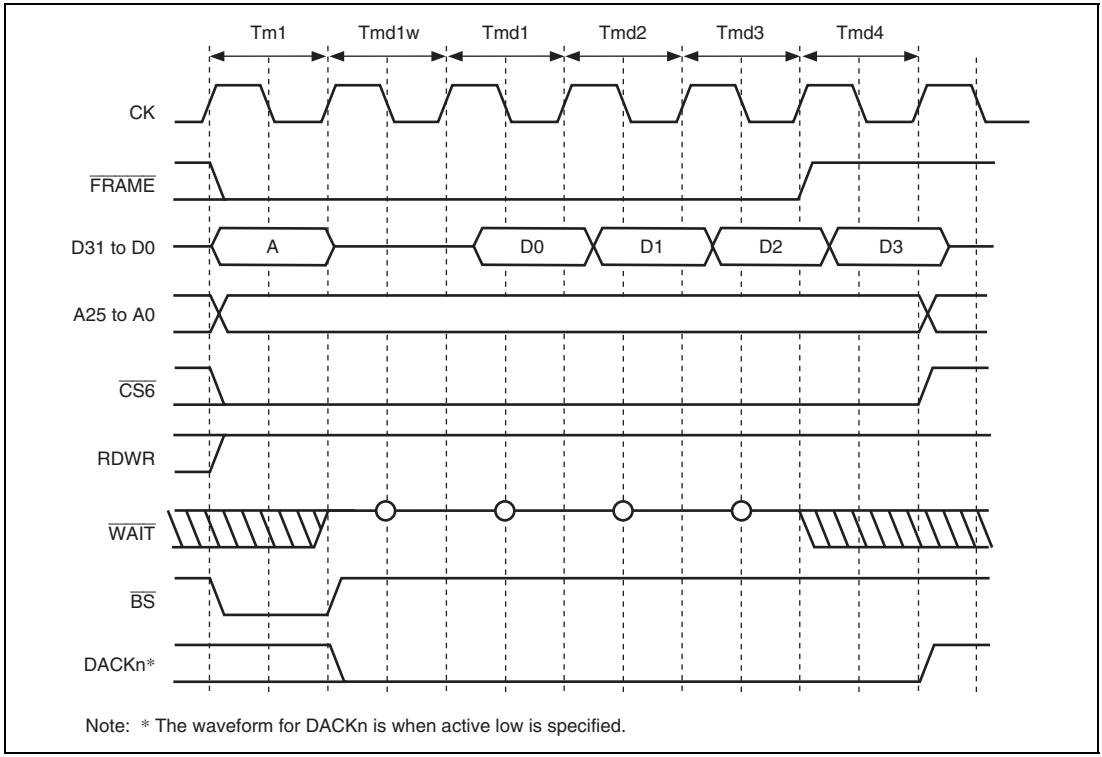


Figure 9.47 Burst MPX Space Access Timing (Burst Read, No Wait or Software Wait 1)

(i) Initial Output in Complementary PWM Mode

In complementary PWM mode, the initial output is determined by the setting of bits OLSN and OLSP in timer output control register 1 (TOCR1) or bits OLS1N to OLS3N and OLS1P to OLS3P in timer output control register 2 (TOCR2).

This initial output is the PWM pulse non-active level, and is output from when complementary PWM mode is set with the timer mode register (TMDR) until TCNT_4 exceeds the value set in the dead time register (TDDR). Figure 11.44 shows an example of the initial output in complementary PWM mode.

An example of the waveform when the initial PWM duty value is smaller than the TDDR value is shown in figure 11.45.

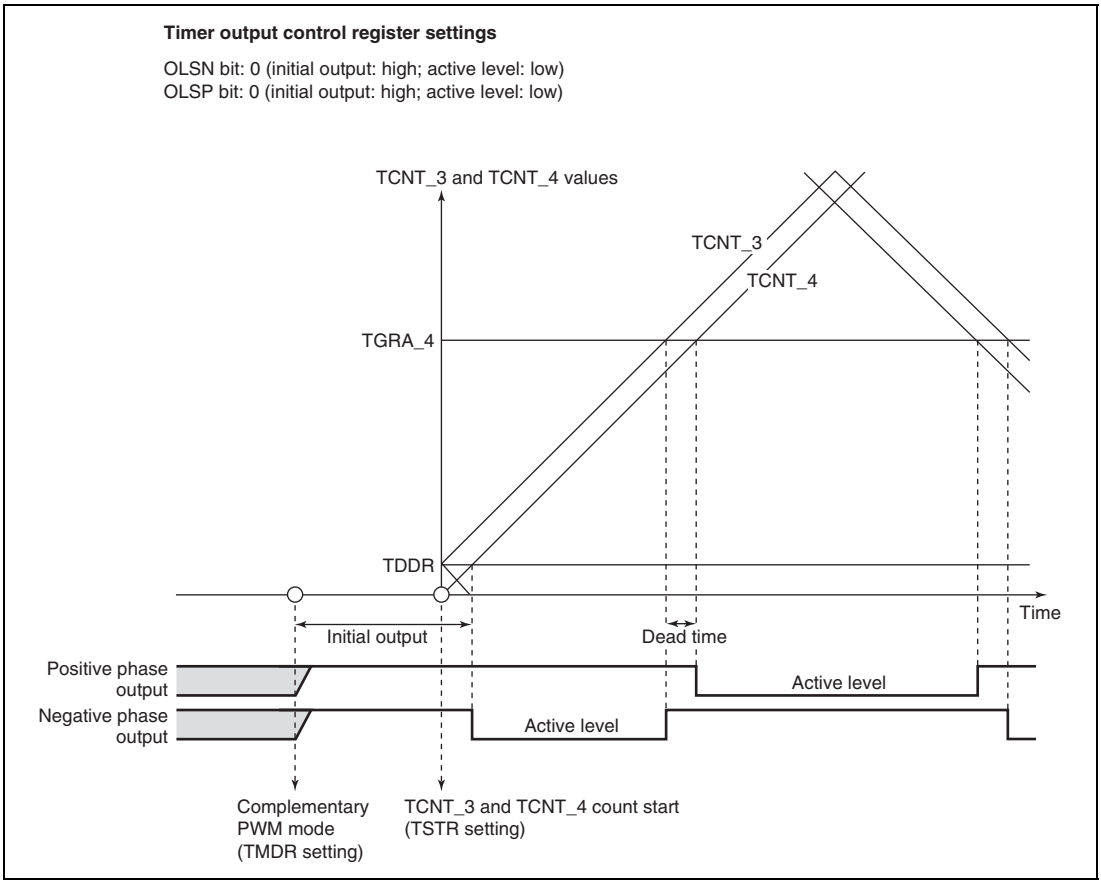


Figure 11.44 Example of Initial Output in Complementary PWM Mode (1)

Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in PWM Mode 2: Figure 11.155 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

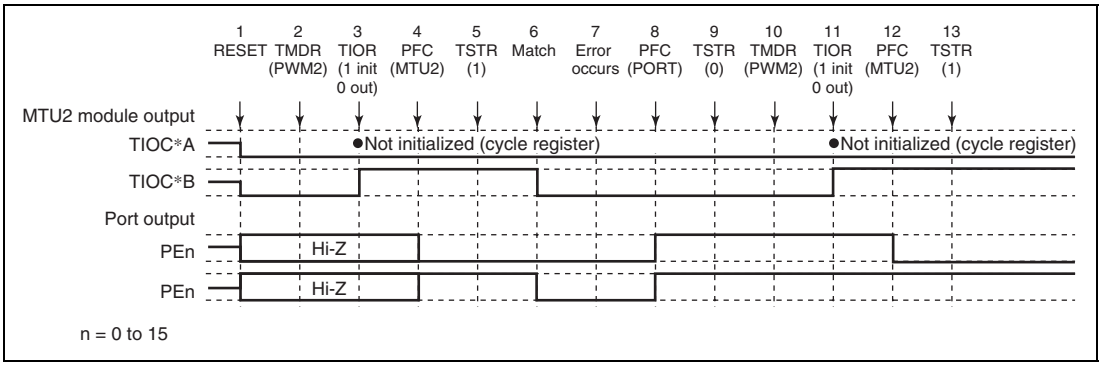


Figure 11.155 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2

1 to 9 are the same as in figure 11.153.

10. Not necessary when restarting in PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized.)
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

Section 12 Multi-Function Timer Pulse Unit 2S (MTU2S)

This LSI has an on-chip multi-function timer pulse unit 2S (MTU2S) that comprises three 16-bit timer channels. The MTU2S includes channels 3 to 5 of the MTU2. For details, refer to section 11, Multi-Function Timer Pulse Unit 2 (MTU2). To distinguish from the MTU2, "S" is added to the end of the MTU2S input/output pin and register names. For example, TIOC3A is called TIOC3AS and TGRA_3 is called TGRA_3S in this section.

The MTU2S can operate at 80 MHz max. for complementary PWM output functions or at 40 MHz max. for the other functions.

15.3.8 Serial Port Register (SCSPTR)

SCSPTR is an 8-bit register that controls input/output and data for the ports multiplexed with the SCI function pins. It controls break signals during serial transmission and reception when writing of output data to the TXD pin is enabled by the settings of bits SPB0IO and SPB0DT. Also, bits SPB1IO and SPB1DT can be used to write output data to the SCK pin. The EIO bit enables or disables RXI interrupts. The CPU can always read and write to SCSPTR. When reading the value on the SCI pins, use the respective port register. For details, refer to section 22, I/O Ports.

Bit:	7	6	5	4	3	2	1	0
	EIO	-	-	-	SPB1IO	SPB1DT	SPB0IO	SPB0DT
Initial value:	0	0	0	0	0	-	0	1
R/W:	R/W	-	-	-	R/W	W	R/W	W

Bit	Bit Name	Initial value	R/W	Description
7	EIO	0	R/W	Error Interrupt Only Enables or disables RXI interrupts. While the EIO bit is set to 1, the SCI does not request an RXI interrupt to the CPU even if the RIE bit is set to 1. 0: While the RIE bit is 1, RXI and ERI interrupts are sent to the INTC. 1: While the RIE bit is 1, only the ERI interrupt is sent to the INTC.
6 to 4	—	All 0	—	Reserved These bits are always read as 0. The write value should always be 0.
3	SPB1IO	0	R/W	Clock Port Input/Output in Serial Port Controls the SCK pin in combination with the SPB1DT bit, the C/$\overline{A}$ bit in SCSMR, and the CKE[1:0] bits in SCSCR.

Table 19.4 A/D Conversion Time (Single Mode)

		STC = 0											
		CKSL1 = 0						CKSL1 = 1					
		CKSL0 = 0			CKSL0 = 1			CKSL0 = 0			CKSL0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	2	—	6	2	—	5	2	—	4	2	—	3
Input sampling time	t_{SPL}	—	24	—	—	18	—	—	12	—	—	6	—
A/D conversion time	t_{CONV}	202	—	206	152	—	155	102	—	104	52	—	53

		STC = 1											
		CKSL1 = 0						CKSL1 = 1					
		CKSL0 = 0			CKSL0 = 1			CKSL0 = 0			CKSL0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	2	—	6	2	—	5	2	—	4	2	—	3
Input sampling time	t_{SPL}	—	36	—	—	27	—	—	18	—	—	9	—
A/D conversion time	t_{CONV}	258	—	262	194	—	197	130	—	132	66	—	67

Note: All values represent the number of states for Pϕ.

Table 19.5 A/D Conversion Time (Scan Mode)

				Conversion Time Calculation Example	
STC	**CKSL1**	**CKSL0**	**Conversion Time (State)**	**Pϕ = 25 MHz**	**Pϕ = 40 MHz**
0	0	0	200 (Fixed)	8 μs	5 μs
		1	150 (Fixed)	6 μs	3.8 μs
	1	0	100 (Fixed)	4 μs	2.5 μs
		1	50 (Fixed)	2 μs	Setting prohibited
1	0	0	256 (Fixed)	10.2 μs	6.4 μs
		1	192 (Fixed)	7.7 μs	4.8 μs
	1	0	128 (Fixed)	5.1 μs	3.2 μs
		1	64 (Fixed)	2.6 μs	Setting prohibited

	Pin Name			
	On-Chip ROM Enabled (MCU Mode 2)		Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
16	PC12	PC12/A12	PC12	PC12
17	PC13	PC13/A13	PC13	PC13
18	PC14	PC14/A14	PC14	PC14
19	PC15	PC15/A15	PC15	PC15
70	PD0	PD0/D0	PD0	PD0
69	PD1	PD1/D1	PD1	PD1
68	PD2	PD2/D2/TIC5U	PD2	PD2/TIC5U
67	PD3	PD3/D3/TIC5V	PD3	PD3/TIC5V
66	PD4	PD4/D4/TIC5W	PD4	PD4/TIC5W
64	PD5	PD5/D5/TIC5US	PD5	PD5/TIC5US
63	PD6	PD6/D6/TIC5VS	PD6	PD6/TIC5VS
62	PD7	PD7/D7/TIC5WS	PD7	PD7/TIC5WS
60	PD8/(AUDATA0*2)	PD8/D8/TIOC3AS	D8/(AUDATA0*2)	PD8/TIOC3AS
59	PD9/(AUDATA1*2)	PD9/D9/TIOC3BS	D9/(AUDATA1*2)	PD9/TIOC3BS
58	PD10 /(AUDATA2*2)	PD10/D10/TIOC3CS	D10/(AUDATA2*2)	PD10/TIOC3CS
57	PD11 /(AUDATA3*2)	PD11/D11/TIOC3DS	D11/(AUDATA3*2)	PD11/TIOC3DS
56	PD12	PD12/D12/TIOC4AS	D12	PD12/TIOC4AS
54	PD13	PD13/D13/TIOC4BS	D13	PD13/TIOC4BS
53	PD14/(AUDCK*2)	PD14/D14/TIOC4CS	D14/(AUDCK*2)	PD14/TIOC4CS
52	PD15 /($\overline{\text{AUDSYNC}}$*2)	PD15/D15/TIOC4DS	D15/($\overline{\text{AUDSYNC}}$*2)	PD15/TIOC4DS
85	PE0/(TMS*1)	PE0/DREQ0/TIOC0A	PE0/(TMS*1)	PE0/DREQ0/TIOC0A
86	PE1/($\overline{\text{TRST}}$*1)	PE1/TEND0/TIOC0B	PE1/($\overline{\text{TRST}}$*1)	PE1/TIOC0B
87	PE2/(TDI*1)	PE2/DREQ1/TIOC0C	PE2/(TDI*1)	PE2/DREQ1/TIOC0C
88	PE3/(TDO*1)	PE3/TEND1/TIOC0D	PE3/(TDO*1)	PE3/TIOC0D
89	PE4/(TCK*1)	PE4/TIOC1A/RXD3	PE4/(TCK*1)	PE4/TIOC1A/RXD3
102	PE5/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE5/$\overline{\text{CS6}}$/TIOC1B/TXD3	PE5/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE5/TIOC1B/TXD3

21.1.3 Port B I/O Register L (PBIORL)

PBIORL is a 16-bit readable/writable register that is used to set the pins on port B as inputs or outputs. Bits PB9IOR to PB0IOR correspond to pins PB9 to PB0 (names of multiplexed pins are here given as port names and pin numbers alone). PBIORL is enabled when the port B pins are functioning as general-purpose inputs/outputs (PB9 to PB0). In other states, PBIORL is disabled.

A given pin on port B will be an output pin if the corresponding bit in PBIORL is set to 1, and an input pin if the bit is cleared to 0. However, bit 3 of PBIORL is disabled in SH7083.

Bits 15 to 10 of PBIORL are reserved. These bits are always read as 0. The write value should always be 0.

The initial value of PBIORL is H'0000.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PB9 IOR	PB8 IOR	PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

21.1.4 Port B Control Registers L1 to L3 (PBCRL1 to PBCRL3)

PBCRL1 to PBCRL3 are 16-bit readable/writable registers that are used to select the function of the multiplexed pins on port B.

SH7083:

- Port B Control Register L3 (PBCRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	PB9 MD2	PB9 MD1	PB9 MD0	-	PB8 MD2	PB8 MD1	PB8 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

21.1.6 Port C Control Registers L1 to L4, H1 to H3 (PCCRL1 to PCCRL4, PCCRH1 to PCCRH3)

PCCRL1 to PCCRL4 and PCCRH1 to PCCRH3 are 16-bit readable/writable registers that are used to select the functions of the multiplexed pins on port C.

SH7083/SH7084/SH7085:

- Port C Control Registers H3 to H1 (PCCRH3 to PCCRH1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Port C Control Register L4 (PCCRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	PC15 MD0	-	-	-	PC14 MD0	-	-	-	PC13 MD0	-	-	-	PC12 MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	PC15MD0	0*[1]	R/W	PC15 Mode Select the function of the PC15/A15 pin. 0: PC15 I/O (port) 1: A15 output (BSC)*[2]

Bit	Bit Name	Initial Value	R/W	Description
8	PC2MD0	0*[1]	R/W	PC2 Mode Select the function of the PC2/A2 pin. 0: PC2 I/O (port) 1: A2 output (BSC)*[2]
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PC1MD0	0*[1]	R/W	PC1 Mode Select the function of the PC1/A1 pin. 0: PC1 I/O (port) 1: A1 output (BSC)*[2]
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PC0MD0	0*[1]	R/W	PC0 Mode Select the function of the PC0/A0 pin. 0: PC0 I/O (port) 1: A0 output (BSC)*[2]

Notes: 1. The initial value is 1 in the on-chip ROM disabled external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MOA31 to MOA0	Undefined	R/W	MOA31 to MOA0 Store the start address of the programming destination on the user MAT. The consecutive 128-byte programming is executed starting from the specified start address of the user MAT. The MOA6 to MOA0 bits are always 0 because the start address of the programming destination is at the 128-byte boundary.

(3.2) Flash multipurpose data destination area parameter (FMPDR: general register R4 of CPU)

This parameter indicates the start address in the area which stores the data to be programmed in the user MAT. When the storage destination of the program data is in flash memory, an error occurs. The error occurrence is indicated by the WD bit (bit 2) in FPFR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MOD31	MOD30	MOD29	MOD28	MOD27	MOD26	MOD25	MOD24	MOD23	MOD22	MOD21	MOD20	MOD19	MOD18	MOD17	MOD16
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MOD15	MOD14	MOD13	MOD12	MOD11	MOD10	MOD9	MOD8	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

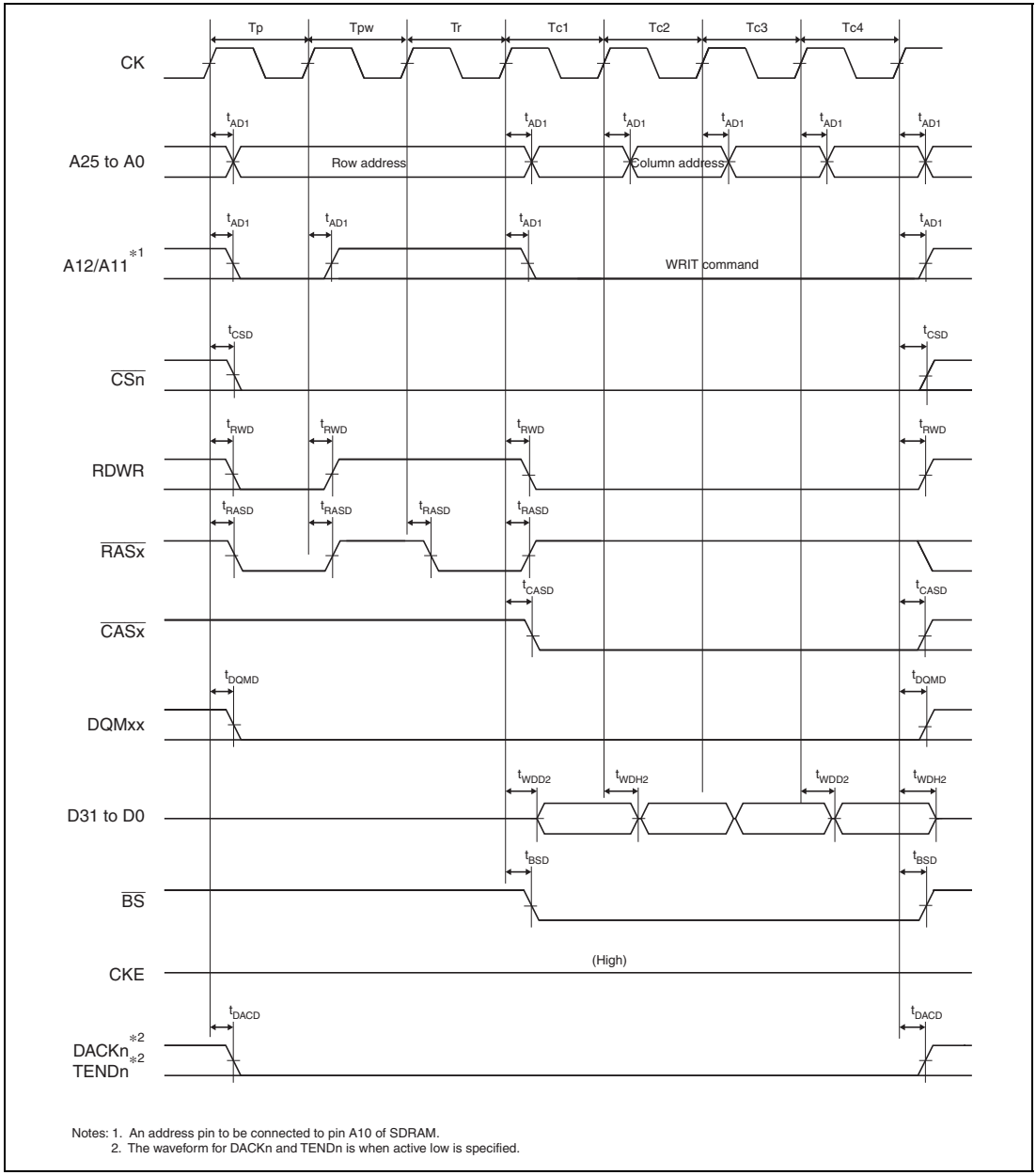
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MOD31 to MOD0	Undefined	R/W	MOD31 to MOD0 Store the start address of the area which stores the program data for the user MAT. The consecutive 128-byte data is programmed to the user MAT starting from the specified start address.

Table 23.18 (2) Usable Area for Erasure in User Program Mode

		Storable/Executable Area			Selected MAT	
	Item	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT
	Selecting on-chip program to be downloaded	√	√	√	√	
	Writing H'A5 to key register	√	√	√	√	
	Writing 1 to SCO in FCCS (download)	√	X	X		√
	Key register clearing	√	√	√	√	
	Judging download result	√	√	√	√	
	Download error processing	√	√	√	√	
	Setting initialization parameters	√	√	√	√	
	Initialization	√	X	X	√	
Erasing procedure	Judging initialization result	√	√	√	√	
	Initialization error processing	√	√	√	√	
	Writing H'5A to key register	√	√	√	√	
	Setting erasure parameters	√	X	√	√	
	Erasure	√	X	X	√	
	Judging erasure result	√	X	√	√	
	Erasing error processing	√	X	√	√	
	Key register clearing	√	X	√	√	

Table 23.18 (3) Usable Area for Programming in User Boot Mode

		Storable/Executable Area			Selected MAT		
	Item	On-Chip RAM	User Boot MAT	External Space	User MAT	User Boot MAT	Embedded Program Storage Area
Programming procedure	Program data storage area	√	X*[1]	√	—	—	—
	Selecting on-chip program to be downloaded	√	√	√		√	
	Writing H'A5 to key register	√	√	√		√	
	Writing 1 to SCO in FCCS (download)	√	X	X			√
	Key register clearing	√	√	√		√	
	Judging download result	√	√	√		√	
	Download error processing	√	√	√		√	
	Setting initialization parameters	√	√	√		√	
	Initialization	√	X	X		√	
	Judging initialization result	√	√	√		√	
	Initialization error processing	√	√	√		√	
	Switching MATs by FMATS	√	X	X	√		
	Writing H'5A to Key Register	√	X	√	√		



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 28.37 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: PRE + ACT + WRITE Commands, Different Row Addresses, WTRCD = 0 Cycle, TRWL = 0 Cycle)